Energy-Efficient and Robust Wireless Connectivity and Sensing Solutions for the Internet of Things

by

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Dedication

To my beloved family for their endless love and support.

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Abstract

In recent years, as smart sensor nodes are being ubiquitously adopted in different environments and applications, there has been an exponential growth in the number of Internet of Things (IoT) sensor nodes which is expected to reach a 1-trillion-node milestone sometime in our lifetime. Wireless connectivity and sensing are the centerpieces to the promised massive IoT networks, which commonly experience strict energy restraints. It has been demonstrated that wireless communication and sensing are some of the major barriers in Ultra-Low-Power (ULP) Wireless Sensor Node (WSN) design due to their high power consumption. Applications such as surveillance, biomedical, and wearable have spurred a tremendous amount of innovation in wireless devices and systems. However, the rollout of the modern wireless solutions has not been able to fully meet the requirements of the modern wireless era, *i.e.* leading to highly scalable wireless communication and sensing network infrastructure while maintaining the low-power and ULP regime. The small form factor and low power consumption requirement pose

severe limitations on the performance of wireless systems. One of the main challenges is achieving high levels of interference tolerance in densely populated wireless networks, in which ULP receivers experience significant degradations. Second, non-integrated millimeter-wave (mm-wave) wireless systems encounter excessive losses due to their distributed nature and fail to preserve the miniature form factor.

The objectives of this research are to analyze and address the aforementioned challenges by proposing new system design techniques as well as circuit architectures to offer end-to-end energy-efficient wireless solutions for connectivity and sensing. Three prototypes of the proposed systems were implemented for evaluation and are discussed in this thesis. The first prototype is a ULP interference-tolerant 433MHz receiver utilizing a novel Dual-Chirp On-Off-Keying (DC-OOK) modulation scheme. This radio consumes 110µW active power while achieving -103dBm sensitivity at 2.5kb/s data rate and a Signal-to-Interference-Ratio (SIR) up to -41dB. The second work is a 900MHz low-power blocker tolerant receiver with chirped OOK modulation that showcases a highly-selective receiver architecture leveraging a novel chirped N-path filter. The third prototype is a 50mW PLL-less fully integrated 60GHz FMCW radar transceiver with on-chip antennas that leverages a novel co-designed transmitter and receiver to enable an ADC-assisted chirp linearization scheme to compensate for chirp non-linearities with minimum power overhead. The prototypes showcased in this research prove the feasibility of simultaneously energy-efficient and blocker-tolerant wireless solutions while maintaining miniaturized form factor.

Chapter 1:

Introduction and Background

1.1 Emerging Computing Devices

Our lives have been forever altered by the introduction of new computing technologies and devices over the past few decades. Each decade a new class of computing technology emerges, according to Bell's Law [1]. In Bell's definition, a computer class is defined as a set of computers with a similar cost, programming environment, network, and user interface, where each class undergoes a standard product life cycle of growth and decline. Historically, there has been a downward trend in the volumetric size of computing devices since the introduction of mainframe computers in the 1960s, 100x every decade, in addition to an increase in production volume and a drop in manufacturing costs when transitioning to a newer generation, as shown in Figure 1.1. This trend has been driven by Moore's Law's prediction of technology scaling, which has made it possible to pack powerful computing devices into increasingly condensing

smart devices. In light of this historical trend, the next generation of emerging computing devices will be able to offer vigorous features with an array of applications in millimeter-scale form factor by the end of the decade.

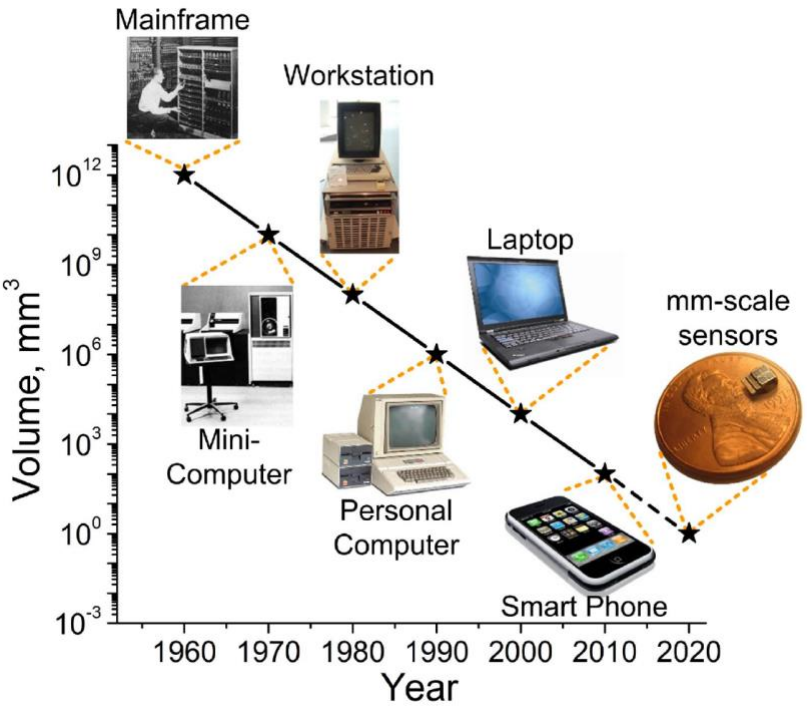


Figure 1.1 Evolution of computers shows 100x volume reduction of computing devices per decade [2].

1.2 Trends in IoT Wireless Sensor Nodes (WSNs)

Due to the exponential rise of smartphones and tablet PCs in the early 2000s–enabled by unprecedented levels of technology scaling–the number of connected IoT WSNs has outpaced

the global population, and this trend continues to grow to become multiple connected WSNs per individual, as shown in Figure 1.2. As the number of IoT connected devices per person have increased, they have reshaped our lives and have redefined how we interact with the world surrounding us.

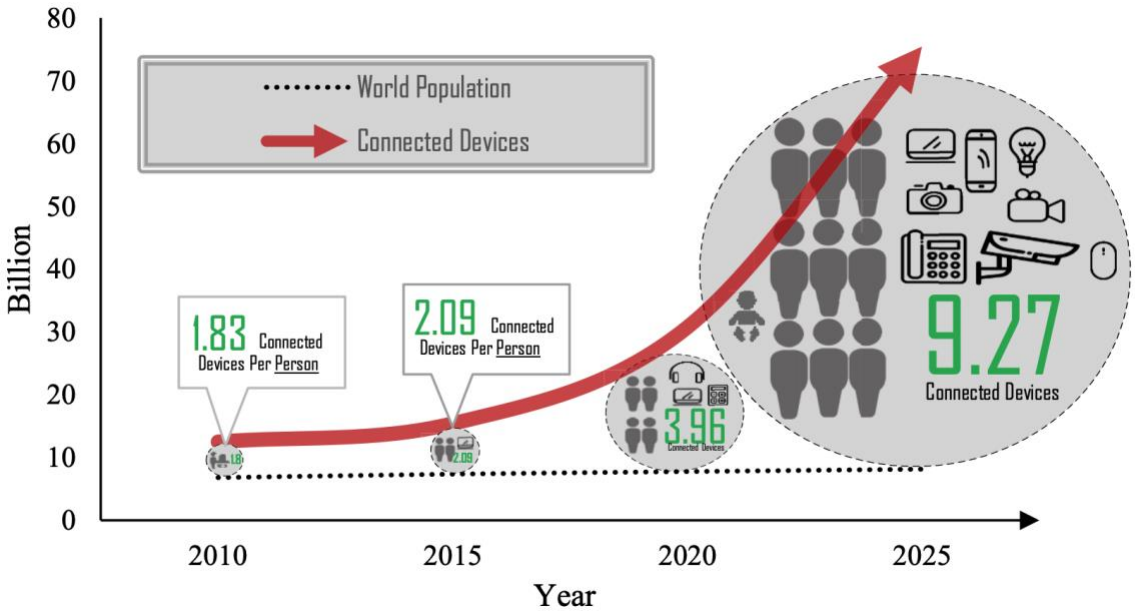


Figure 1.2 Number of IoT connected devices per person vs year [3].

In addition, the number of IoT-connected devices has now surpassed the overall number of non-IoT connected devices starting in 2021 and is expected to reach a record number of 31 billion by 2025, Figure 1.3. By 2025, the annual IP traffic from such an immense scale of WSNs could reach as high as 1 zettabytes. Considering that conventionally adopted wireless LAN links consume approximately 5μJ/bit for data transmission, the annual energy dissipation required to wireless transmit all of this data over a massive IoT network is:

$$Energy\ Dissipation = 8 \times 10^{21} \times 5 \times 10^{-6} = 4 \times 10^{16}\ Joules$$

This is almost equal to the annual electric energy used in Washington DC. Given the limitations of battery technologies and their relatively short lifecycle, this staggering figure illustrates how conventional wireless solutions fail to deliver the promised 100 billion or more connected WSNs and call for game-changing developments in low-power wireless technology. As such, more sustainable and cost-effective wireless solutions will be needed to facilitate widespread adoption of WSNs.

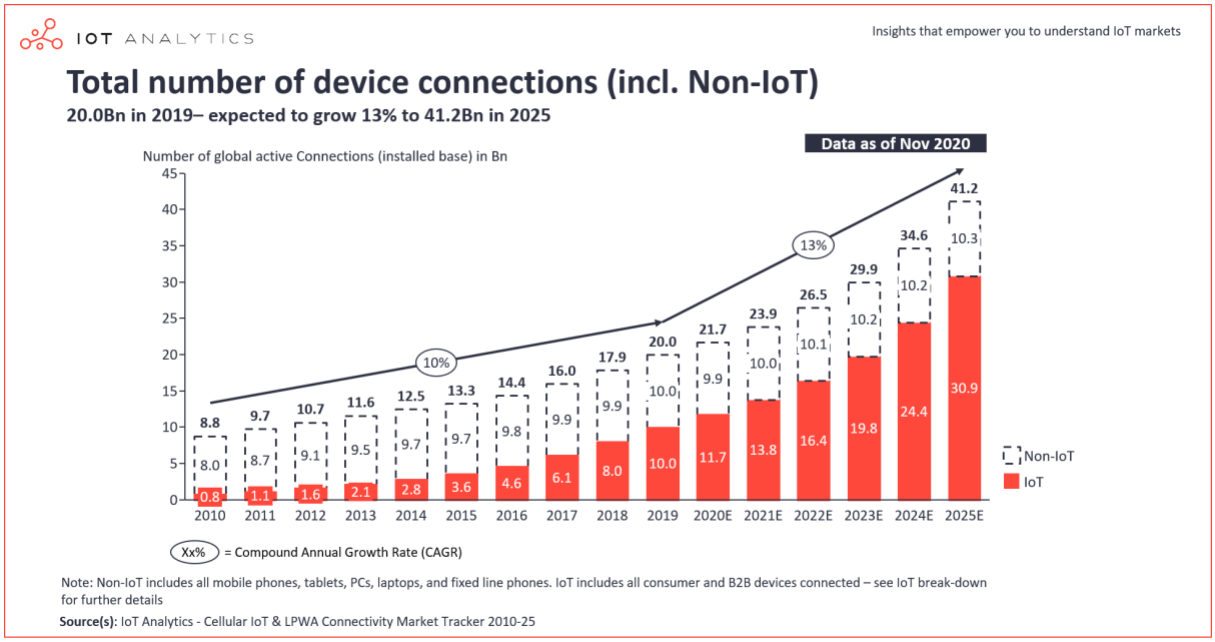


Figure 1.3 Total number of active device connections worldwide, source: IoT Analytics.

1.3 Radios in Wireless Sensor Nodes

Based on reports in the state-of-the-art publications and commercial WSN data sheets, it can be observed that wireless transceivers are among the most power-hungry blocks in WSNs. To obtain a better insight into the matter, the power consumption of the EKG WSN presented in [4] is broken down for different blocks in Figure 1.4. It is evident that the RF transmitter dominates the entire power consumption of the WSN and accounts for nearly 90% of the dissipated energy. In order to prevent such high-power consumption levels, duty-cycling the WSN operation can be done, but at the price of increased latency.

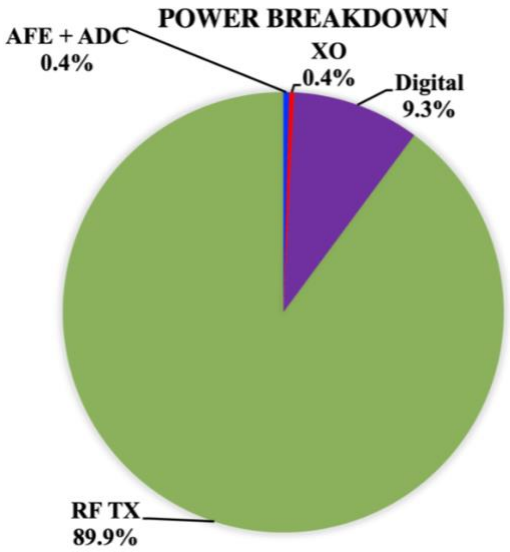


Figure 1.4 Power breakdown of the EKG WSN published in [4].

Wireless transceivers are the dominant consumer of energy due to several reasons. The receiving end components have high current requirements since they have to deal with high frequency signals in the RF and mm-wave frequency bands and amplify such signals at high frequency. Moreover, in order to operate the transceivers in the long-range domain under high sensitivity requirements, the RF frontend blocks must provide optimal noise performance, thereby requiring higher DC current consumption. On the transmitting side, the chip must generate and amplify power at RF and mm-wave frequencies, which poses an even greater challenge for the ULP transmitter design, especially at mm-wave frequency bands where the carrier frequency is close to the transistors' f_T/f_{MAX}. A global imperative to develop energy-efficient wireless systems has been stronger than ever due to the challenges mentioned above. While ULP radio design for IoT applications faces a number of practical challenges, achieving optimal performance in WSNs with extended or infinite battery lifetime necessitates gaining a deep understanding of design tradeoffs and requirements in ULP wireless system design. In the next section, such requirements and design tradeoffs will be discussed in depth.

1.4 ULP Radio Design Requirements and Tradeoffs

As the Internet of Things (IoT) era gains momentum, ULP radios are expected to gain a tremendous amount of demand. However, there are several design challenge in radios for IoT applications, including 1) achieving adequate sensitivity levels to satisfy the required range of communication, 2) ensuring the ULP power consumption regime to guarantee energy autonomy

while not compromising other crucial performance metrics, 3) ensuring sufficient interference tolerance levels for the WSNs to operate in the condensed spectrum of the modern IoT world, and 4) maintaining mm-scale form factors to accelerate pervasive adoption of the next generation of computers.

1.4.1 Sensitivity

Receivers are restricted to detecting and demodulating the smallest signal levels that their sensitivity can handle, and this is directly correlated with their power consumption. A receiver achieving enhanced sensitivity levels must have lower noise levels and sufficient signal amplification at RF and IF frequencies, resulting in higher DC current consumption. In order to cope with adverse scenarios, the receiver sensitivity specifications would normally be overdesigned, as any degradation in the receiver sensitivity would cripple a reliable communication link. There have been many contributions and studies made by research groups to reduce the power of radios, resulting in a significant improvement in ULP radio performance in numerous aspects, particularly sensitivity. In order to determine the trends and tradeoffs involved with ULP radio design and to identify the bottlenecks, a survey was conducted on the receiver chips published in top tier conference and journal publications [5].

The power consumption of a wireless receiver vs. its sensitivity is shown in Figure 1.5. As can be seen, with the exception of nano-Watt receivers, for every 20dB improvement in the receiver's sensitivity level or 10x improvement in communication range, the receiver requires a 10x increase in DC current. This simply implies that the receiver range and DC power

consumption scale linearly together, which can be a key limiting factor for deployment of energy-autonomous WSNs in remote areas.

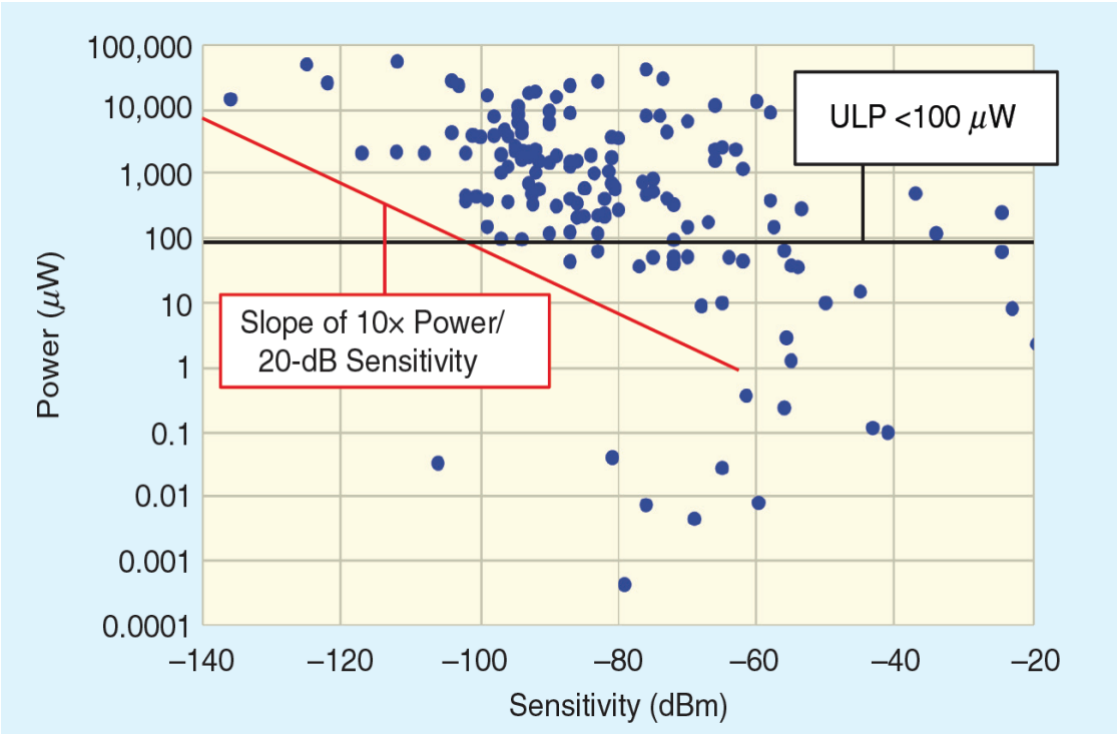


Figure 1.5 A survey of wireless receivers published in selected IEEE conferences and journals from 2005 – 2021 [5]

To make a more meaningful comparison between different receivers and gain a deeper understanding of ULP receiver design trends and tradeoffs, the power vs sensitivity chart needs to be revisited, which can be done by normalizing the sensitivity of the receiver to its data rate and plotting the normalized sensitivity vs power consumption, Figure 1.6. Where the normalized sensitivity is defined as follows:

$$S_{NORM} = S - 10log(\frac{Data\ Rate}{1kbps})$$

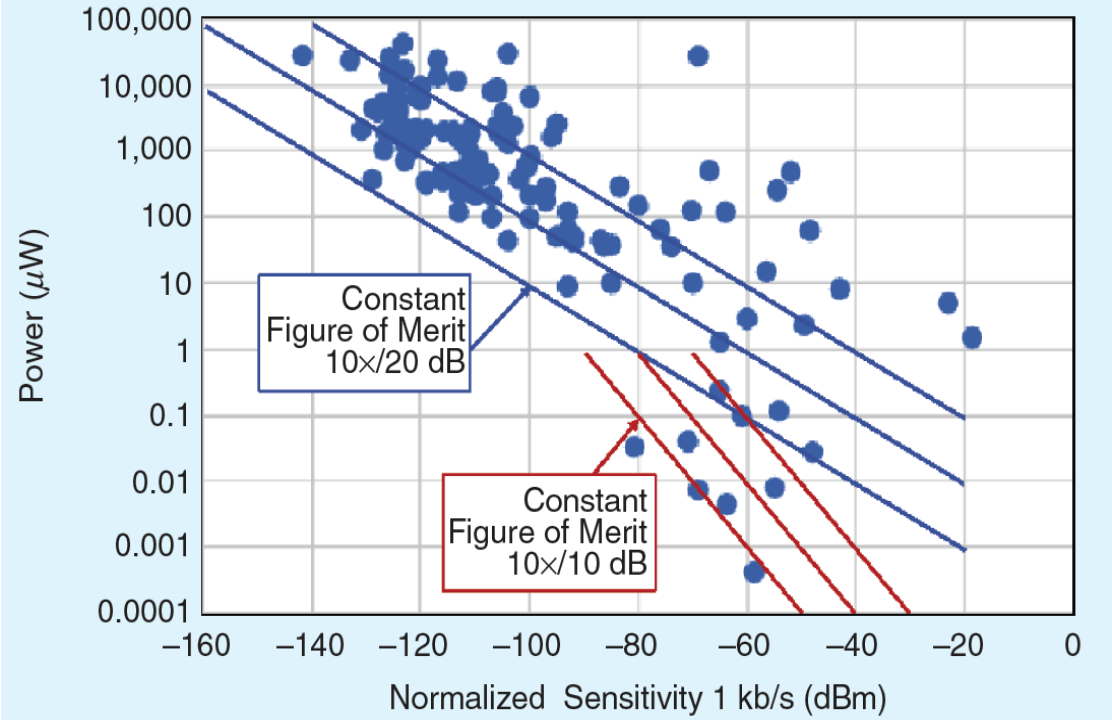


Figure 1.6 Normalized sensitivity vs power consumption for ULP receivers [5]

After normalizing the sensitivity, the spread in points is reduced, particularly for nano-Watt receivers as they have relatively low data rates, and as expected the performance of different radios can be visualized and compared more meaningfully.

1.4.2 Selectivity

There has been an explosive growth in the number of IoT wireless connections in recent years. Due to the limited bandwidth being shared among many standards, this has resulted in an unprecedented amount of RF spectrum congestion, particularly in the unlicensed frequency bands, Figure 1.7. As a result, ULP radios' operation could be significantly degraded, potentially resulting in less reliable wireless links and hinderance of the widespread adoption of WSNs. In addition, fully integrated ULP radios face even greater challenges, since maintaining the receiver selectivity in a populated spectrum requires higher levels of power consumption, specifically in narrowband channels [6], which in turn would lead to shorter battery lifetimes in the WSNs.

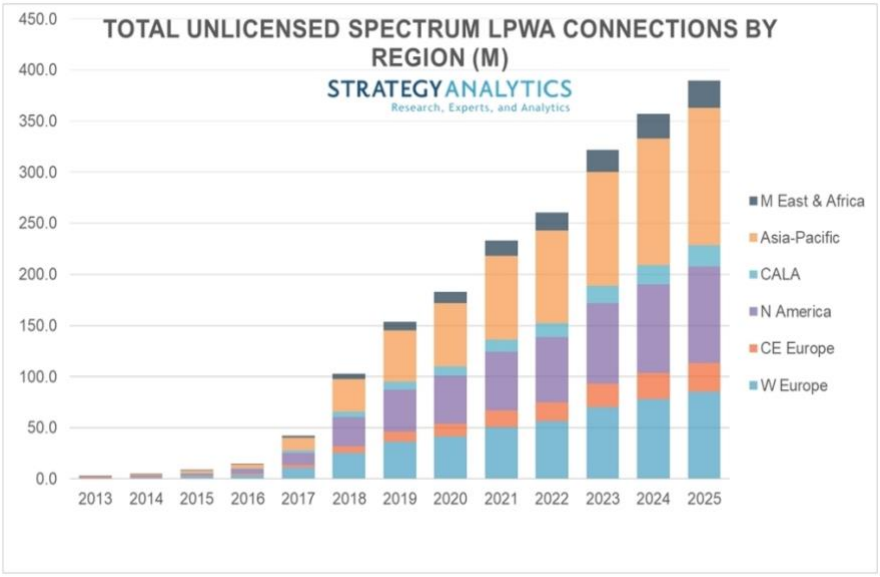


Figure 1.7 Number of IoT Low-Power Wide-Area Network (LPWAN) connections in the unlicensed frequency bands vs. year

Figure 1.8 illustrates this tradeoff, with only 43 of 179 ULP radio publications reporting their SIR performance, most of which have power consumption levels higher than 100's of micro-Watts, which solidifies the hypothesis that ULP receivers are susceptible to in-band interference.

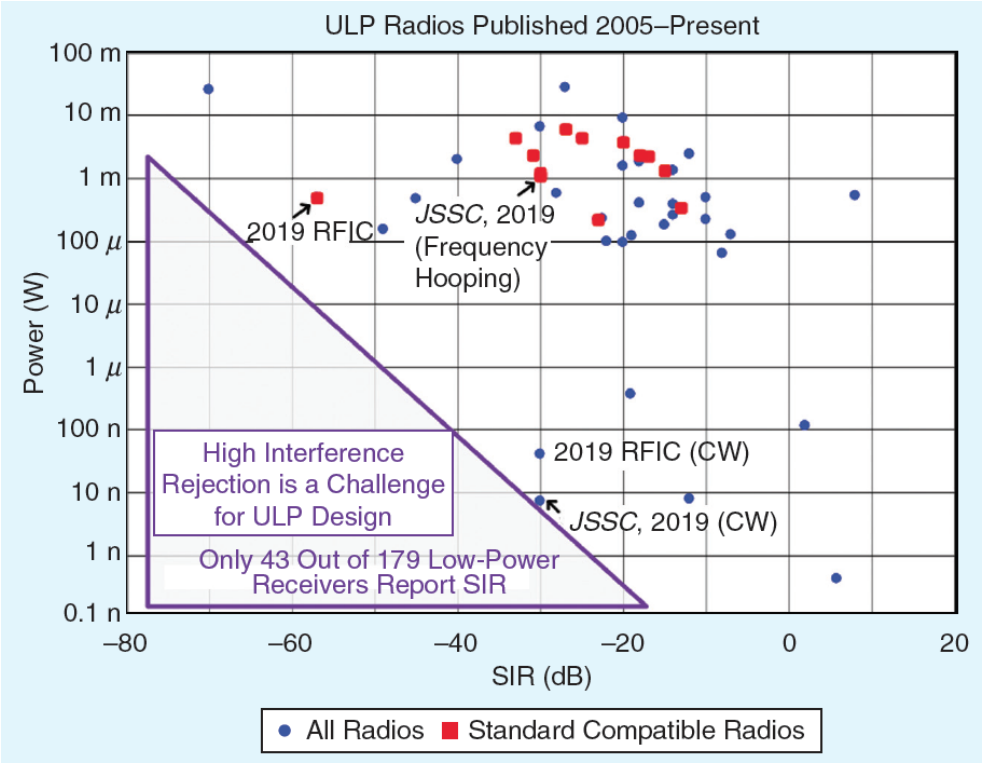


Figure 1.8 Blocker tolerance (SIR) in ULP radios vs power dissipation [5]

1.4.3 Form Factor

The modern wireless sensor system is made up of multiple components, including a microcontroller, power management, sensor, transceiver, timer/clock, battery, and antenna,

Figure 1.9. The components are almost always commercially available off-the-shelf ones that can be bought separately and arranged on a circuit board. While it has the advantage of being flexible for designers and having low cost, it does not resemble future sensor nodes' new class of computers. In most cases, the bulky battery occupies a large portion of the total volume and the radio antenna extends several centimeters outside the WSN body.

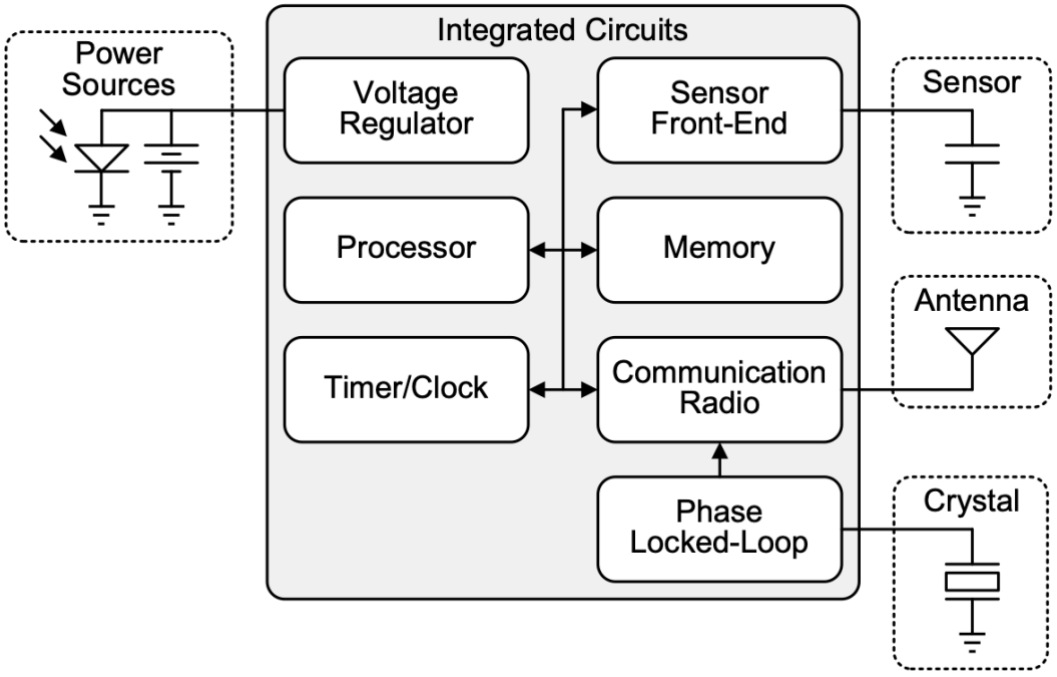


Figure 1.9 Block diagram of a typical WSN [7]

Therefore, these would translate into very large dimensions up to 10's of centimeters on at least one side. Considering these obstacles, the integration of the battery and antenna are two major challenges to achieving integrated cubic mm-scale wireless sensor nodes [8] [9]. Researchers at UC Berkeley introduced the idea of smart dust, also known as tiny form factor computers, in

early 2000 [10]. Since then, the IoT industry and the big data era took off throughout the world. Nevertheless, University of Michigan researchers have made a significant breakthrough in millimeter-scale computers during the last decade. Their studies focused on holistic and systematic investigations [11] [12] [13]. Resulting from these efforts is Michigan Micro Mote (M^3), the world's smallest computer, Figure 1.10.

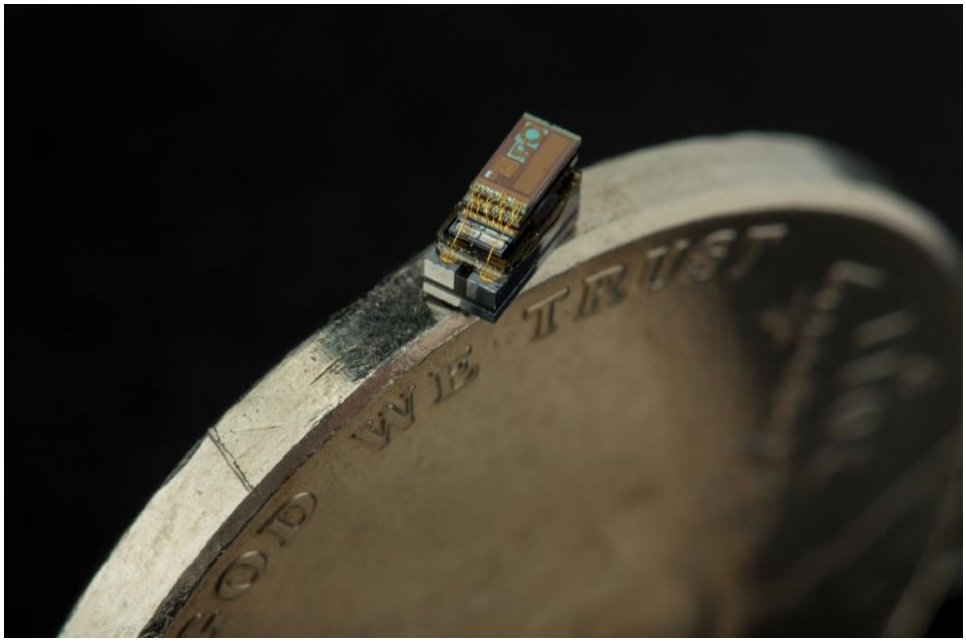


Figure 1.10 Michigan Micro-Mote: a stacked millimeter-scale computing platform

In addition to M^3, Other universities as well as research institutes have presented related research [14] [15]. There have been significant research efforts aimed at developing techniques for creating devices with such small form factors, like designing ultra-low-power, energy-efficient integrated circuits and systems, leveraging state-of-the-art semiconductor technologies

[16] [17] [18]. In contrast with the existing system-on-chip (SoC) design methodology currently used, the M^3 platform introduced new modular design concepts. It consists of separate chips (less than 3mm x 3mm in size) that each perform a specific function, e.g., processor, power management unit, solar cell, radio, etc. A platform of this kind has the advantage of being able to design each module into its own best-fit process node, as opposed to SoCs. As small as such WSNs are, wired communication is practically impossible. Therefore, RF and millimeter-wave layers for wireless sensing and communication are essential.

1.5 Solutions for Enhancing Performance in Energy-Restricted Radios

As discussed in the previous sections, there are design tradeoffs between power consumption and other key metrics of performance for a wireless receiver. The requirements for the low power wireless receivers can be achieved through different approaches and solutions, which can empower the extension of battery life and still maintain the ULP operation regime. These solutions are offered on three different levels: battery level, network level, and circuit level. Each of these levels will be discussed in more detail in the following sections.

1.5.1 Battery Level Solutions

One means of reducing the need for frequent battery maintenance in massive networks of WSNs with small form factors is enhancing the energy density in batteries. Battery technology, however, has progressed much more slowly in comparison to semiconductor technology over

the past few decades, as shown in Figure 1.11. It is striking that while energy density has increased only 4x over the span of 20 years, semiconductor technology has advanced 75x faster than battery technology over the same period. This trend is known as Snail's law, and refers to the relatively slow pace of technological progress in the battery industry [19].

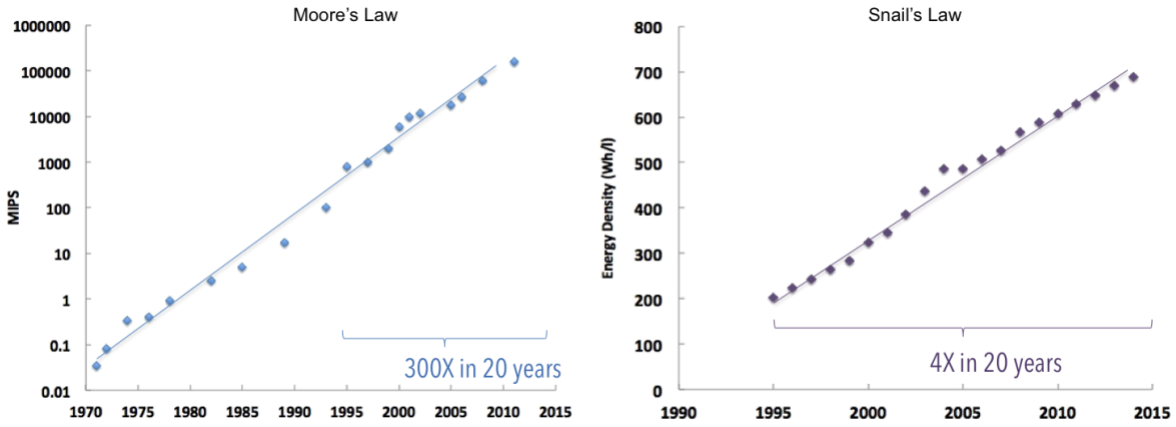


Figure 1.11 Semiconductor technology improvements vs battery energy density improvement over a 20-year time span [19]

Due to the lagging technology of batteries, energy sourcing is constrained in WSNs, presenting a significant challenge to the design of ultra-low-power wireless communication and sensing systems.

1.5.2 System Level Solutions

In light of the battery limitations, alternative solutions are needed more than ever for different aspects of a wireless system. A significant amount of innovation potential lies at the system level, in which a lot of design variables can be optimized in conjunction with the wireless transceiver, such as communication protocols, modulation schemes, bit-level and packet-level

duty cycling, leveraging ULP wakeup receivers, and so on, to obtain robust operation with the desired blocker tolerance and communication range while maintaining the ULP operation regime. In this dissertation, several novel system level solutions have been proposed and showcased to enhance the ULP receiver's performance.

1.5.3 Circuit Level Solutions

To ensure meeting the receiver specification requirements with minimal energy and hardware overhead, different approaches have been taken both on the block level and architecture level. For instance, *Q*-enhanced amplifiers have been adopted to achieve high gain amplifiers at RF frequency bands with minimal power consumption overhead [20]. Integrated RF circuit blocks such as Low Noise Amplifiers (LNAs) are co-designed with high-*Q* MEMS filters to obtain narrowband filtering at RF frequencies with sufficiently high RF amplification [21]. Other circuit level solutions such as leveraging integrated digital control loops have been proposed in the literature to enhance certain blocks' performance [22]. Moreover, co-designing antenna and RF/mm-wave blocks, especially at mm-wave frequency bands can offer significant improvements in area, loss, and operating efficiency in both transmitters and receivers [23] [24] [25].

A variety of wireless receiver architectures have been developed, as well. Among RF and millimeter wave circuit designers there are several architectures that are widely adopted:

1) **ED-First receivers:** The RF front-end features an all-passive design, which reduces the power of the RX to nanowatts. In such architectures, the RF envelope detector converts the incoming signals to DC, Figure 1.12. As a consequence of the high noise bandwidth,

an envelope detector in such an architecture typically limits the RX sensitivity to about -60dBm. A high-*Q* transformer can improve sensitivity by an additional ~20dB by providing passive gain and filtering at the front-end [26] (Figure 1.12). In addition, above 1GHz center frequency, the *Q* factor of the off-chip matching network may be limited as well. Within this architecture, the utilized integrated interference mitigation techniques are mostly limited to continuous wave (CW) interference signals which would translate into an additional DC offset for the comparator [22]. This assumption is not valid for all wireless channels, especially the populated unlicensed frequency bands where pulsed jammers with various modulation schemes are prevalent, therefore making them less effective in a real-world setting. Moreover, the operating RF frequency of this architecture is limited due to the relatively large shunt capacitance in the RF detectors.

2) **Mixer-First Receivers:** In another effort to improve power usage, the first RX stage is designated as the passive mixer stage rather than an active RF gain (LNA) [27] [28] (Figure 1.12). Due to the dominance of the first RX stage in RF performance, mixer-first radios have a higher noise figure (NF) despite offering an optimal power consumption, reducing their range and sensitivity. Besides, this architecture offers adequate selectivity levels with a sub-milliwatt power budget [29] [30]. For so-called mixer-first receivers, the local oscillator and buffers account for the largest power consumption block. Ring oscillators (ROs) can lower LO power especially in more advanced CMOS nodes compared to conventional LC oscillators [31]. The problem with ROs, however, is their

lower frequency stability. This makes radio design more challenging since significant performance degradation may occur with sensitivity and selectivity. As an alternative, an LC oscillator with an off-chip inductor can overcome the limited quality factor for on-chip inductors resulting in a significant power reduction by up to 75% compared with fully on-chip LC oscillators [32].

3) **LNA-First Receiver:** The demands on long-range applications usually require a sensitivity level better than -100dBm, which is the reason why RF gain blocks are usually used in wireless receivers, Figure 1.12. In these scenarios, the LNA-first topology is usually adopted. This architecture; however, demands high power consumption and in some cases suffers from lower selectivity compared to the mixer-first receivers. To reduce average power, bit-level duty cycling is also applied in LNA first radios [33], similar to RF ED based wake-up radios. In addition, lower supply voltages have been used to improve the power efficiency of LNAs [34].

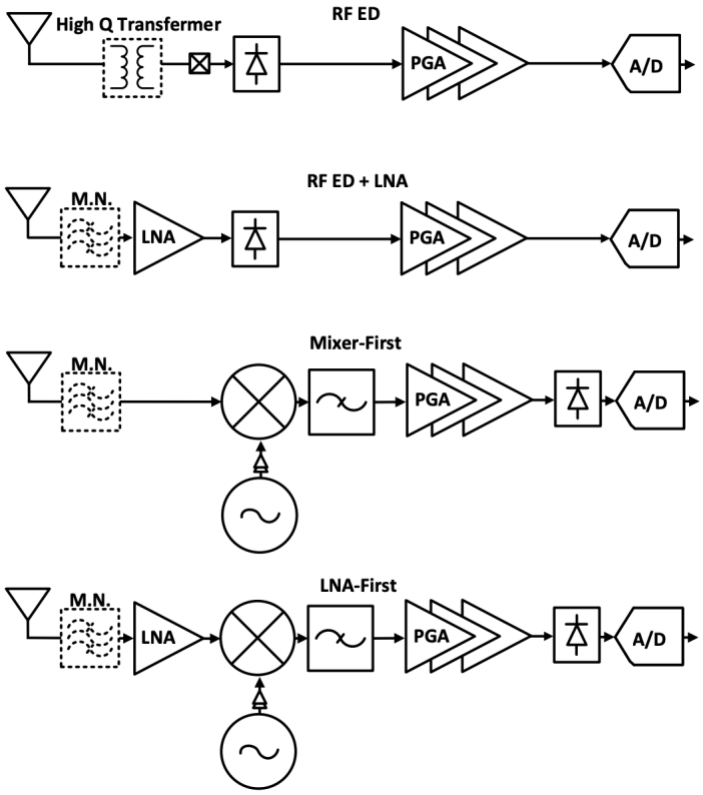


Figure 1.12 Low power radio architectures [5]

1.6 Contributions and Thesis Organization

The wireless transceiver is a key limiting factor in the development of the new class of computing devices as discussed in previous sections. The dissertation presents several approaches for overcoming these obstacles and contributes to development and miniaturization of energy-efficient and fully-integrated wireless systems for sensing and communication.

In Chapter 2, a 433MHz ULP receiver with high level of in-band and out-of-band blocker tolerance is presented. Several novelties were proposed and demonstrated in this research on

various aspects of a ULP wireless receiver designed to overcome interference challenges and communicate at a sensitivity level better than -100dBm. First, a novel dual-chirp OOK modulation scheme was proposed and used to alleviate the adverse effects of in-band blockers. Second, an energy-efficient *Q*-enhanced RF frontend was used to filter out of band interference. Third, a customized RF packet structure along with a novel sliding window chirp synchronization scheme was proposed and implemented for packet synchronization to ensure robust operation in the receiver. This receiver consumes 110µW, while achieving an SIR as high as -41dB for in-band blockers and sensitivity of -103dBm at 2.5kb/s. The receiver uses off-chip inductors for RF input matching as well as load impedance for the *Q*-enhanced RF amplifier.

In Chapter 3, a 900MHz chirp modulated mixer-first receiver is presented that leverages a novel chirped N-path filter at IF for enhanced receiver selectivity. The proposed receiver uses an LC oscillator leveraging an off-chip inductor for better phase noise performance and lower power consumption. Moreover, a chirped Miller N-path filter is proposed and designed at IF to ensure enhanced interference tolerance and lower in-band noise. This chip was designed and fabricated in a 65nm process and consumes 320µW power, while achieving -58dB SIR and -88dBm sensitivity at 5kb/s.

In Chapter 4, a variety of technologies for energy-efficient and high-precision ranging in energy-restricted mm-scale wireless sensor nodes are discussed and the system level requirements for hardware implementation of such ranging techniques are studied in depth.

In Chapter 5, a novel mm-scale PLL-less Frequency Modulated Continuous Wave (FMCW) radar transceiver is presented. The proposed transceiver leverages co-design between the transmitter high frequency blocks and the receiver's Digital Signal Processing (DSP) blocks, which are running at low clock frequencies, to eliminate the need for power-hungry RF blocks such as a chirp PLL to facilitate robust and low-power operation. Moreover, the transceiver chip utilizes on-chip antennas to minimize off-chip components and ensure mm-scale form factors. Finally, the RF front end blocks on both the transmitter and receiver are co-designed with the antennas in order to achieve maximal efficiency and minimize power consumption.

Chapter 2:

A 110μW 2.5kb/s -103dBm-Sensitivity Dual-Chirp Modulated ULP Receiver Achieving -41dB SIR

2.1 Introduction

Because of the growth of IoT applications which require long-range data transmission, LPWAN technologies have become increasingly popular over the recent years for a diverse set of applications, Figure 2.1. However, enabling communication ranges of up to tens of kilometers with ultra-low power wireless sensor nodes is a major challenge. Additionally, due to the rapid expansion of IoT devices in recent years, stricter requirements have been placed on IoT ULP radio receivers (RX) that can operate in an increasingly crowded spectrum while maintaining ultra-low-power (ULP) consumption, high sensitivities, and low cost. Prior ULP radios utilizing on-off keying (OOK) modulation with sub-μW power consumption offer good sensitivity, but are susceptible to in-band (IB) and out-of-band (OOB) interference and have high latency overhead [26].

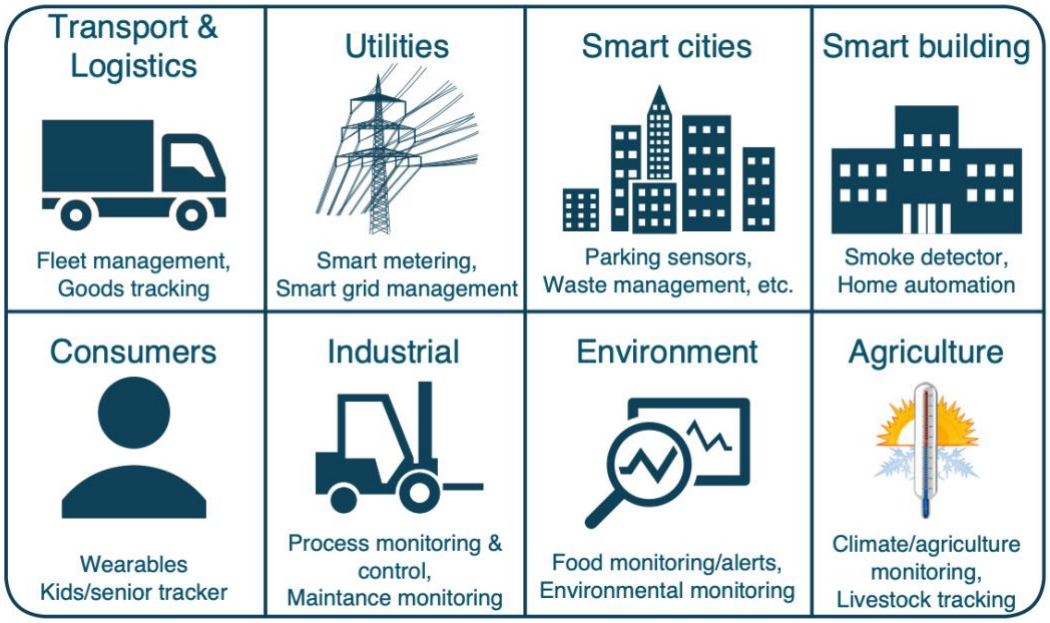


Figure 2.1 Massive IoT applications enabled by LPWANs [35]

As shown in Figure 2.2, high-*Q* off-chip MEMS resonators and envelope tracking loops can be leveraged to mitigate OOB blockers and continuous wave (CW) IB blockers [21] [36], but fail to reject IB pulsed blockers, which are known to be frequently encountered in Industrial, Scientific, and Medical (ISM) bands due to a broad variety of radio standards. Digital control loops have also been used to dynamically adjust the threshold voltage of the demodulator comparator to suppress CW blockers in ULP receivers modulated with OOK [22] [37]. However, this approach suffers from the relatively large loop response time and fails to mitigate amplitude modulated blocker signals at high data rates. Two-tone OOK modulation can alleviate OOB blockers [38], but struggles to address close IB blockers and transient pulsed interferences. The works in [36] and [39] achieve strong blocker rejection, but come at the cost of lower sensitivity and higher power consumption compared to other ULP RXs.

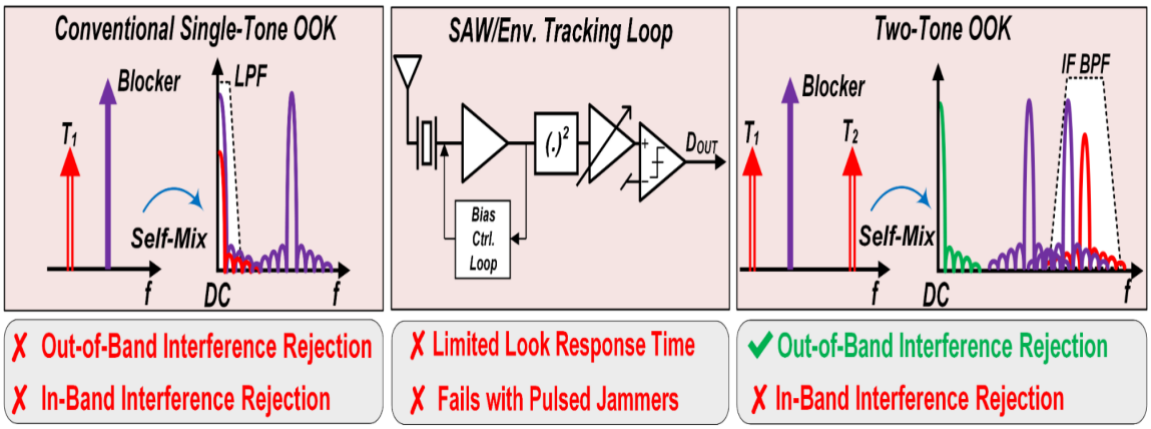


Figure 2.2 Interference rejection in prior at ULP receivers

To overcome these challenges and shortcomings of the existing solutions, we have proposed a novel dual-chirp OOK (DC-OOK) modulated ULP RX architecture that consistently achieves strong IB and OOB blocker rejection without sacrificing other important RX metrics of sensitivity, power, data rate, and cost.

2.2 Dual-Chirp OOK Modulation and Demodulation

Most ULP radios employ simple modulation schemes such as energy detection modulations to avoid significant hardware and power overhead associated with demodulation. Modulation schemes that use energy-detection, such as single-tone or two-tone On-Off-Keying (OOK) and Frequency Shift Keying (FSK), are widely adopted in ULP radios as they are energy-efficient. Modulation schemes with such performance characteristics have low power consumption along with good RX sensitivity performance, but are subject to significant RX performance degradation if in-band or out-of-band

interference is present, Figure 2.2. Furthermore, local oscillators and their buffers are one of the major consumers of the power in the RF receivers. One of the techniques to eliminate the need for power hungry RF oscillators is employing two-tone energy detection modulations such as two-tone OOK and two tone FSK [40] [38], which offer low power consumption along with enhanced channel selectivity compared to their single-tone counterparts.

Spread spectrum modulation schemes such as Code Division Multiple Access (CDMA) and chirp modulation, which are well known and widely adopted in commercial applications such as cellular and LoRa LPWAN radios, take advantage of the spreading and de-spreading principle during modulation and demodulation to enhance immunity to narrowband interference [41] [42], Figure 2.3.

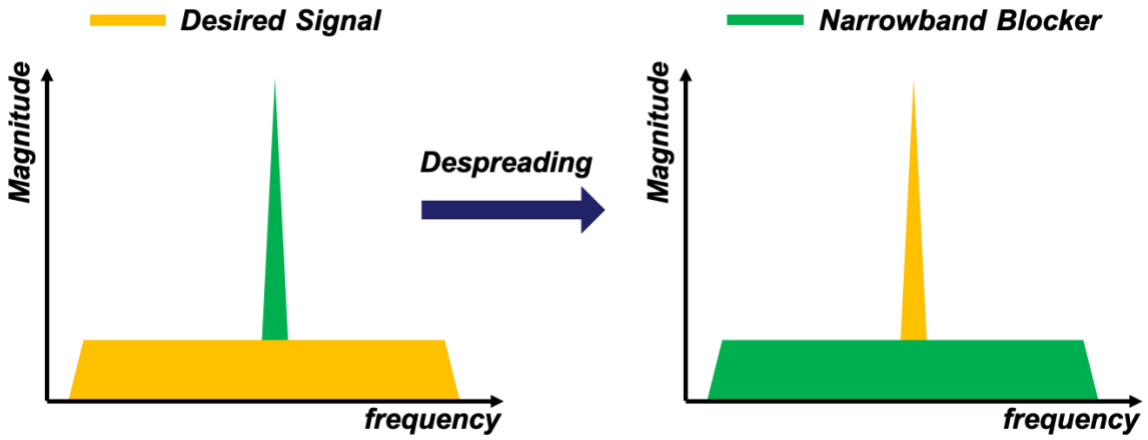


Figure 2.3 Spread spectrum communication in the presence of a narrowband blocker signal

In this work, we have presented a novel modulation scheme that simultaneously offers the benefits of spread spectrum and two-tone modulations schemes, with minimal power and

hardware implementation overhead requirements. The proposed modulation is OOK-based and a ‘1’ symbol consists of two RF chirp signals at two different start frequencies and ramp rates, Figure 2.4. After self-mixing and band pass filtering (BPF) the incoming dual-chirp RF message, a single low-frequency chirp at IF is generated due to the intermodulation of the dual chirps passing through the squaring operation of a self-mixer, Figure 2.4. The IF chirp frequency is therefore the difference between the two RF chirp signal frequencies. After band pass filtering, the encoded signal is seen as a chirp signal (symbol ‘1’) or a zero-energy signal (symbol ‘0’).

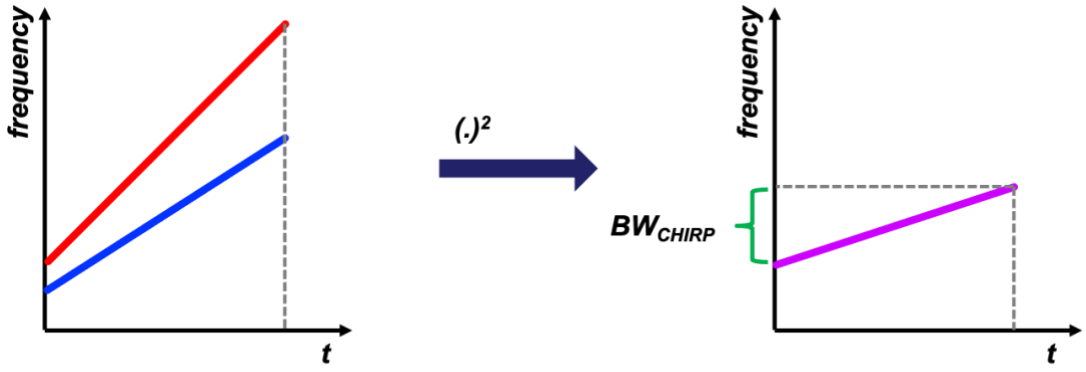


Figure 2.4 Basic illustration of a '1' symbol in the proposed DC-OOK modulation at RF (left) and IF (right)

In order for the proposed DC-OOK modulation to work robustly, a reliable and energy efficient demodulation scheme is required on the receiving end. Prior art LoRA LPWAN receivers that use chirp spread spectrum modulation have traditionally implemented the demodulator after the Analog to Digital Converter (ADC) in the digital domain, Figure 2.5

[40]. This method has a few benefits including 1) allowing for the implementation of sharp FIR filters in the digital domain to improve the Signal to Noise Ratio (SNR); and 2) incorporating an FFT engine into the DSP to detect the message after chirp de-spreading to improve noise and interference immunity. However, the conventional demodulator designs required high speed and high-resolution ADCs along with complex DSP algorithms and implementations, causing the receiver to consume substantially higher levels of power.

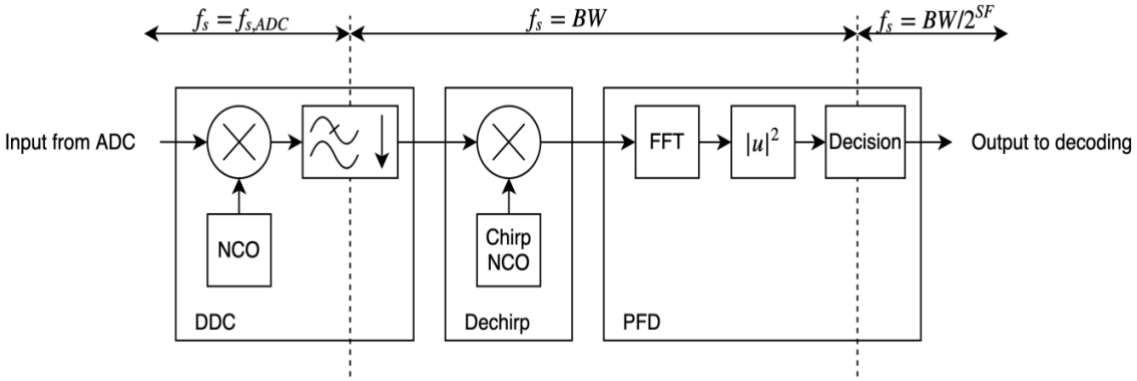


Figure 2.5 Conventional LoRa demodulator block diagram [43]

Presented in this work is a simple yet effective chirp demodulation scheme in the analog domain that offers robust demodulation of incoming signals without incurring significant hardware complexity and power consumption. The proposed scheme correlates the incoming low-frequency chirp message with a local low frequency chirp signal–that is generated by a chirp Phase Locked Loop (PLL)–in the analog domain and generates an OOK-modulated signal at the output, whose demodulation is much easier and energy-efficient than the conventional digital domain chirp demodulators. The operating principle of the proposed analog correlation-based chirp demodulation is depicted in the frequency domain in Figure 2.6.

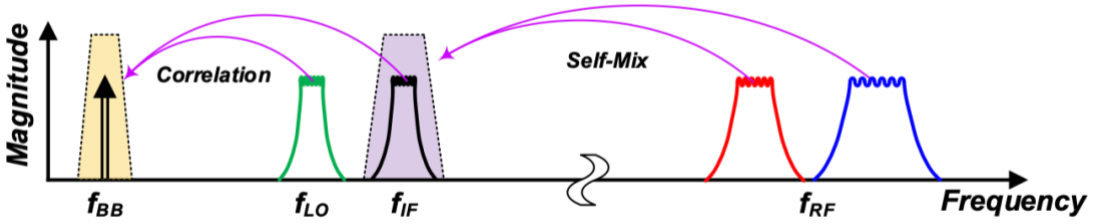


Figure 2.6 Frequency domain demonstration of the proposed analog correlation-based chirp demodulation

2.3 Receiver Architecture

A block diagram of the proposed receiver architecture is shown in Figure 2.7. In order to achieve low-power operation and long range, an LNA-first architecture followed by a self-mixer stage has been adopted, obviating the need for a power-hungry Local Oscillator (LO).

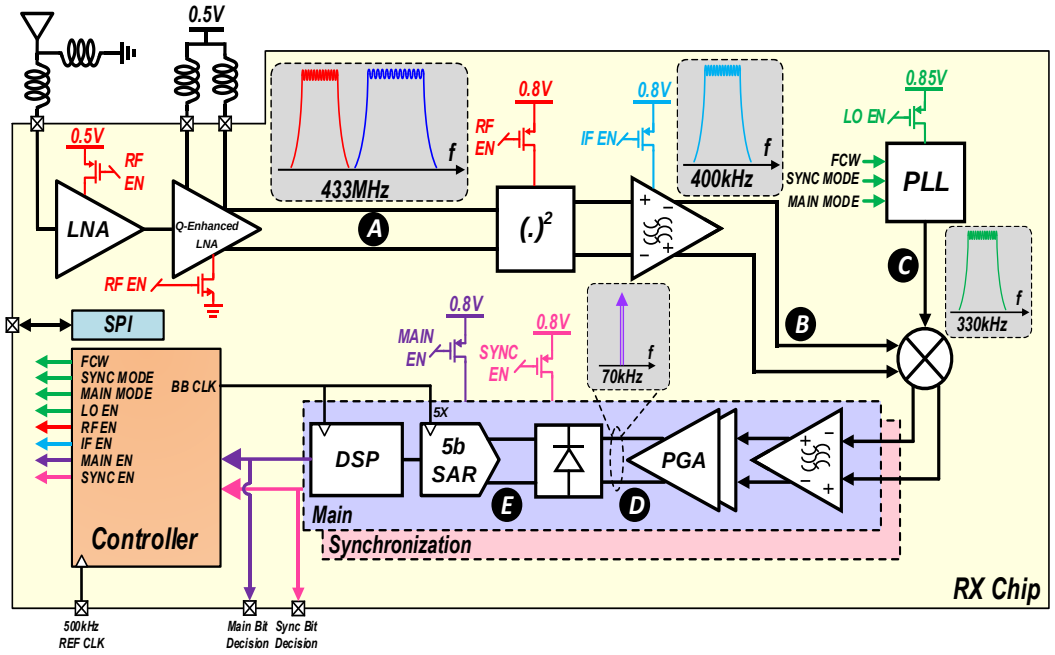


Figure 2.7 Block diagram of the proposed receiver

Furthermore, the waveforms at different points of the receiver are depicted in Figure 2.8. As discussed in the previous section, the incoming DC-OOK RF signal consists of two RF chirp signals ramping at two different chirp rates. The incoming DC-OOK RF signal is amplified by a high-gain and low-noise RFFE to maximize the self-mixer conversion gain while rejecting OOB interferers, point A Figure 2.8.

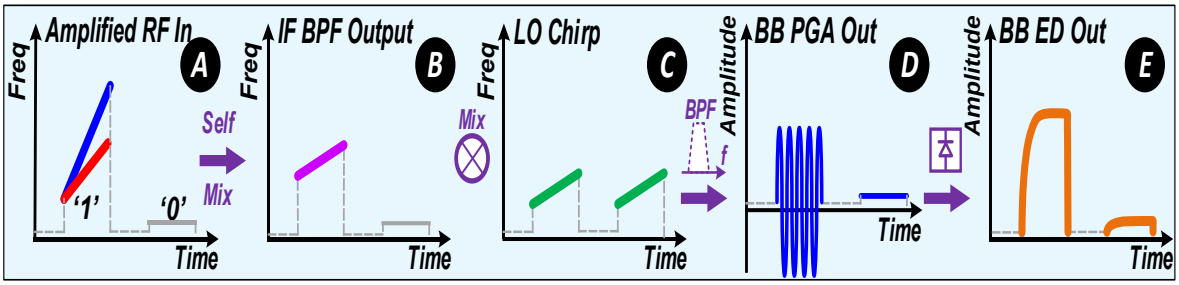


Figure 2.8 Time domain waveform at the output of each RX stage

The RF signal is then down-converted by an active self-mixer stage, which generates a single low-frequency chirp at the IF frequency band due to the intermodulation of the dual chirps passing through the squaring operation of the self-mixer. It follows then that the IF chirp frequency is determined by the difference between the two RF chirp frequencies. After band pass filtering, the encoded signal appears as a chirp signal (symbol '1') or a zero-energy signal (symbol '0') (point B), Figure 2.8. In the next step, in order to demodulate the chirp signal, the IF chirp is correlated with a synchronized LO chirp (point C) with a slope identical to the incoming signal IF chirp, which generates a tone signal at the baseband center frequency and a chirp signal at high frequency. The mixer output then passes through another second order band pass filter stage and the programmable gain amplifiers (point D). Next,

the output is fed to an envelope detector (ED) to extract amplitude information (point E) followed by a 5b SAR ADC with 5x oversampling ratio followed by a majority voting digital demodulator, which improves the baseband SNR requirement for a given BER by 4dB.

In addition, as discussed in the previous sections, the proposed receiver comes with enhanced immunity to IB interference while retaining a strong rejection of OOB interference. This is achieved by the spread spectrum nature of the dual-chirp modulation along with analog chirp correlation at IF which suppresses the blocker signals present in the desired channel by spreading them in the frequency spectrum. The operation of the receiver in presence of narrowband blocker signals is demonstrated in Figure 2.9.

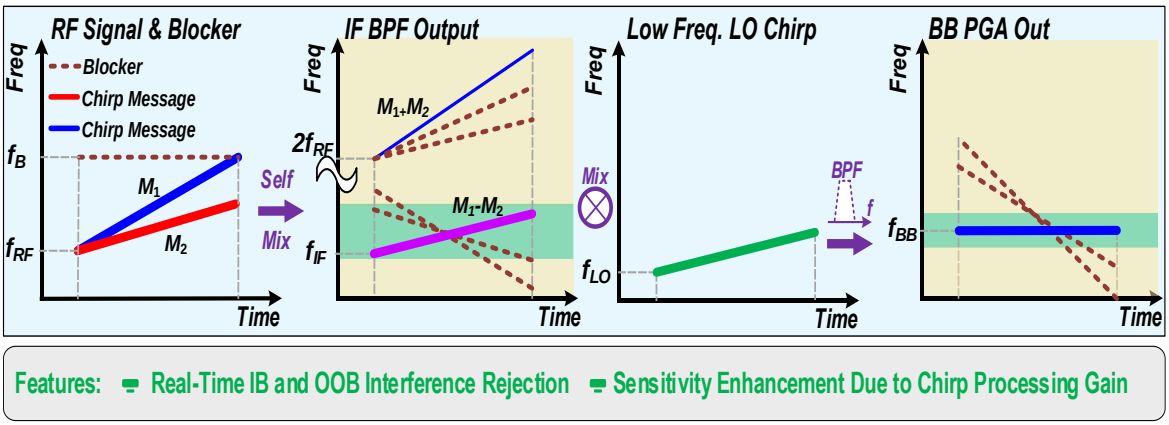


Figure 2.9 The concept of spread-spectrum IB interference mitigation in the proposed RX

2.4 Packet Structure and Synchronization

To guarantee reliable operation of the ULP RX, the RF packet and the LO chirp timing must be synchronized. To ensure robustness of packet synchronization, two different efforts were made on each of the transmitting and receiving sides. First, on the transmitting side, the RF

packet structure is carefully designed to assist the ULP receiver in synchronizing the LO with the incoming RF message and demodulating the dual-chirp modulated packet data. An illustration of the DC-OOK modulated packet at IF is shown in Figure 2.10. The received packet is composed of three different frames: 1) a 20-bit packet synchronization frame, which enables timing alignment between the incoming RF packet and the ULP receiver; 2) a 4-bit preamble detection frame for detecting the start of the main data frame in the packet; 3) a packet data frame (payload) with a programmable length.

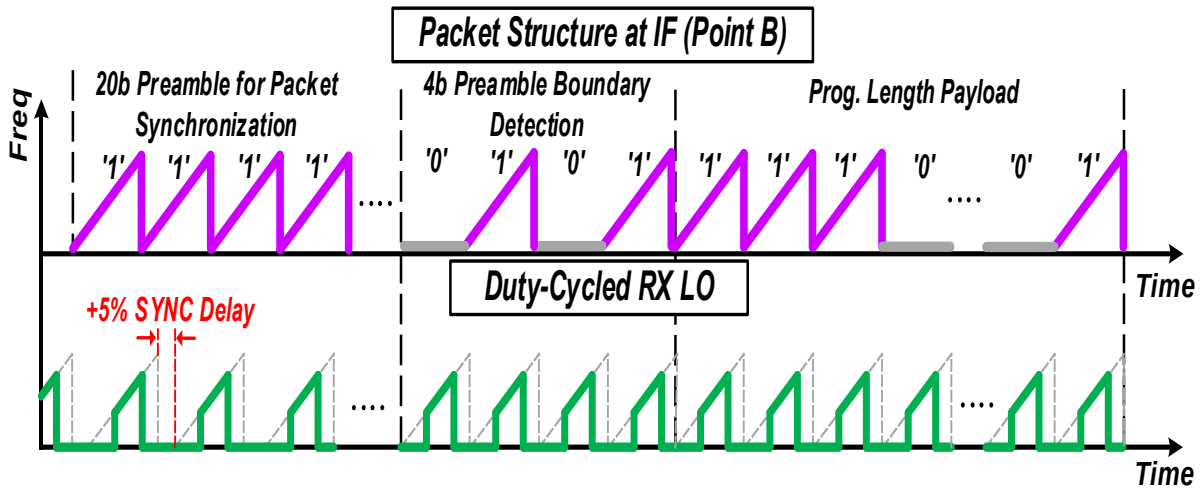


Figure 2.10 Downconverted RF packet structure

Second, the ULP receiver synchronizes and receives the payload data from the RF packet with the assistance of an on-chip finite state machine (FSM) which one of its responsibilities is controlling the RF packet-level operation and synchronization. The ULP RX packet level operation is composed of two different modes: the packet synchronization (SYNC) mode and the Main RX mode, respectively. By default, the duty-cycled RX is operating in SYNC

mode that searches for the RF synchronization frame by enabling the SYNC baseband path and disabling the Main baseband path along with generating a sliding LO chirp with a programmable delay of 5% per symbol, as shown at the bottom of Figure 2.10. As soon as the SYNC demodulator detects a '1' symbol from the incoming 20-bit packet SYNC frame, the SYNC demodulator handshakes with the FSM to switch the operation mode from the SYNC mode to the Main RX mode, where the Main baseband path is enabled and SYNC baseband path is turned off. The ULP RX determines the start of the main data frame by detecting a preamble sequence. After successful preamble detection, the FSM moves to data reception mode to receive a data payload with programmable-length. As soon as the number of data reception cycles reaches its maximum data length, the FSM forces the ULP RX to go back to the default operation (SYNC) mode. A flow chart diagram of the operation of the FSM during the SYNC and Main modes is shown in Figure 2.11.

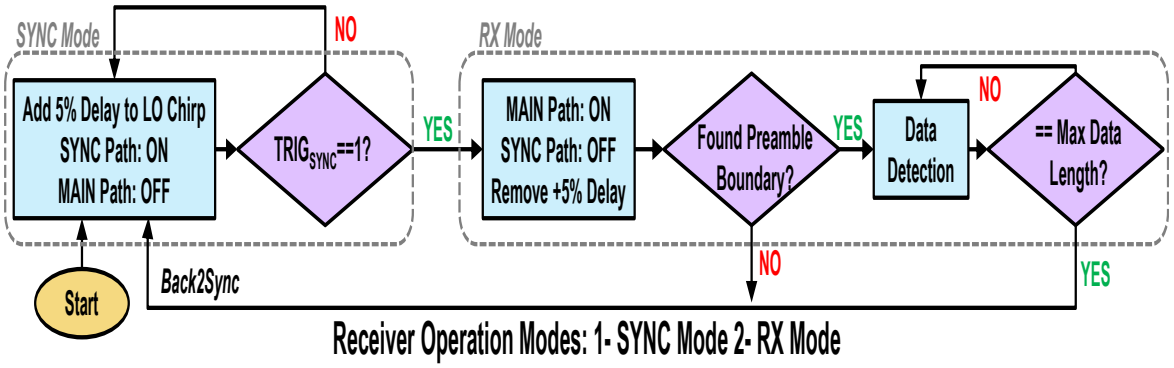


Figure 2.11 Flow chart diagram of the FSM operation

The effect of LO and RF symbol offset on the symbol SNR has been simulated. As expected, the simulation result indicates that there is a direct tradeoff between the symbol energy

degradation and the symbol offset, Figure 2.12. Thus, the length of the preamble sequence for packet synchronization was chosen as a result of optimization between receiver latency and the symbol energy (SNR). Based on simulation results, a 5% symbol offset during the synchronization phase guarantees SNR degradation smaller than 4.5dB, Figure 2.12.

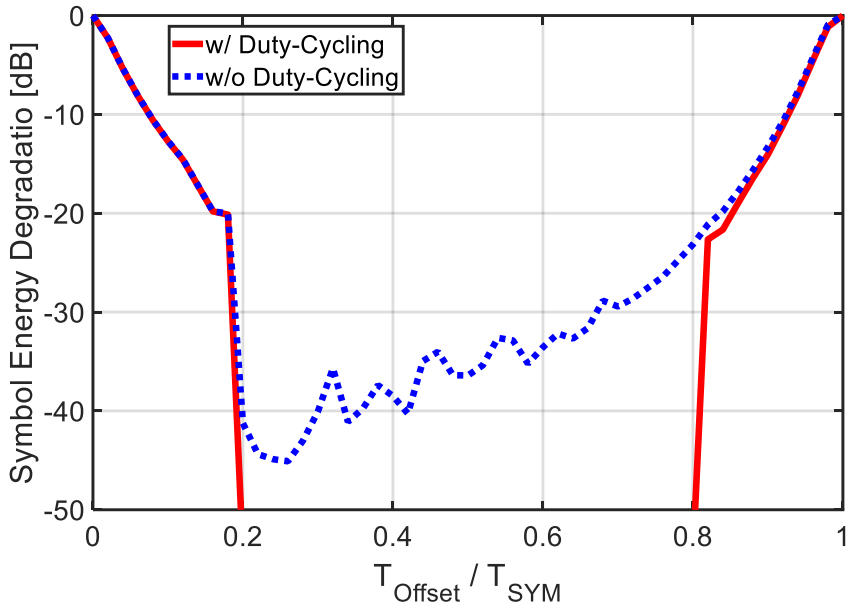


Figure 2.12 Simulated DC-OOK modulated symbol energy degradation vs normalized symbol offset with and without duty-cycling

2.5 FSM Timing and Duty-Cycling

As discussed in the previous section, one of the duties of the integrated FSM is controlling the ULP RX's operation mode by handshaking with the SYNC and Main receive chains. In addition, another responsibility of the integrated FSM is controlling the receiver data rate as well as enhancing the energy-efficiency of the ULP RX by performing bit-level duty-cycling. A block diagram of the designed FSM including the baseband demodulators

for the SYNC and Main paths is shown in Figure 2.13. The FSM is designed with a programmable symbol period and duty-cycling ratio. To avoid high latency in the receiver while maintaining low-power operation, a symbol rate of 2.5kb/s (T_{SYM}=400µs) with 50% duty cycle was chosen.

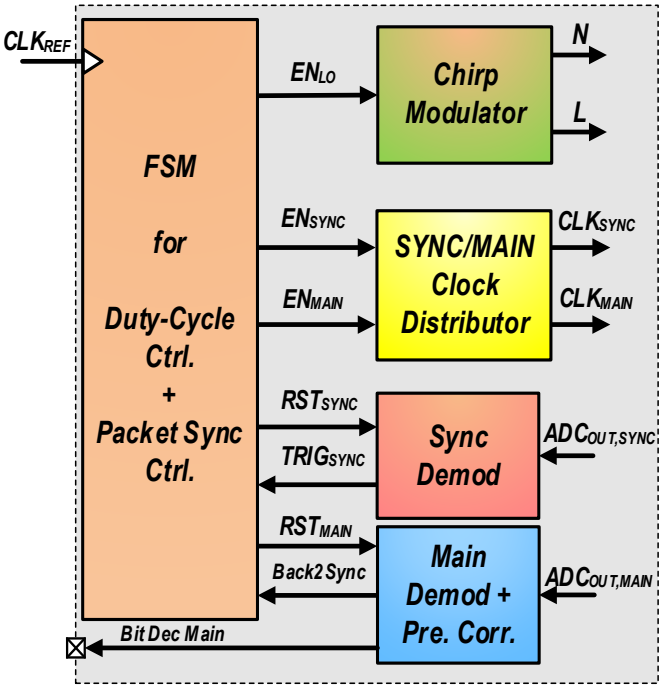


Figure 2.13 FSM block diagram

In addition, to achieve high speed operation with minimal power overhead, the FSM was designed to insert an adjustable delay between the enable signals for various blocks. This ensures sufficient startup time for the low frequency and slow blocks such as baseband and IF chain blocks and bias circuits, while avoiding unnecessary active time for high speed and power-hungry blocks such as RF amplifiers. A timing diagram of the bit-level duty-cycling along with the breakdown of the power consumption in the ULP RX is shown in Figure 2.14.

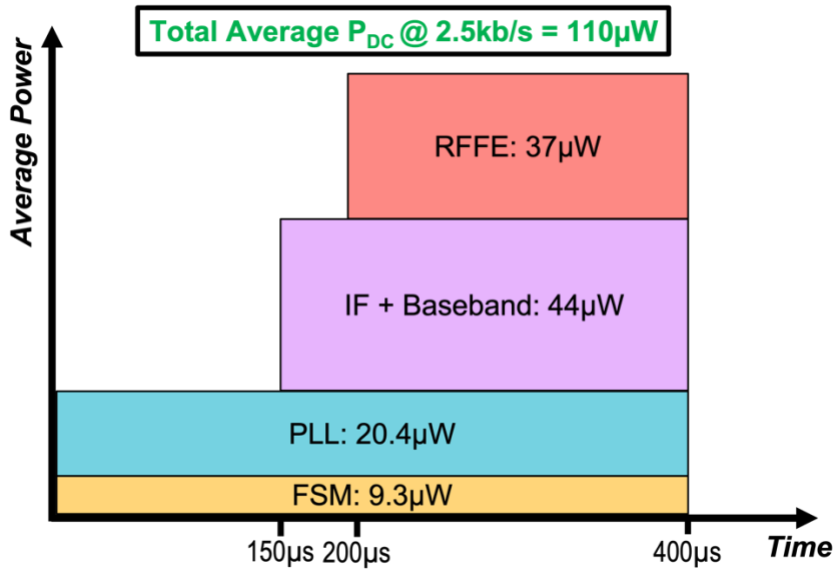


Figure 2.14 Power breakdown of the duty-cycled ULP RX

2.6 Low Power Circuit Implementation

2.6.1 RF Frontend

In order to obtain sensitivity levels better than -100dBm, adoption of high-gain and low noise RF amplifiers is inevitable. Moreover, since an LO-free architecture has been utilized for power saving, sufficient RF gain before the self-mixer stage is vital for optimal noise performance and conversion gain, as the receiver noise figure quadratically depends on the amplitude of the RF signal going into the self-mixer. Based on simulation results, an RF gain higher than 50dB is required for a sensitivity better than -100dBm, which can be challenging to achieve at RF frequencies. Moreover, conventional integrated RF amplifier solutions suffer from low passband *Q* and thus fail to suppress OOB blockers sufficiently. In order to deliver high RF gain along with narrow RF bandwidth in the ULP RX, two different steps

were taken. 1) off-chip inductors were utilized due to their inherently higher *Q* compared to their on-chip counterparts; and 2) a *Q*-enhanced single-to-differential LNA stage was adopted in the RF chain, Figure 2.15. Using the *Q*-enhanced LNA as the second stage in addition to a current-reused first stage LNA guarantees low input noise and sufficient RF gain at the 433MHz RF frequency.

As part of designing receivers for high sensitivity levels, it is necessary to meet strict noise figure requirements, which also mandates higher current consumption in the receiver RF blocks. To mitigate this challenge, a low voltage RF frontend has been developed to substantially reduce the ULP RX power consumption. The RF frontend operates on a 0.5V, while drawing 148µA active current based on measurements. According to the simulation results, the RF amplifier chain provides an adjustable gain of 30dB-60dB.

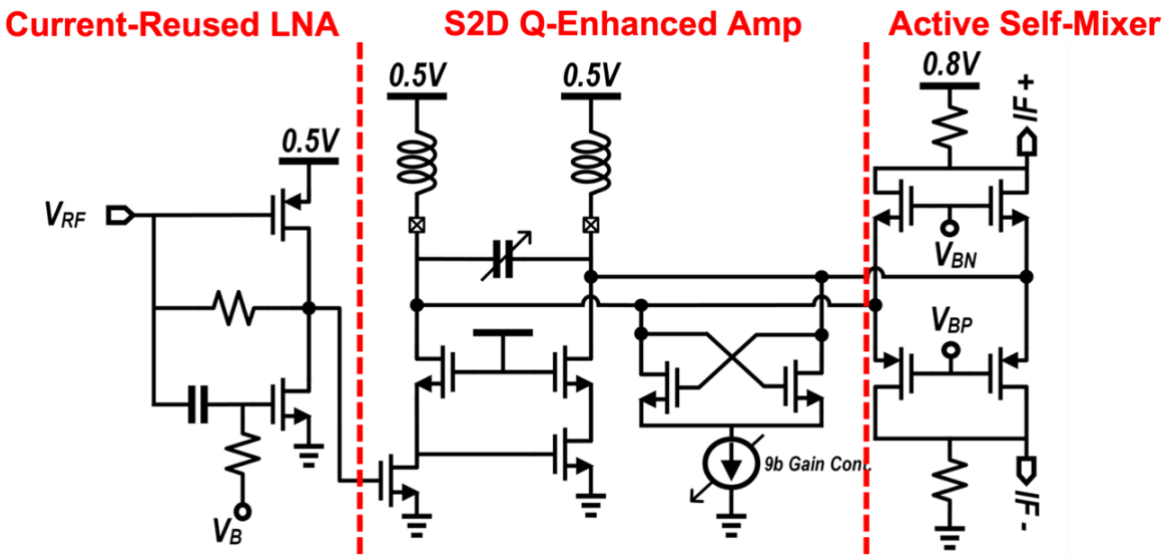


Figure 2.15 Schematic diagram of the designed RF frontend, AC-coupling caps and bias circuits are not shown for simplicity

In addition, in order to down-convert the incoming dual-chirp modulated RF signal to a differential IF signal at 400kHz center frequency, a current reused active self-mixer was designed, operating on a 0.8V supply with 5µA active current, Figure 2.15.

2.6.2 IF and Baseband

The IF signal is amplified using a low noise Programmable Gain Amplifier (PGA) and is then bandpass filtered using a second order active-RC filter centered around 400kHz. The schematic diagram of the PGA and the bandpass filter is shown in Figure 2.16 and Figure 2.17, respectively.

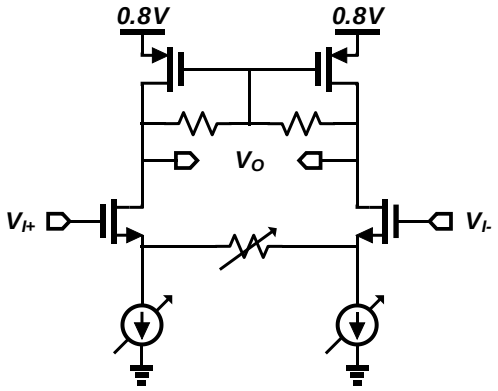


Figure 2.16 IF and baseband PGA stage

The IF signal is correlated with the chirp signal that is generated by a low frequency and energy-efficient analog fractional-N PLL through a double balanced passive mixer. The resulting baseband signal is a tone that passes through a second order active-RC biquad bandpass filter centered around 70kHz, similar to that of the IF. The baseband signal is then

amplified by two PGA stages and the amplitude information is extracted from the baseband signal using a 14-stage differential passive envelope detector (ED) [44], Figure 2.18.

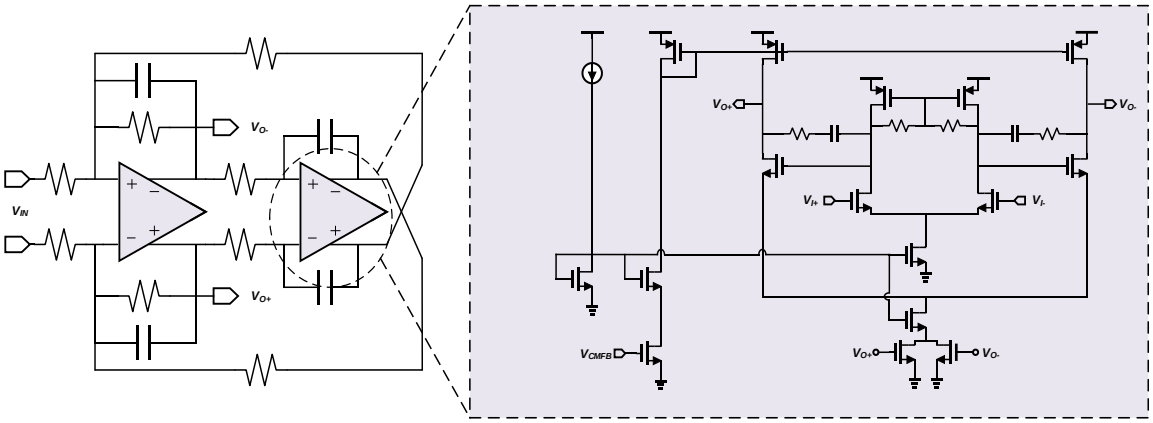


Figure 2.17 IF/baseband second order bandpass biquad filter and the designed OpAmp schematic

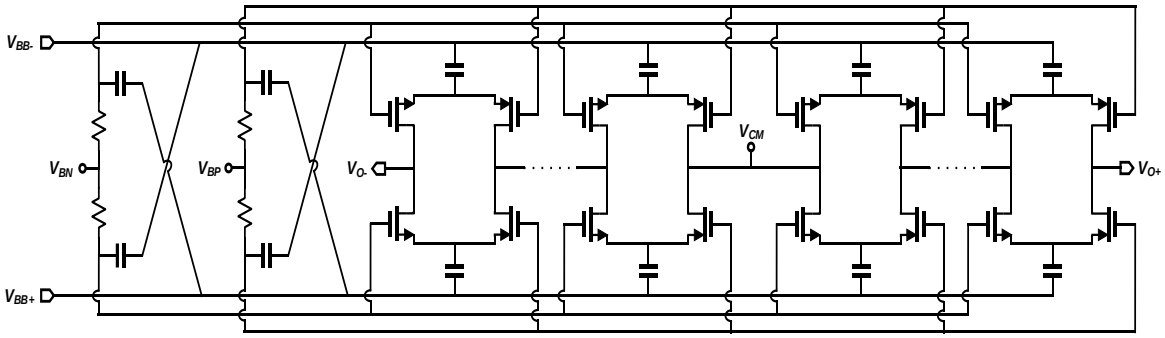


Figure 2.18 Fully differential 14-stage IF passive ED schematic diagram

Followed by the baseband is a 5-bit synchronous Successive Approximation Register (SAR) Analog to Digital Converter (ADC) whose clock is generated by the FSM and quantizes the incoming demodulated baseband data. Moreover, to enhance the baseband data SNR, a digital integrator along with a digital comparator with an adjustable threshold is employed in the baseband demodulator, Figure 2.19, to decide the incoming symbol's value.

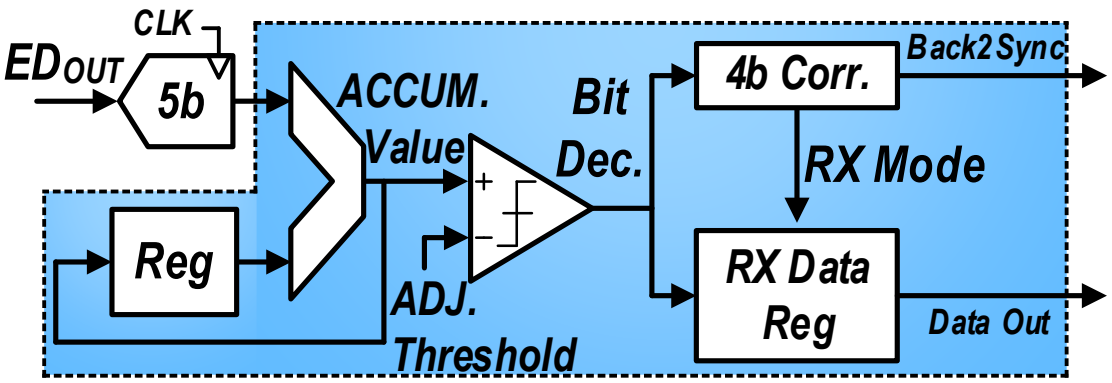


Figure 2.19 Block diagram of the baseband demodulator DSP

2.6.3 Chirp PLL

In order to demodulate the incoming chirp signal in the analog domain, a smooth low-frequency chirp signal is required. For this purpose, an analog fractional-N PLL with a reference frequency of 500kHz is designed, Figure 2.20. In order to achieve a smooth chirp and reduce the dithering effect, the PLL was designed at a higher frequency with larger N (4MHz - 8MHz) and its output frequency was divided (divide ratio = 14) to generate the desired local chirp signal. The PLL uses a 5-stage ring Voltage Controlled Oscillator (VCO) and a second order loop filter for smoothing the VCO control voltage. The PLL was duty-cycled to have a 50% (200µs) pre-charge time for settling and the rest of the symbol period (200µs) ramp time. Based on measurements, the PLL consumes 24µA active current from a 0.8V supply.

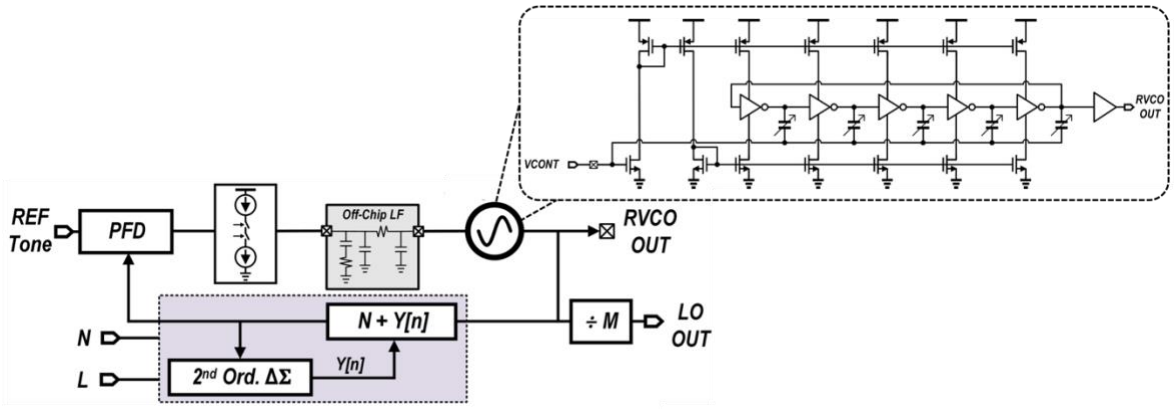


Figure 2.20 Chirp PLL block diagram

The chirped LO will have some deviation from an ideal linear chirp mostly due to the dithering in the fractional-N PLL, Figure 2.21, which can potentially affect the baseband signal's SNR and thus receiver's sensitivity. To ensure minimal baseband SNR degradation, the effect of chirp frequency deviation was characterized in simulation, Figure 2.21. Based on the simulation result, Δf_{RMS}<15kHz will guarantee symbol energy reduction smaller than 2dB. To achieve this spec, a programmable divider was employed after the PLL output to reduce the dithering effect stemming from the $\Delta\sum$ modulator.

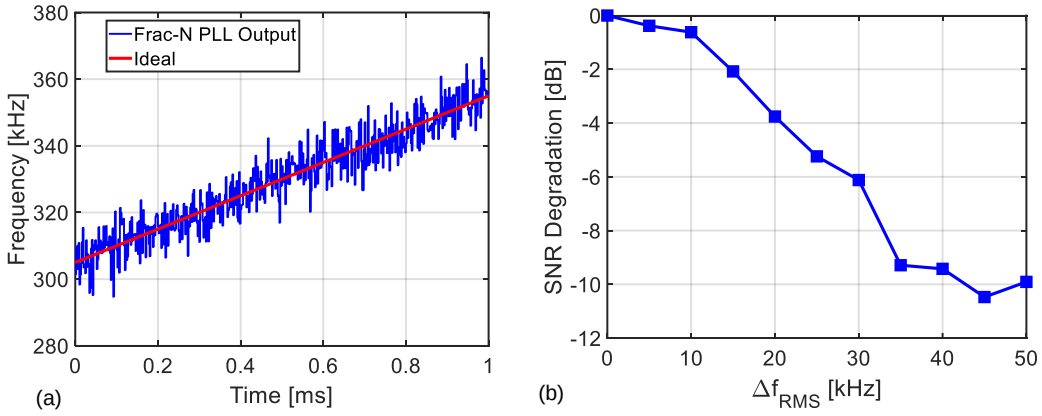


Figure 2.21 (a) Simulated LO chirp with frac-N PLL dithering; and (b) simulated effect of RMS frequency deviation on symbol energy

2.7 Measurement Results

The chip was fabricated in a 28nm CMOS process, Figure 2.22, and consumes 110µW at 2.5kb/s data rate. The measured input reflection coefficient of the ULP RX is plotted in Figure 2.23. Figure 2.24 demonstrates the measured and estimated PN of the PLL before and after the frequency divider, along with the transient plot of the chirp PLL output frequency with data-rate of 2.5kb/s and 50% duty cycling.

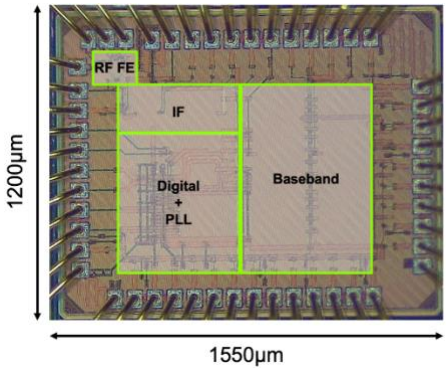


Figure 2.22 Die micrograph

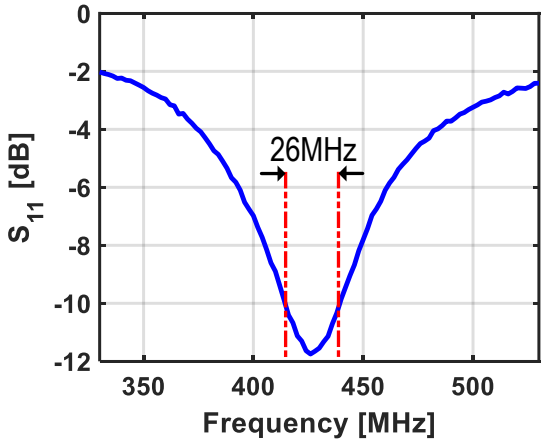


Figure 2.23 Measured input reflection coefficient

To demonstrate flexible operation of the chip for achieving high levels of blocker tolerance and high sensitivity, the chip was configured and measured for two different modes of

high-sensitivity and high-SIR. The measured RX sensitivity for BER<10^{-3} with 50% duty-cycling is -103dBm for the high-sensitivity configuration, Figure 2.25. The RX's blocker rejection is measured in the presence of a 1.6kb/s OOK modulated IB and OOB blocker signals at variable frequency offsets, as presented in Figure 2.26.

In this configuration, the RX achieves -19.2dB SIR for an OOK blocker with 1MHz offset, with the RF input power set 3dB higher than the RX sensitivity. The proposed RX can flexibly operate in different configurations for optimal sensitivity or blocker tolerance by adjusting the RF chain amplifiers. When the RX is configured for high interference rejection, an SIR of -20dB at 500kHz offset for the same blocker with sensitivity of -92dBm can be achieved, Figure 2.26.

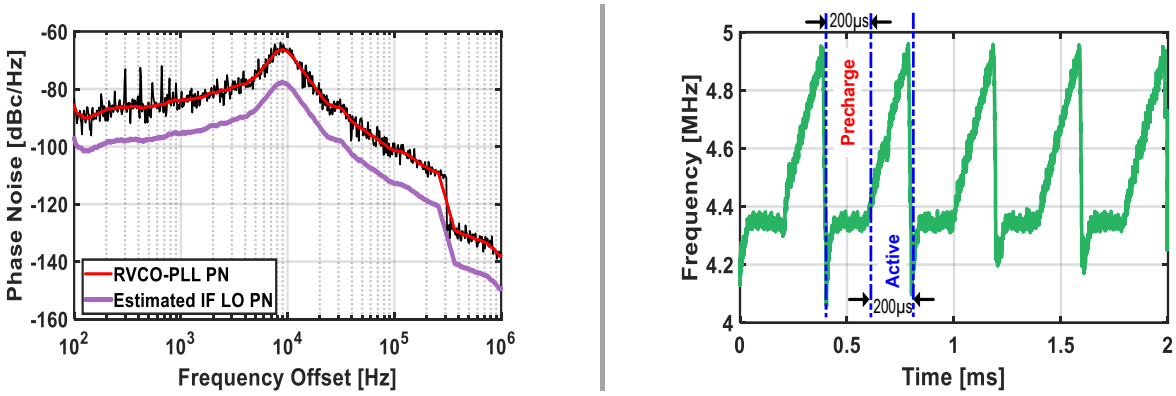


Figure 2.24 Measured and estimated PLL PN (left) and chirp PLL output frequency vs time (right)

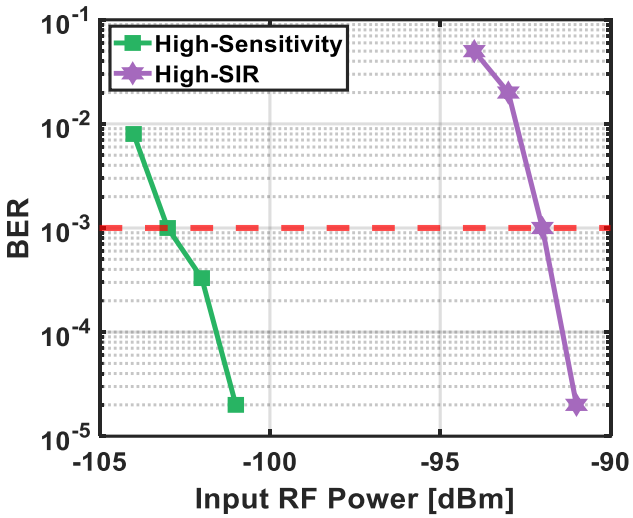


Figure 2.25 Measured RX sensitivity for the high-sensitivity and high-SIR modes

In addition, transient operation of the ULP RX during chirp packet synchronization and demodulation is captured and exhibited Figure 2.27, with RF input power 3dB higher than the RX sensitivity level.

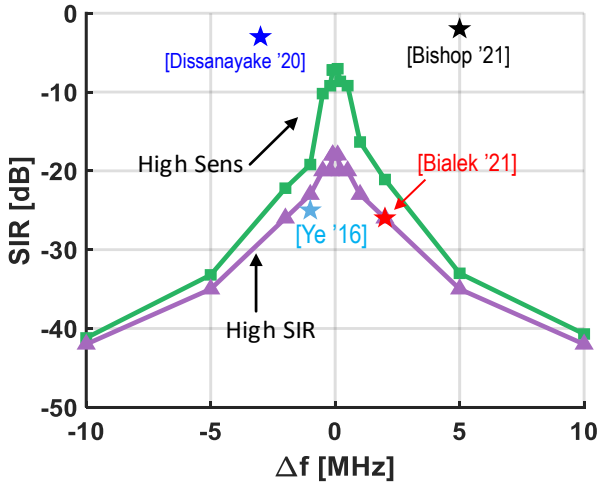


Figure 2.26 Measured SIR of the ULP RX in high-sensitivity and high-SIR modes

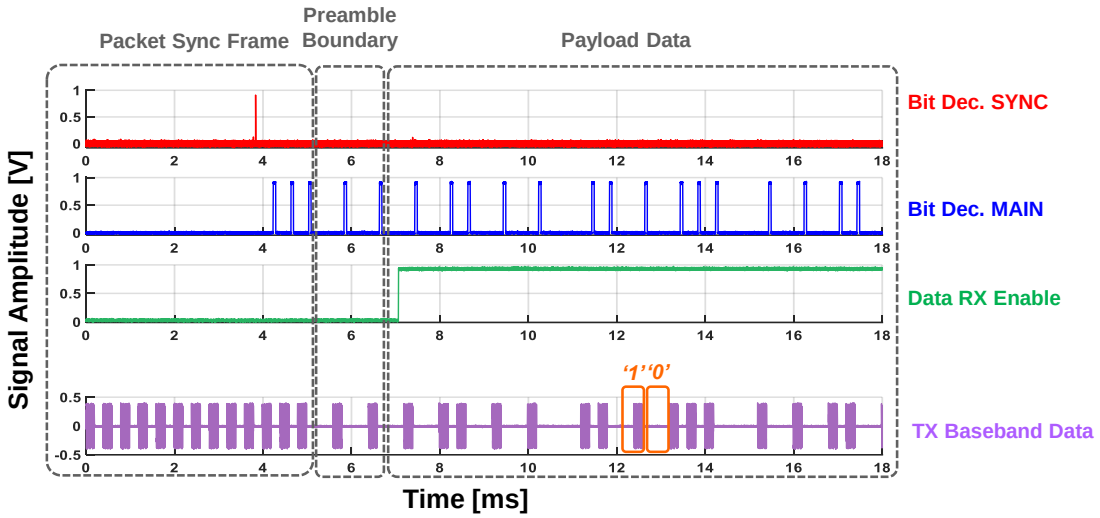


Figure 2.27 Transient operation of the ULP RX during packet synchronization and demodulation

2.8 Conclusion

This is compared with the state of the art in Table 2.1. The DC-OOK modulation allows this ULP RX to handle up to 20dBc IB blockers as close as 200kHz, while rejecting OOB blockers (≥5MHz) as high as 41dBc.

Table 2.1 Performance comparison with state-of-the-art.

	This Work		Bialek ISSCC '21 [5]	Bishop ISSCC '21	Mangal ISSCC '19 [1]	Moody VLSI '19	Ye ISSCC '16 [2]	Dissanayake VLSI '20 [4]
CMOS Process	28nm		65nm	65nm	130nm	65nm	65nm	65nm
Carrier Frequency	433MHz		0.75GHz–1GHz	2.4GHz	434.4MHz	428.3MHz	915MHz	434MHz
Sensitivity	–103dBm[2]	–92dBm[2]	–86dBm[2]	–91.5dBm[1]	–79.1dBm[1]	–106dBm[1]	–70dBm[2]	–99dBm[1]
Data Rate (DR)	2.5kb/s		10kb/s	8192b/s	100b/s	62.5b/s	10kb/s	100b/s
Power Consumption	110µW	108µW	176µW	20.9µW[3]	0.42nW	288nW	150µW	2.17µW
SIR	OOK –19dB @ 1MHz[4] OOK –40dB @ 10MHz[4]	OOK –23dB @ 1MHz[4] OOK –41dB @ 10MHz[4]	CW & QPSK –26dB @ 2MHz[4]	CW –2dB @ 5MHz 16QAM –15dB @ 10MHz[4]	OOK 8dB @ 1MHz OOK 5.8dB @ 3MHz	CW –16dB @ 3MHz[5]	CW –13dB @ 1MHz[4] CW –16dB @ 3MHz[4]	CW –3dB @ 3MHz
Modulation	Dual Chirp-OOK		Three-Tone Code Mod.	CE-OOK	OOK	OOK	Transmitted Reference Mod.	CE-OOK
Supply Voltage	0.5V/0.8V		0.7V	0.6V/1V	0.4V	0.75V	1V	0.5V/0.75V
Interference Rejection Method	Dual Chirp Modulation		Code-Domain Filtering, N-Path Filter	N/A	High-Q FE, DLL for CW Jammer	MEMS Filter, Offset Control Loop	Transmitted Reference, Shifted Limiter	Two Tone FSK Modulation
Active Area	0.75mm^2		0.32mm^2	2.24mm^2	0.1mm^2	3.95mm^2	N/A	4.5mm^2
Normalized Sensitivity†	–107dBm	–96dBm	–96dBm	–100.6dBm	–69.1dBm	–94dBm	–80dBm	–89dBm
FoM*	116.6dB	105.7dB	103.5dB	117.4dB	133dB	129dB	88.2dB	115.6dB

[1] MDR = 10^{-3}
[2] BER = 10^{-3}
[3] 10ms Latency
[4] 3dB Desensitization
[5] 6dB Desensitization, MDR = 10^{-2}

†Normalized Sensitivity = Sensitivity [dBm] – 10log(DR [kb/s])

**FoM = – Sensitivity [dBm] + 10log(DR [kb/s]) – 10log(P_{DC} [mW])*

Chapter 3:

A 900MHz -88dBm-Sensitivity -58dB-SIR Receiver Leveraging a Novel Chirped N-Path Filter

3.1 Introduction

A 900MHz -88dBm-Sensitivity -58dB SIR Receiver Leveraging a Chirped N-Path

In the rapidly developing world of Wireless Sensor Networks (WSNs), our environments are increasingly becoming more intelligent and autonomous. The WSNs can be incorporated into a wide variety of applications, including medical healthcare, environmental monitoring, intelligent infrastructure, and surveillance. In order to enable large-scale deployment of IoT WSNs with prolonged battery life, sensors need to meet critical and stringent physical and performance requirements such as low-power, high scalability, and small form factor. As the modern IoT era nears, delivering the promise of 1-trillion connected IoT devices relies on the ability of WSNs to operate in increasingly crowded spectrums while maintaining ultra-low-power consumption, high sensitivity, and low cost. While energy-detection (ED) based receivers consume ultra-low-power, they fail to deliver sufficient sensitivity levels for

latencies better than 1ms and are found to be susceptible to modulated interference without passive high-*Q* filtering [37] [26] [38]. The ability to handle modulated interference signals, which are becoming increasingly common in the unlicensed ISM frequency bands due to large-scale IoT network deployments and presence of multiple radio standards such as ZigBee, WLAN, Bluetooth, and cellular networks, is imperative in the design and implementation of wireless solutions for massive IoT networks [45] [46].

Basic binary modulation schemes are commonly adopted in the WSN's radio solutions because of simple and relatively low-power transceiver architectures. Among the commonly used binary modulation schemes, FSK and PSK schemes offer the highest interference tolerance [47] [30]. Nevertheless, these modulations are prone to in-band interferences [48]. Considering the limited energy budget in WSNs, simpler and more effective ULP interference robust receivers that do not compromise performance for energy-efficiency are more essential than ever. A variety of techniques have been presented in the literature to mitigate interference in ULP receivers. [36] relied on feedback loops to detect constant envelope blockers and tailor LNA bias points accordingly, but it suffers from slow loop response and operates poorly in the presence of non-constant envelope blockers. [39] and [49] presented N-path mixer-based receivers for enhanced selectivity, but require quadrature LO generation at RF frequency and rely on off-chip LO sources. Dual-IF architecture along with N-path filters were utilized in [50] to achieve enhanced sensitivity and interference tolerance, but failed to deliver sufficient levels of blocker immunity in close in-band frequencies. In this work, we have explored potential solutions on the system and circuit

level to mitigate these issues. As the first step, a closer look was taken into the spectrum in the desired RF frequency band of 915MHz.

Among the 915MHz ISM band signals being transmitted, the 802.11ah standard transmission occupies the widest bandwidth compared to the other standards, with a maximum bandwidth of 16MHz [51]. Thus, the other radio standard signals in the 915MHz ISM spectrum are relatively narrowband, making narrowband interference rejection schemes more compelling for mitigating them.

3.2 Chirp Spread Spectrum Signaling

The use of spread spectrum techniques can mitigate the effects of narrowband interference signals [52]. It is well known that Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS) are highly effective spread spectrum techniques with high performance, but these techniques mandate high power consumption and implementation complexity as argued in [53] [54]. Another spread spectrum technique that has been mostly employed for ranging and RADAR applications is chirp spread spectrum. Conventionally, the spreading and de-spreading of the signal on the transmitting and receiving ends is done using Surface Acoustic Wave (SAW) filters [55], but these had an increased cost and volume overhead. Moreover, recently chirp spread spectrum has been adopted for long range wireless transmission in the LoRa standard for LPWAN applications [42]. In this work, we have used chirp direct modulation–for spreading the RF signal–in conjunction with an OOK modulation for the data transmission. The chirp spreading can be

done either through a chirped LO or SAW filters, as discussed. Direct chirp modulation was first proposed in [56] along with Differential Phase Shift Keying (DPSK) modulation. A simplified block diagram of a conventional direct chirp modulated wireless system using chirped LO is shown in Figure 3.1.

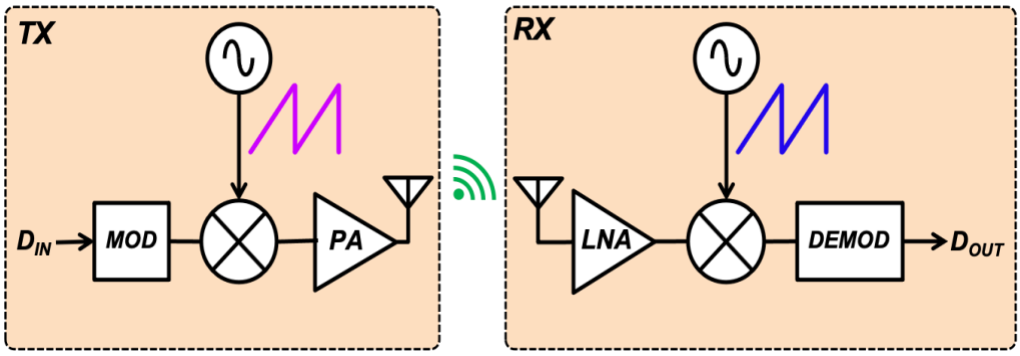


Figure 3.1 Simplified block diagram of a wireless system with direct chirp modulation

The theoretical probability of error for the traditional OOK and chirped-OOK modulation schemes as a function of energy-to-noise spectral density ratio (E_b/N_0) is calculated and plotted in Figure 3.2. As can be seen, the chirp spreading does not affect the SNR requirement compared to traditional OOK modulation.

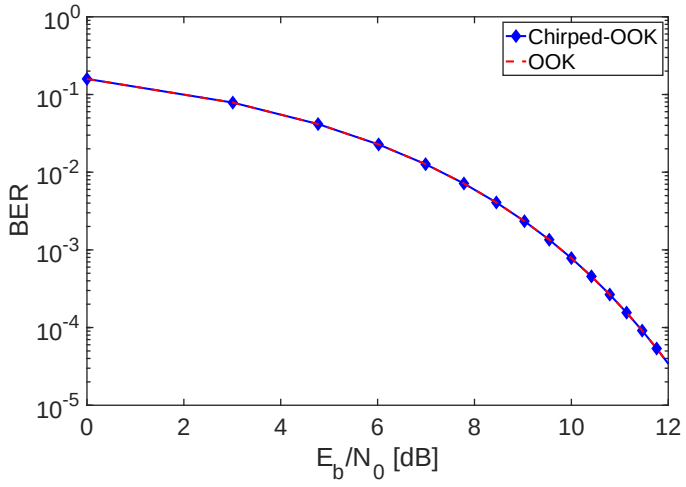


Figure 3.2 BER performance of chirped-OOK and OOK modulation schemes

However, chirped-OOK has an advantage of spreading and rejecting narrowband blockers in the spectrum. This blocker mitigation is quantified and described using processing gain which is defined as [57]:

$$G_P = \frac{BW_{CHIRP}}{BW_{Despread}}$$

Where BW_{CHIRP} is the RF chirp bandwidth and $BW_{Despread}$ is the signal bandwidth in the receiver after de-spreading the chirp message.

3.3 Chirp Receiver Architecture

As discussed in the previous section, large chirp bandwidth is essential for achieving high processing gain and strong blocker rejection in the receiver. The work in [58] demonstrated strong blocker rejection performance by employing ≥100MHz chirp bandwidth for signal spreading and de-spreading at the RF frontend. However, achieving such large chirp

bandwidth demands chirp signals be generated at RF frequencies on the RX, which requires high frequency and complex LO generation circuits that are power-intensive. Alternatively, by down-converting the RF signal to a lower IF frequency, the de-spreading of the incoming chirped RF signal can be accomplished by using more flexible and energy-efficient circuitry. However, this approach requires large IF bandwidth, which can cause severe degradation of receiver noise and linearity performance due to wide channel bandwidth. Through the use of novel techniques on the circuit and architecture levels, we have proposed a low-power solution that addresses these challenges. A novel and area-efficient chirped Miller N-path filter was proposed as a way of mitigating the challenges posed by large IF bandwidth requirements. This filter substantially limits incoming interference and noise signals right after down-conversion.

The receiver architecture is shown in Figure 3.3. A mixer-first architecture has been adopted for low-power consumption and enhanced linearity. The incoming RF signal is down-converted to an IF frequency of 7.8MHz through a passive mixer with a tone LO. The incoming RF chirp message is then filtered using a chirped N-path filter that has a time-varying frequency response, whose concept of operation is shown in Figure 3.4. The advantages of the proposed chirped N-path are: 1) reducing the incoming noise bandwidth in the receiver; and 2) filtering co-channel blockers.

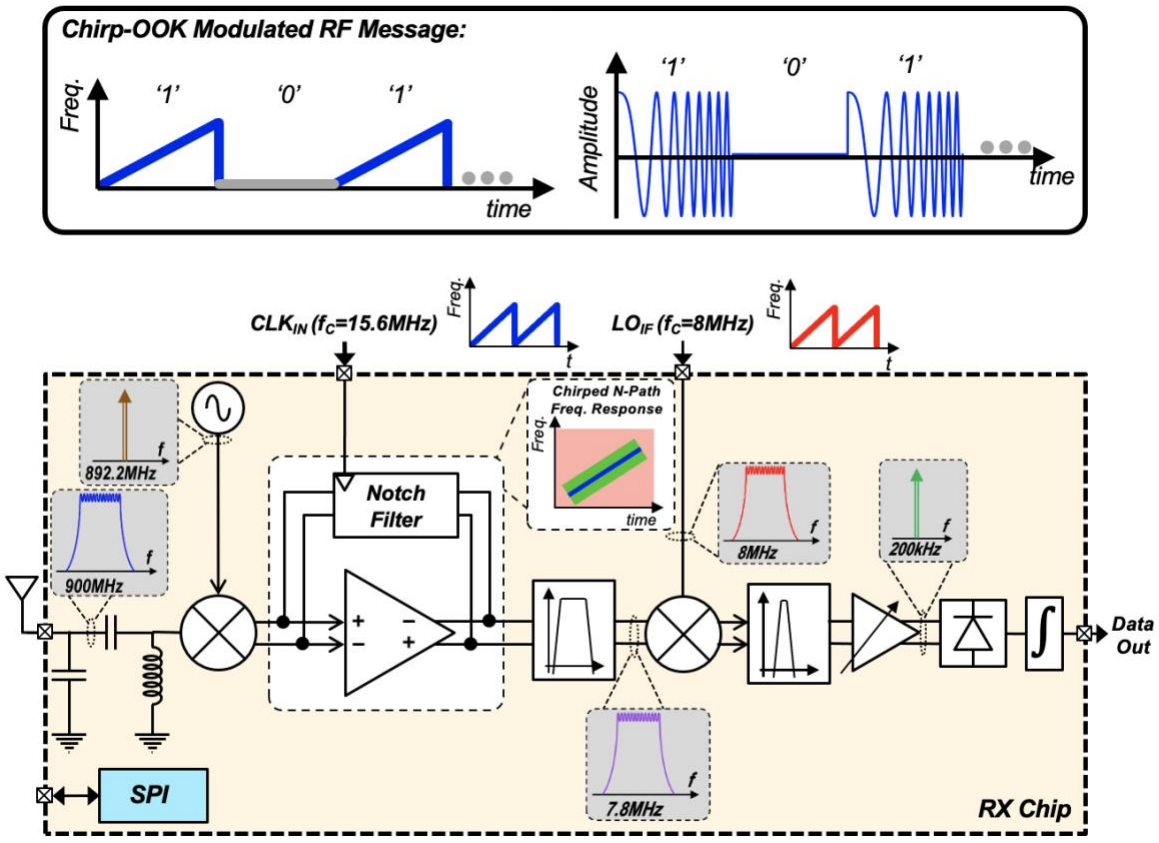


Figure 3.3 Proposed chirp RX block diagram

The IF signal is bandpass filtered using a second order active RC filter to eliminate higher order harmonics of the N-path filter output. Next, the chirp signal is correlated with a low-frequency chirped LO through a passive mixer stage, which generates a 200kHz tone signal for a '1' symbol and zero energy for a '0' symbol at baseband. The baseband signal is filtered using a second order biquad filter and amplified using PGA stages. Lastly, the ED and integrator stages obtain the energy information of the baseband signal and smooth it out.

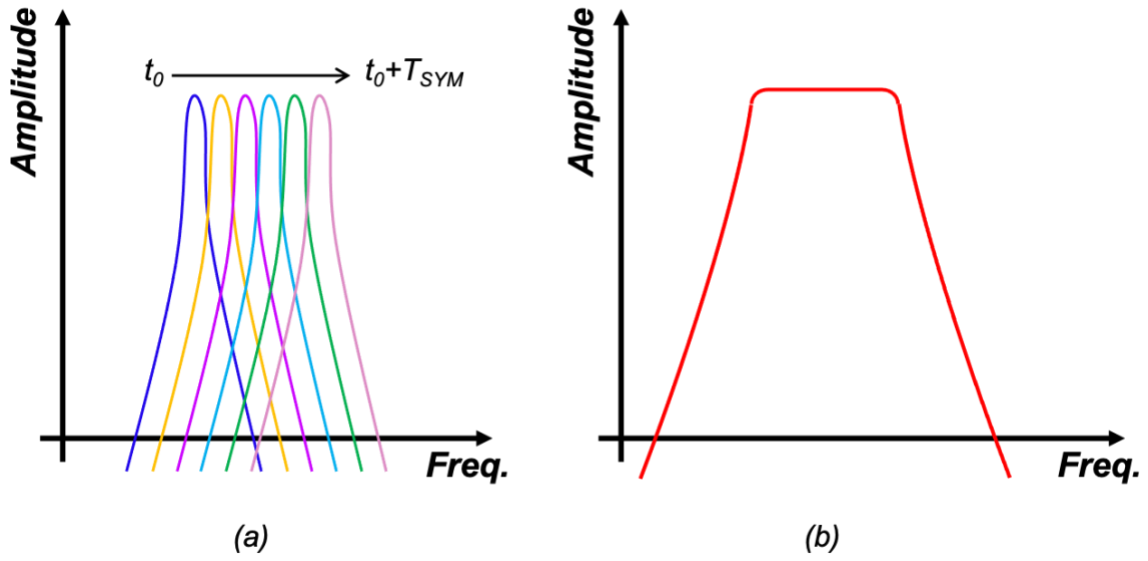


Figure 3.4 IF filter frequency response in chirp RX: (a) Time-varying frequency response with the proposed chirped N-path filter and (b) Conventional wideband bandpass filter

An additional strength of the proposed architecture is its resistance to chirped interference - even if it is co-channel. The blocker rejection would depend on the ratio of the interference and LO chirp bandwidth as well as their sweep time. The most adverse scenario arises when the chirp bandwidth and period (T_{SYM}) of the LO and interference are identical. In this case the adverse effects of the chirped blocker are significant when the interference chirp symbol edges are time-synchronized with that of LO chirp symbols, and its effect on RX performance will be similar to that of a narrowband interference in a narrowband fixed LO communication system.

3.4 Low-Power Circuit Design

3.4.1 RF Frontend

The receiver leverages a balanced passive mixer followed by a chirped 4-phase N-path bandpass filter, Figure 3.5. Filtering the wideband IF chirp with a conventional bandpass filter requires a relatively large bandwidth of 1MHz, through which in-band blockers and excessive noise would pass, Figure 3.4(b). Moreover, rejecting undesired out-of-band blockers requires steep roll-off in the bandpass filter's frequency response, which dictates higher order filters and thus added power consumption and chip area.

In this receiver, we designed a bandpass filter that addresses these challenges with minimal power and area penalty. We implemented a high-*Q* bandpass filter with a substantially smaller passband bandwidth compared to the chirp bandwidth (1MHz), whose narrowband time-varying frequency response covers the whole IF chirp bandwidth during a symbol period (T_{SYM}), Figure 3.4 (a). For this purpose, we have adopted an N-path filter whose clock frequency is chirped in synchronization with the incoming chirped-OOK symbol at IF, with identical chirp ramp rates.

Conventional passive N-path filters are able to generate the bandpass response [59] [60], but at the cost of lower RX sensitivity. Moreover, large capacitor arrays and an increased number of clock phases are required to achieve a large *Q* in the N-path filter at low IF frequencies, resulting in a greater silicon footprint and higher power consumption. Miller N-path filters have proven effective for area-efficient and high-*Q* filtering while providing voltage gain [61]. In this receiver, we have adopted a 4-phase Miller N-path filter to synthesize a chirped

N-path frequency response and simultaneously achieve sufficiently large *Q*, compact silicon footprint, and IF voltage gain.

An IF center frequency of 7.8MHz was chosen for the chirped N-path filter as an optimal solution for simultaneously achieving sufficient chirp bandwidth, high *Q* in the N-path, and low-power 4-phase clock generation. The Miller N-path stage uses a current-reused fully-differential single-stage operational transconductance amplifier (OTA) for optimal voltage gain and input-referred noise level. Moreover, four branches of switched-capacitors with 28.5pF capacitance on each were used to implement the high-*Q* Miller N-path filter.

Finally, switch sizes in the RF passive mixer and the Miller N-path filter were co-optimized to minimize the receiver noise figure and LO buffer power consumption, while ensuring sufficient RF frontend linearity.

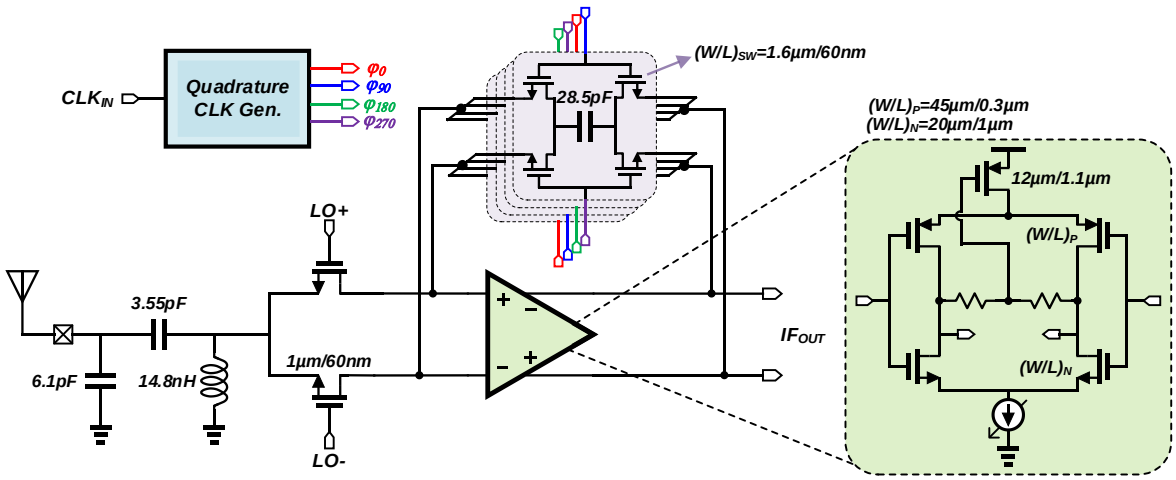


Figure 3.5 Schematic diagram of the RF frontend and IF chirped N-path filter

3.4.2 RF LO Generation

The incoming chirp-modulated OOK RF signal is down-converted using an on-chip tone LO. In this receiver a tone LO was adopted to avoid complex and power hungry chirp synthesis circuits at RF frequency. For LO frequency stability and low LO phase noise (PN) in the receiver, an LC-based digitally-controlled oscillator (LC DCO) was adopted using an in-package RF inductor, Figure 3.6.

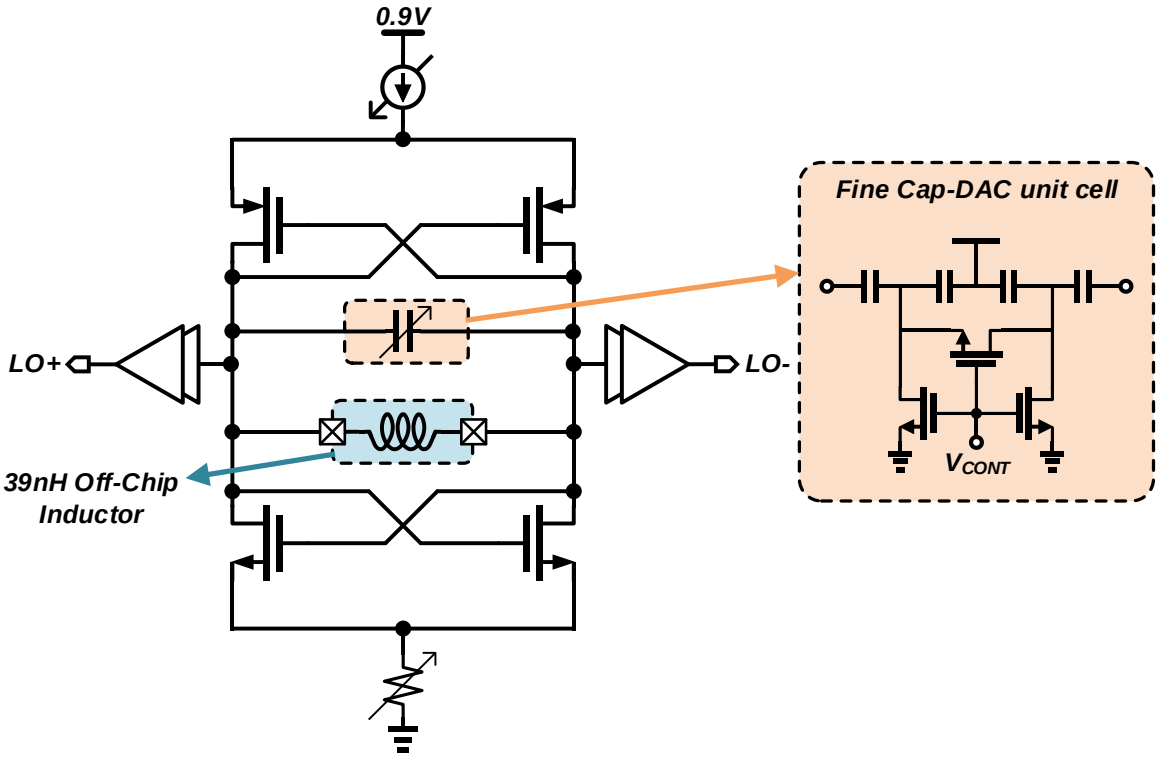


Figure 3.6 Current re-used LC VCO using in-package RF inductor

Using compact off-chip inductors in the VCO LC-tank has several benefits. First, the maximum realizable inductance value is limited to ~15nH in the on-chip inductors, depending on the process. This would translate into a limited voltage swing in the VCO's LC-tank, which could limit the phase noise of the VCO for a fixed DC bias current. Whereas

the off-chip inductors offer substantially greater values of inductance at RF frequencies that can ensure larger shunt resistance at resonance. This is very desirable for low-power circuit design, where the active current budget is severely limited.

Additionally, the DCO power consumption is primarily limited by the quality factor (Q) of the LC-tank which is dominated by the on-chip inductor's Q, typically <14, whereas the off-chip inductor typically has Q>30 at 900MHz. For instance, to achieve a center frequency of 900MHz with a target DC current budget of 70µA and a voltage swing >300mV$_{PP}$, L_{TANK}>25.5nH is required (assuming Q=30). There is, however, a limit of 15nH to the on-chip inductor values.

To gain a better perspective on how the performance of on-chip and off-chip inductors compare, the simulated quality factor of an on-chip 12nH inductor and the measured Q of an off-chip 12nH inductor with a 0402 footprint are compared in Figure 3.7. As discussed earlier, the off-chip inductor offers a significantly (2.25×) higher quality factor at 900MHz.

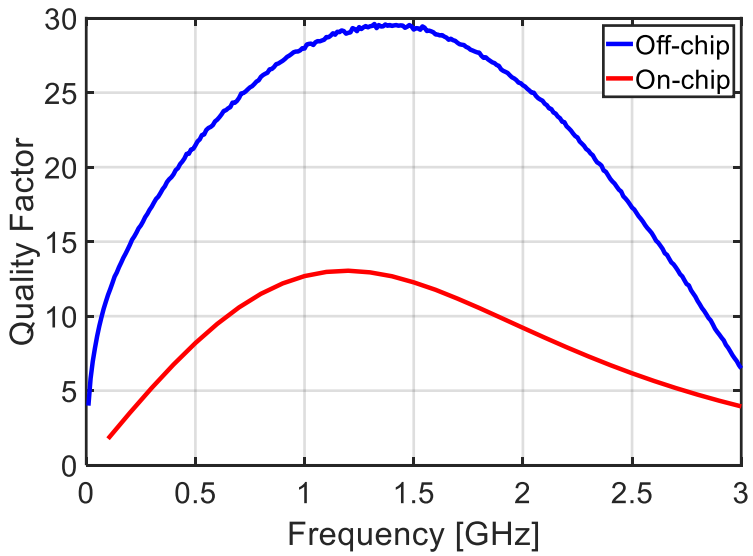


Figure 3.7 Q factor comparison for off-chip and on-chip 12nH RF inductors

In light of the advantages of off-chip inductors for low-power design, a 39nH off-chip inductor was chosen for the LC-tank to ensure sufficiently low LO PN while maintaining a small power budget. The inductor and die were integrated on a chip-on-board wire-bonding platform, allowing for a small form factor that can fit in a QFN package. The external inductor is placed close to the edge of the die for minimizing the bond-wire parasitics to avoid degrading the effective inductor *Q*. Therefore, the chip layout floorplan is optimized to only include two PADs at the side which the off-chip inductor is connected to the LC tank.

In the LC DCO, a PMOS current source and a tail resistor are employed to guarantee a 50% duty-cycle after the LO buffers to avoid self-mixing problems caused by second harmonics. Three capacitor banks for coarse and fine tuning are designed to cover the entire tuning range of 80MHz. Each unit capacitor consists of MOM capacitors and NMOS switches. To reduce the equivalent series resistance (ESR), large W/L LVT transistors are used. The LC-DCO in combination with the LO buffers consume 112μW DC power and achieve -120dBc/Hz PN at 1MHz offset.

3.4.3 IF and Baseband Circuits

The IF bandpass filter is a second order active RC biquad filter that was designed using two low-power and high-gain current-reused OTA stages with a 7.8MHz center frequency and a wide tuning range. The schematic diagram of the IF bandpass filter is shown in Figure 3.8.

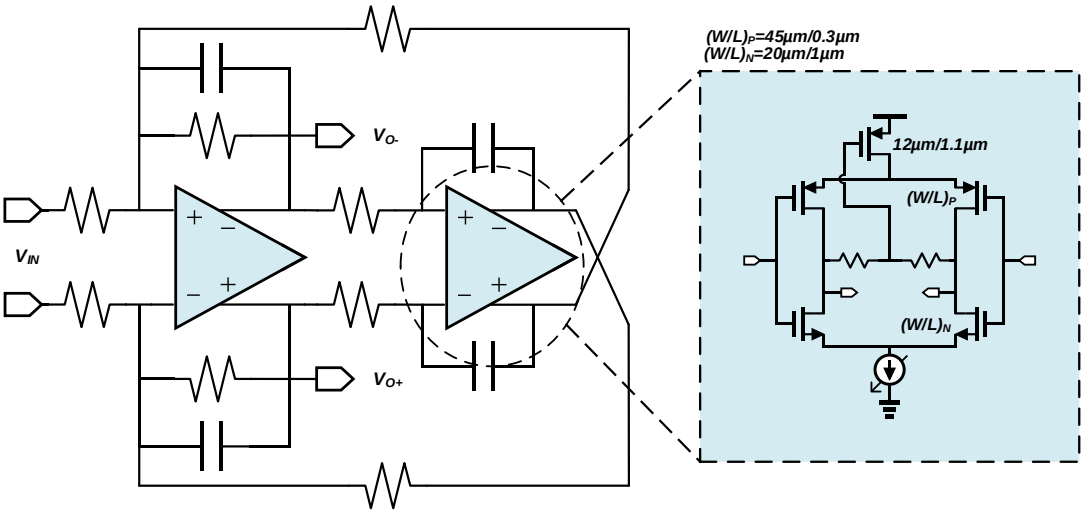


Figure 3.8 Schematic of the IF biquad filter

After correlating the incoming chirp message with a chirped LO centered around 8MHz using a double-balanced passive mixer, a second order bandpass filter was adopted to filter the desired baseband tone centered around 200kHz. A two-stage active RC biquad filter using high gain two-stage OTAs was designed, as shown in Figure 3.9.

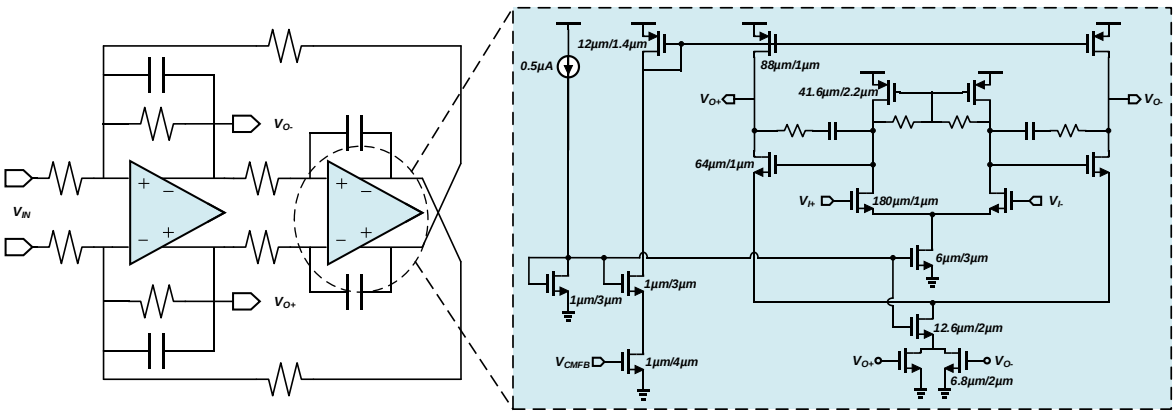


Figure 3.9 Schematic of the baseband biquad filter and OTA

The baseband signal is then amplified through two stages of PGA. To realize sufficiently small values for the lower cut-off frequencies with reasonable passive values and area, self-biased amplifier stages with programmable capacitive feedback were designed and utilized, Figure 3.10.

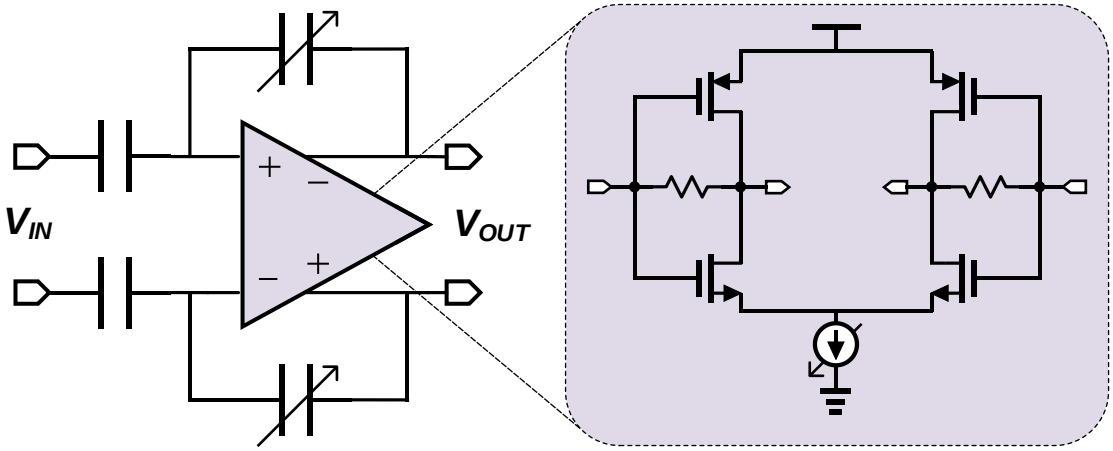


Figure 3.10 Baseband PGA stage schematic

Finally, the energy content of the demodulated chirped-OOK message is detected by an active ED stage followed by an integrator to further suppress the noise and enhance the RX sensitivity, Figure 3.11.

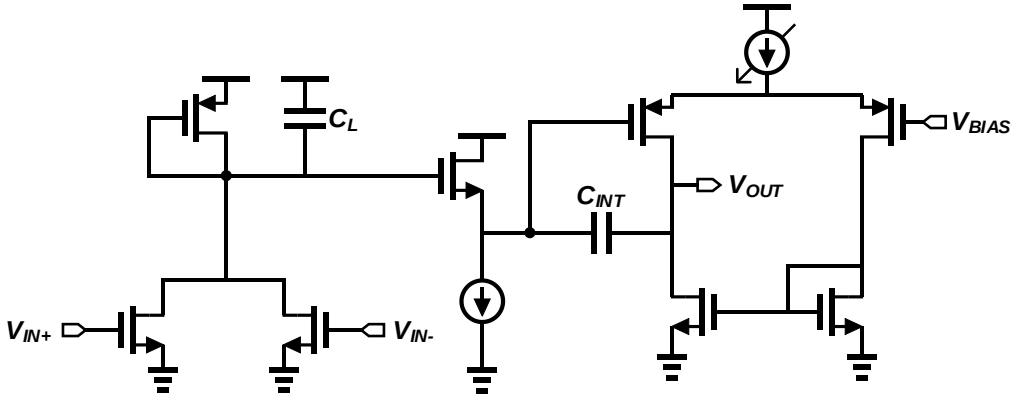


Figure 3.11 Baseband envelope detector and integrator schematic

3.5 Measurement Results

The chip was designed and fabricated in a 65nm CMOS process and occupies 2.19mm^2 area, Figure 3.12.

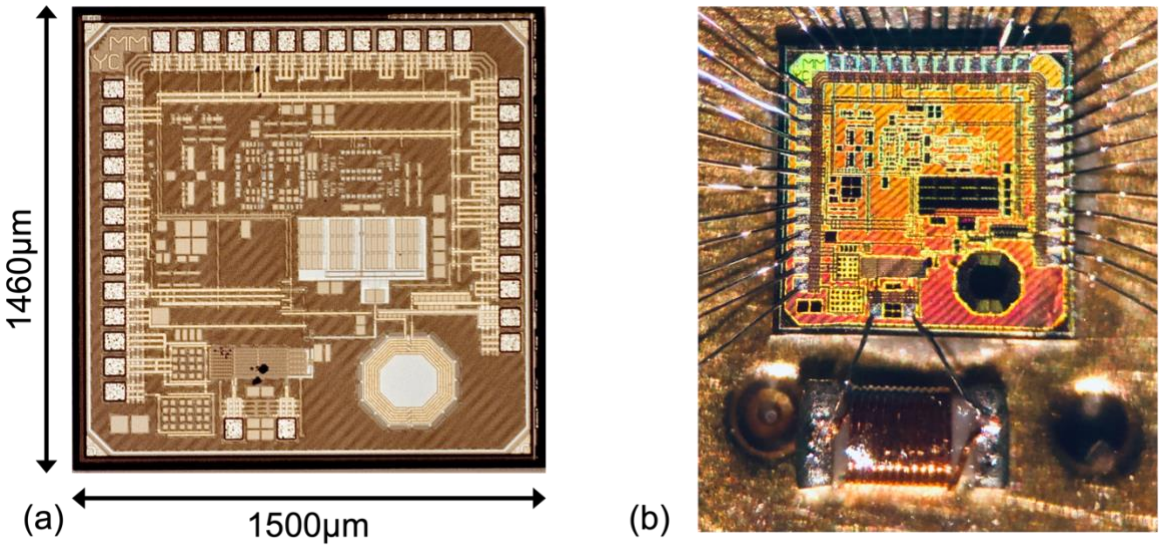


Figure 3.12 (a) Chirped-OOK RX die photo; and (b) off-chip inductor wire-bonded to the CMOS chip

The measured input reflection coefficient of the ULP receiver is shown in Figure 3.13. The receiver has 80MHz of input matching RF bandwidth centered at 906MHz.

Moreover, according to the measurement results the RF frontend combined with the IF N-path stage provide 26dB voltage conversion gain with a 3dB bandwidth of 100kHz at 8MHz IF frequency, for the tone mode of operation, while delivering approximately 26dB conversion gain in the chirped operation mode, shown in Figure 3.14.

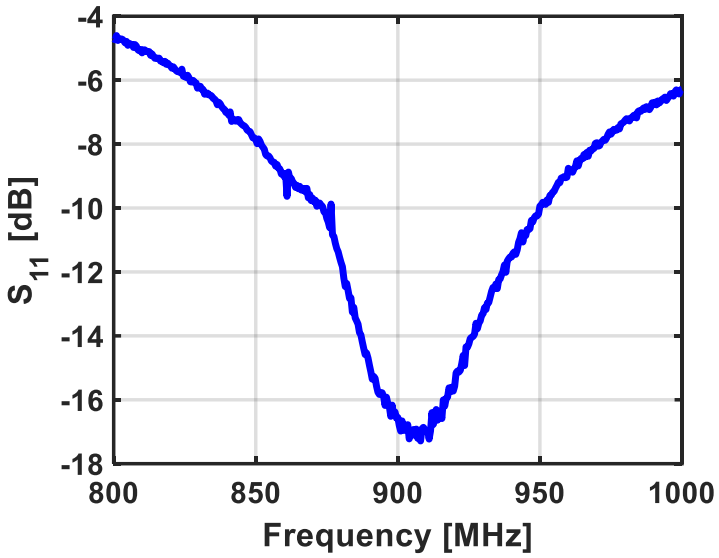


Figure 3.13 Measured RX input matching

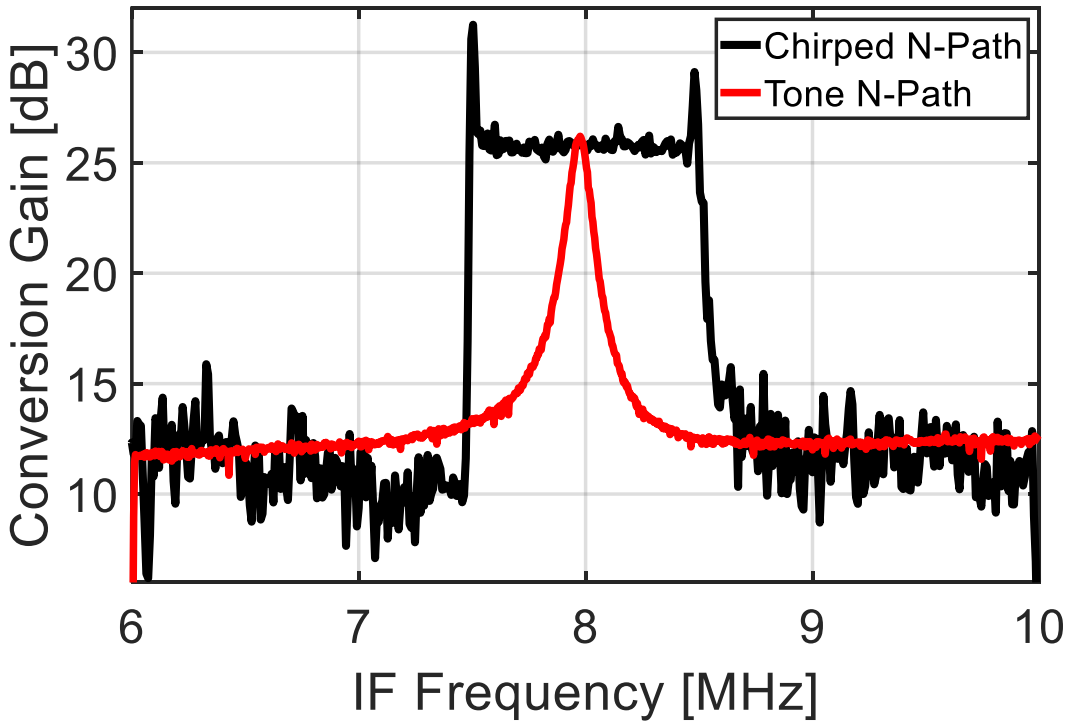


Figure 3.14 Measured frequency response of RFFE and IF N-path with tone and chirp clock

The LC oscillator is centered around 900MHz and based on measurement results, has a phase noise of -120dBc/Hz at 1MHz frequency offset, Figure 3.15, while consuming 112µW active power including the LO buffers.

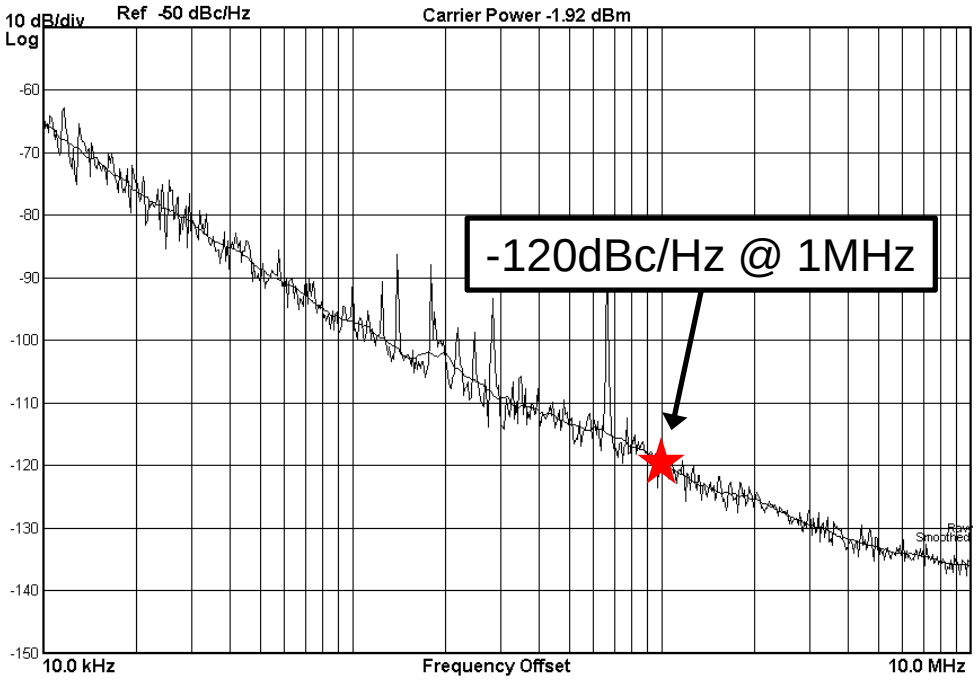


Figure 3.15 Measured VCO phase noise at 900MHz center frequency

The RX conversion gain from the RF input to the IF biquad filter output was simulated in the presence of a continuous wave blocker at 1MHz frequency offset from the RF carrier, Figure 3.16. Based on the simulation results, the conversion gain drops 1dB when the blocker signal is 38dB (or more) stronger than the RF input signal.

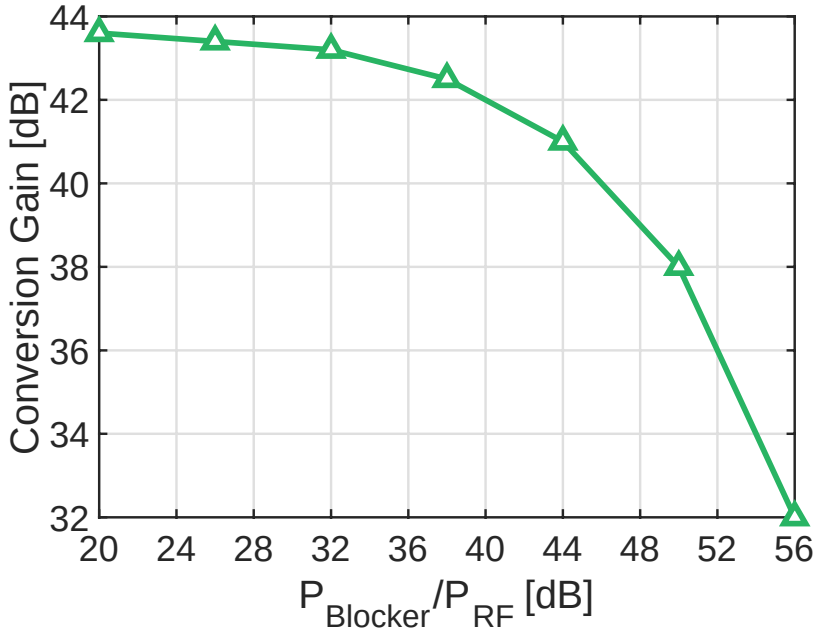


Figure 3.16 RX conversion gain in the presence of tone blocker with 1MHz offset

The power breakdown chart of the designed chip is shown in Figure 3.17, while the total power consumption is 320µW from a 0.9V supply voltage according to the measurements.

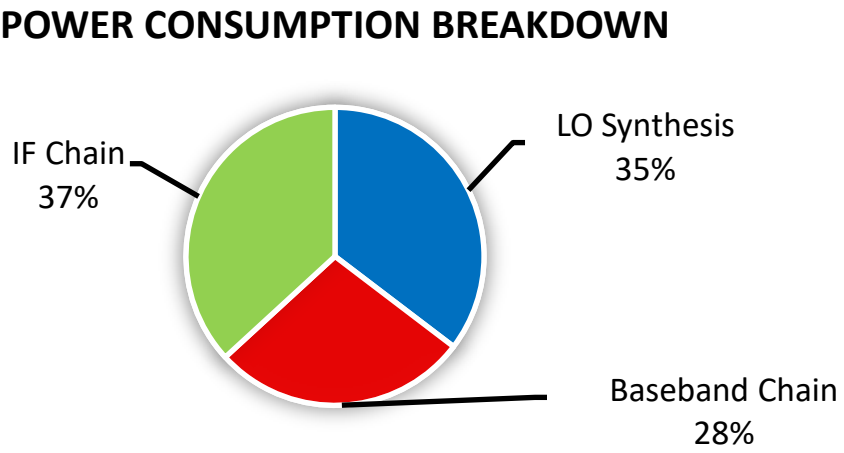


Figure 3.17 ULP receiver power breakdown chart

The BER performance of the receiver vs RF input power is measured and plotted in Figure 3.18. The receiver has -88dBm sensitivity for BER=10^{-3} at 5kb/s data-rate.

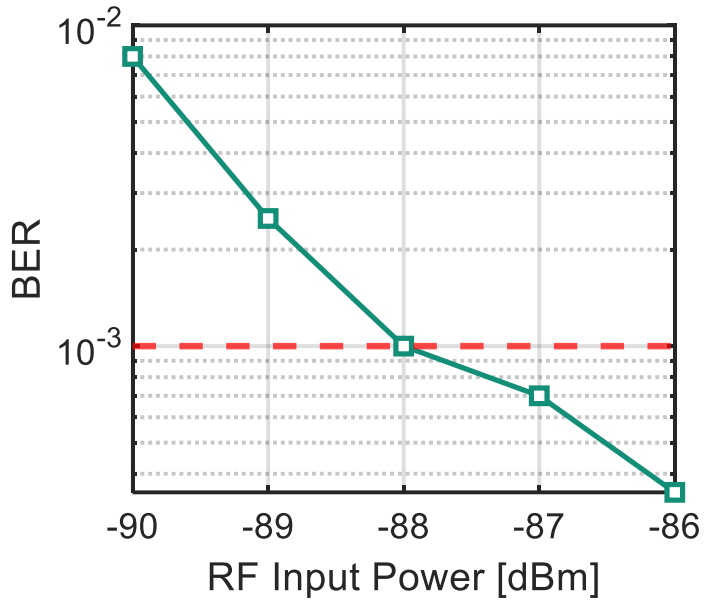


Figure 3.18 Measured RX BER performance

The receiver's performance was characterized in presence of a tone blocker signal. In this experiment, the RF input power is set 6dB above the RX sensitivity level and the maximum blocker power which guarantees BER≤10^{-3} is measured. The receiver can tolerate blocker signals as strong as -58dBc at 10MHz offset. Moreover, the receiver is capable of rejecting interference signals 40dB stronger than the desired RF message at 1.5MHz offset from the chirp center frequency, Figure 3.19.

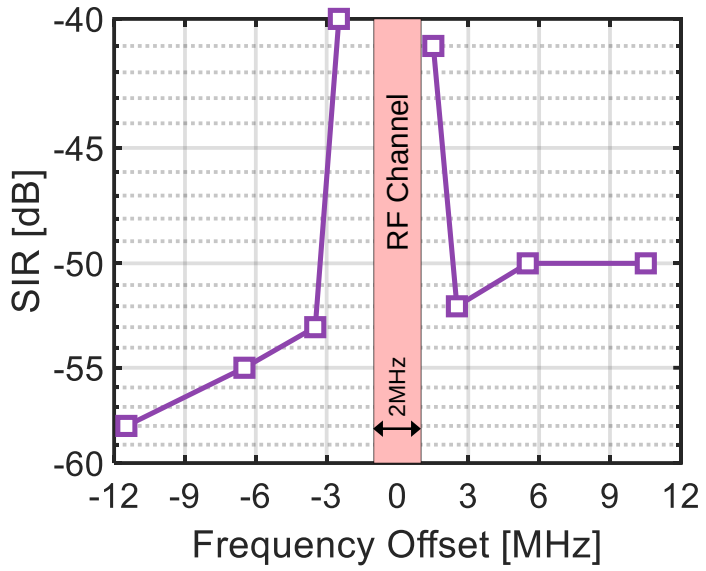


Figure 3.19 Measured receiver SIR vs frequency offset from RF carrier frequency

3.6 Conclusion

A low-power and blocker-tolerant ULP receiver was proposed and fabricated in a 65nm CMOS process, having the capacity to handle close in-band blockers as high as 41dB above the RF signal level. Several novel circuit and architecture level techniques were employed to ensure strong interference tolerance and high sensitivity levels while maintaining a power consumption level well below a milliwatt. The performance of the proposed ULP receiver is compared with state-of-the-art in Table 3.1. The receiver achieves -88dBm sensitivity at 5kb/s data-rate while consuming 320µW of active power and can reject blockers as strong as 58dBc. In Figure 3.20, the normalized sensitivity and SIR performance of this ULP receiver is compared with sub-mW ULP receivers published in the literature. This receiver

achieves the highest SIR among the sub-mW receivers, while consuming 36% lower power compared to the closest data point on the SIR comparison plot.

Table 3.1 Performance summary and comparison with state-of-the-art

	This Work	**ISSCC 2015** [50]	**RFIC 2020** [34]	**ESSCIRC 2019** [62]	**JETCAS 2014** [58]
RX Power	320µW	99µW	445µW	499µW	235µW
Sensitivity	–88dBm	–92dBm	–91.5dBm	–99dBm	–70dBm
Carrier Frequency	900MHz	2.4GHz	2.4GHz	915MHz	2.4GHz
CMOS Technology	65nm	65nm	40nm	55nm	65nm
Voltage	0.9V	0.5V	0.2V/0.45V	0.9V	1.2V
Modulation	Chirped-OOK	OOK	MC-OOK	BFSK	Chirped-FSK
SIR	–41dB @ 1.5MHz –58dB @ 10MHz	–4dB @ 1MHz –27dB @ 5MHz	5dB @ 1MHz –18dB @ 5MHz	–4dB @ 1MHz –20dB @ 5MHz	–7dB @ 1MHz –7dB @ 5MHz
Data-Rate	5kb/s	50kb/s	62.5kb/s	100kb/s	1Mb/s
Matching Network	On-chip	On-chip	On-chip	On-chip	Off-Chip Inductor

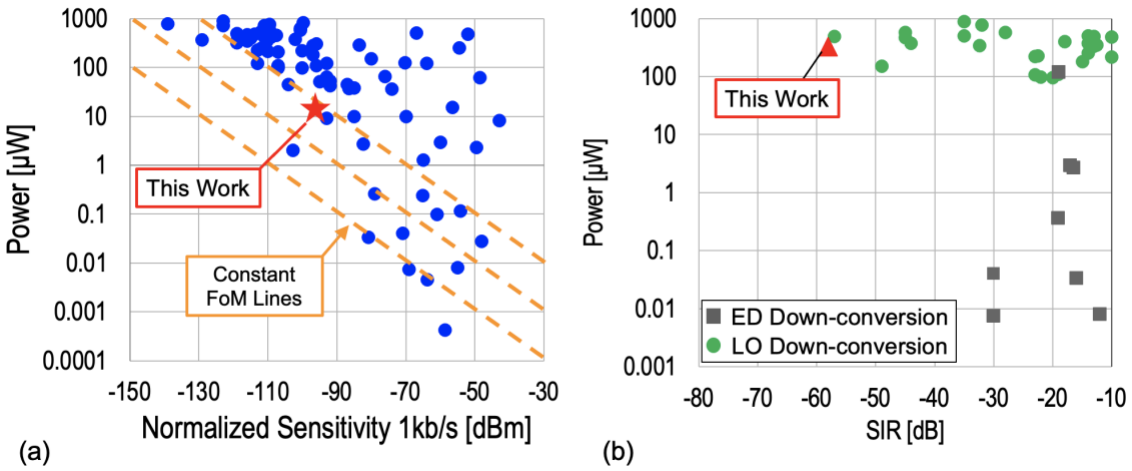


Figure 3.20 ULP RX performance comparison with sub-mW radios published in the literature (adopted from the ULP RX survey [63]) (a) normalized sensitivity; and (b) SIR.

Chapter 4:

Wireless Ranging Technologies

4.1 Introduction

Researchers have long debated the possibility of using wireless signals for not just communication, but also sensing purposes. A new research area focused on utilizing radio waves to sense the environment was discovered by Heinrich Hertz in 1886, when he demonstrated that radio waves can be reflected from solid objects. World War II saw the widespread adoption of radar techniques in various countries to detect objects far away. A radar signal round trip travel time can be calculated easily and precisely to pinpoint an object. A project of the US government called the Global Positioning System (GPS) was launched in 1973 for the purpose of obtaining geolocation and time information anywhere on or near the surface of the Earth with satellite signals.

Context-aware computing is a computing model wherein services can recognize and exploit contextual data. [64] defines context as any information that can be used to characterize the situation of an entity. In essence, almost any information available at the time of an

interaction is considered context information, including time of day, light level, who you are with, as well as battery, display, network, or bandwidth availability. There has been a lot of interest in methods that provide knowledge of an object's location both in research and business. The location data provides contextual information which when combined with sensor data can provide additional derived insights.

An instance of context-aware service is one that can extract, interpret, and use information from its environment, such as location. Numerous services rely on being aware of where something or someone is located. Especially, as the Internet of Things (IoT) expands, wireless ranging and localization are gaining popularity in part because of their ability to provide a broad range of services and omnipresence via connectivity.

Increasingly popular smart phones are driving an exponential growth in the demand for location-based services. Intelligent malls and warehouses as well as public safety tracking are becoming commonplace, thanks to the modern wireless technologies. In a similar fashion to the search engine on the Internet, a localization system is a search engine for the real world.

A wide array of operations, such as monitoring facilities at a commercial port like the Los Angeles port or managing assets at a skyscraper construction site, heavily depend on contextual information. In such environments, deploying WSNs at every point is essential in obtaining environmental data–including location data–that can be used for a multitude of applications. Nonetheless, there are a handful of limitations to the hardware and energy resources available in a WSN, which makes collecting information quite challenging. Thus, in order to fully harness the limited resources in the WSNs, maximize the operating

efficiency, and provide users with a unique experience, it is indispensable that the WSNs are capable of determining their real time position with minimal hardware and energy overhead. Therefore, it is imperative to consider and analyze the energy consumption and hardware requirements of different localization methods for different applications.

Studies in the literature mainly focus on the network, system, signal processing, and accuracy aspects of various methods of localization and rarely address the hardware implementation requirements [65] [66] [67], especially in the context of Internet of Things and its implications for WSN design for localization and ranging systems.

A comprehensive survey of ranging and localization systems is presented in this chapter, with an emphasis on their suitability and effectiveness for use in IoT networks. Various perspectives on the localization system are discussed, including complexity, accuracy, cost, infrastructure, energy-efficiency, privacy, security, and scalability [68] [69] [70].

4.2 Localization Techniques

In this section, different approaches for determining the location of an object are covered. These techniques leverage various information such as range, angle, etc. to determine the location of the WSN.

4.2.1 Angle of Arrival

In the Angle of Arrival (AoA) method, antenna arrays on the receiving end are employed to determine the angle at which the incident wave intrudes the receiver [71] [72]. As shown in Figure 4.1, this angle can be estimated through calculating the time difference of arrival at

individual elements of the antenna array. While this method can be effective for short distances, it faces serious challenges when it comes to long distance applications, as even small errors in angle calculation could result in a large location error, mandating more sophisticated hardware solutions. Its major advantage is that it requires only two transmitter anchors in order to determine node locations in the 2D space and three anchors in order to determine node locations in the 3D space.

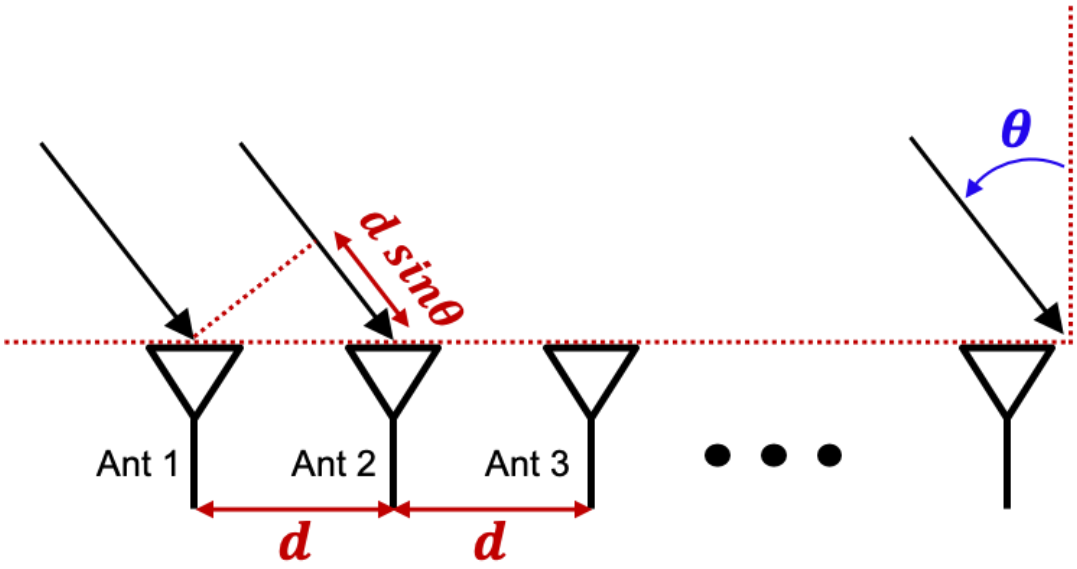


Figure 4.1 Angle of Arrival operating principle

4.2.2 Angle of Departure

As with the AoA method, the Angle of Departure (AoD) method determines the incident waveform's angle by observing the phase difference between the antenna elements [73]. The antenna array elements, however, are employed only on the transmitting anchor device, and not on the receiving end, Figure 4.2. As a result, this method can potentially shift the energy-consumption and hardware complexity burden of the WSNs to the reference node by

eliminating the need for antenna arrays on all sensor nodes. Thus, reducing the cost, size, and complexity of WSNs is possible and could eventually lead to their widespread adoption.

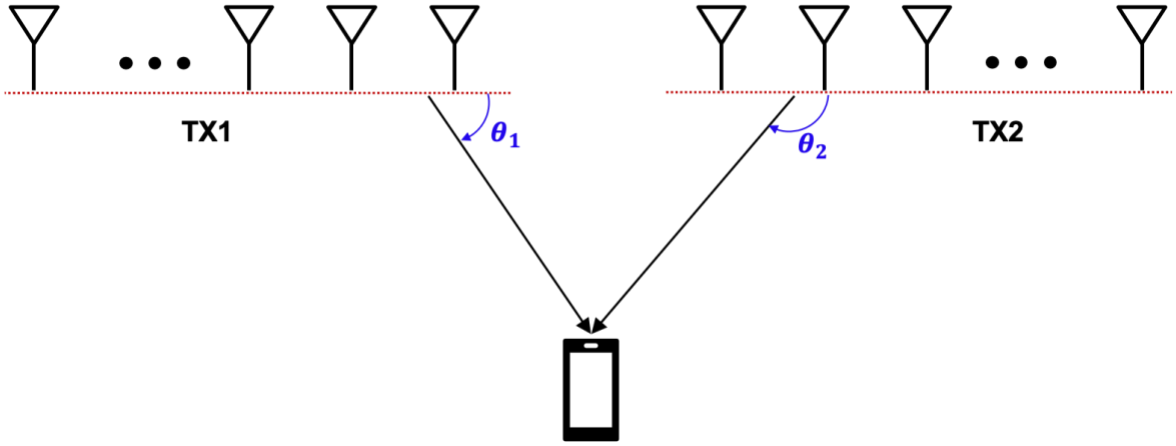


Figure 4.2 Angle of Departure operating principle

4.2.3 Phase of Arrival (PoA)

In this method the distance between the transmitter and the receiver is estimated using the phase or phase difference of the carrier signal [74]. It is common for the signals transmitted from the anchor nodes or user device to be of pure sinusoidal form, with the same frequency and zero phase offset, to identify the phase of the signal at the receiver side. As visualized in Figure 4.3, one of the techniques to obtain the distance between the transmitter and the receiver involves assuming a finite delay, T_d, between the transmit and receive units, which can be converted into a fraction of the signal wavelength and thus is related to phase shift [74].

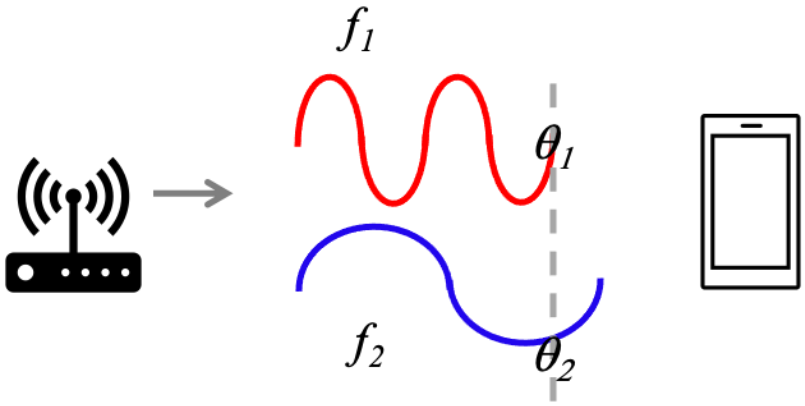


Figure 4.3 Range estimation using Phase of Arrival

4.2.4 Received Signal Strength Indicator (RSSI)

One of the simplest techniques for ranging is Received Signal Strength (RSS), which is widely adopted for a wide variety of applications [75]. The RSS can be used for estimation of distance between the transmit and receive units and represents the actual incident signal power at the receiver and is commonly expressed in dBm or milliwatts. Through application of different wave propagation models, the absolute distance between the TX and RX can be estimated [76]. On the other hand, the RSSI is defined as an indicator for the RSS, which is a relative measure of RSS [77]. As discussed, the distance between the TX and RX units (d) can be estimated as follows:

$$d = 10^{\frac{R_0 - RSSI}{10n}}$$

Where R_0 is the reference RSSI value at a reference distance and n is the path loss exponent. The RSSI-based method is fairly simple and cost-effective, requiring minimal hardware overhead. However, it suffers from poor accuracy, especially in crowded environments and with the presence of multipath effect.

4.2.5 Channel State Indicator (CSI)

The transmission channel, over which the data is transmitted, has a frequency-dependent amplitude and phase response. In some cases, such as Ultra-Wide Band (UWB), a wideband signal is transmitted over the air that might have a higher bandwidth compared to the channel, in which case might distort the signal phase and amplitude information. In addition, a TRX link with multiple antennas may produce a different channel frequency response depending on the spacing between the array elements. As a way to mitigate this problem, channel impulse responses (CIR) are used to extract frequency-dependent channel responses, enabling higher precision in ranging and localization [78] [79]. The channel frequency response is often referred to as CSI.

4.2.6 Time of Flight (ToF)

This method leverages the wave propagation delay between the transmitter and the receiver to determine the distance between them and is also known as Time of Arrival (ToA) [80]. The target distance can be calculated by multiplying the ToF by the wave propagation speed, i.e. 3×10^8 m/s. Once the distance between the sensor node and the anchor nodes (minimum 3 anchors) is known, the location of the sensor node with respect to the anchors can be obtained using basic geometry, Figure 4.4.

There are two different approaches for ToF measurement, one is in time domain, in which the sampling rate at the receiving end affects the ranging accuracy. The other approach is frequency domain ToF, in which the transmitted signal's bandwidth determines the ranging resolution. This method is advantageous for adoption in multipath environments and is

comparatively simple; however, in order to operate accurately, timing synchronization between the anchor nodes as well as the sensor nodes is obligatory.

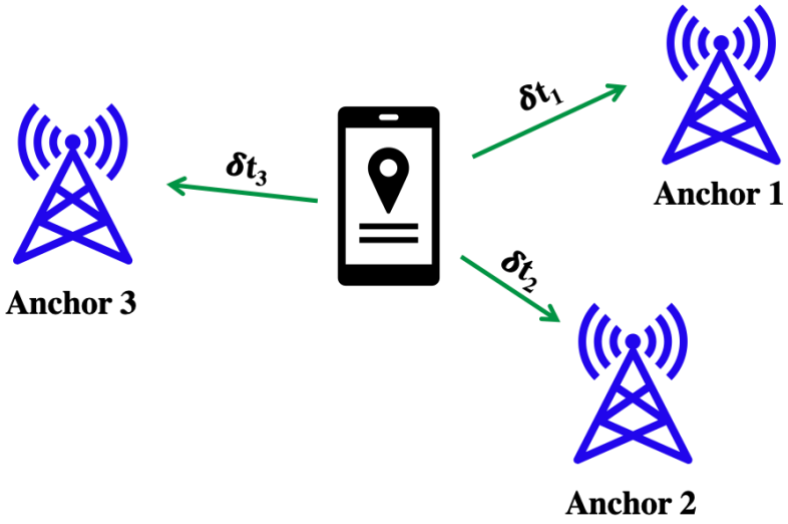


Figure 4.4 ToF ranging and location finding

4.2.7 Time Difference of Arrival (TDoA)

In this approach, the difference between the measured wave propagation time from the anchor nodes to the sensor node is leveraged to calculate the location of the sensor node with respect to the anchor nodes, where a minimum of three anchors are required. Once the wave propagation time differences are obtained, a system of hyperbola equations will be formed which could be solved for the sensor location [81]. In contrast to the regular ToA method, TDoA uses the difference in propagation times whereas the ToA method uses the absolute propagation times for sensor positioning. By comparison, this method has the major advantage that only the anchor nodes need to be synchronized, whereas with the ToA method, both the anchor nodes and the sensor nodes must be synchronized. This advantage

is accentuated even further by the fact that IoT networks usually consist of thousands or even millions of WSNs. In such scenarios, adopting the TDoA would have a significantly lower power, cost, and network complexity overhead compared to the ToA method, since timing synchronization is only necessary between anchor nodes, which could be as few as three anchors.

4.3 Ranging and Localization in IoT Networks

In IoT networks, millions of sensor nodes are connected wirelessly and are utilized for applications where a massive number of connections is needed with low energy usage and low data rates. The latency of the data transmission is usually insignificant as well. The need for localization is often very strong for such applications, which usually require additional infrastructure and increase costs. The vast number of already deployed WSNs, combined with the relatively low power consumption and cost of these networks would make existing IoT networks a compelling option for applicability in ranging and localization applications. Some of these applications include environmental monitoring, smart transportation, smart cities, intelligent animal tracking, emergency services, and smart homes.

A majority of IoT sensor nodes currently operate with existing localization sensors (e.g. GPS, Bluetooth, WiFi, and gyroscope) and a standard radio communication module (e.g. NB-IoT, LoRa), which add power and cost overhead. Due to the introduction of LPWAN, communication modules can be made significantly more affordable. As an example, the combination of LPWAN (for communication) and GPS (for positioning) has been adopted

for patient monitoring [82] and highway tracking [83]. In addition, if LPWAN–or potentially any other IoT communication link such as Bluetooth–can be explored to provide localization capabilities, it may be possible to reduce or eliminate other localization sensors to further reduce node costs and power consumption.

The base stations, which are widely deployed in IoT networks and have fixed locations, can also act as the anchor nodes for ranging and localization. Ultimately, these steps would allow for the addition of services which require location-stamped sensor data with minimal infrastructure addition costs. However, given the limited available resources in IoT networks along with their massive number of WSNs, while evaluating and comparing different wireless ranging and localization methods and approaches in IoT networks, there are several important factors to consider:

1) **Energy-Efficiency:** The battery capacity on the WSNs is limited, which could pose severe limitations on the lifespan of WSN. It is crucial to use energy-efficient circuits and systems in order to avoid additional economic and environmental costs associated with battery maintenance. In addition, location data is intended to improve the services provided to the users. The use of such systems that consume a great deal of energy and drain the batteries of user devices might not be widespread. This is because localization is an additional service on top of what the sensor node is primarily intended for, such as sensing and communication.
2) **Communication capability:** It is crucial for the WSN to be able to obtain location information and communicate, with minimal hardware overhead. Wireless

transmission schemes that are capable of data transmission and ranging/localization are key enablers of such sensor modules.

3) **Range:** When evaluating a localization method, it is also essential to evaluate the receiving range of the technology used. Ideally, the range of a standard localization system should be adequate so that it can be effective in large spaces such as hospitals, airports, office spaces, etc.. In addition, a large range will result in fewer anchor points and reduced cost. Nevertheless, the increase in distance between the transmitter and receiver can result in interference and performance degradation. Based on the intended application of the localization system, the reception range could be chosen.
4) **Latency:** Real-time range/location requires the system to report the user's location data instantly. Which requires the system to be able to identify users with minimal information and perform complex operations with millisecond precision, that could reduce the accuracy of estimating users' positions. In the same vein, to achieve reliable and high-accuracy location data, the adoption of complicated and time-consuming signal processing techniques are not feasible, which accentuates the urge for designing fast and efficient algorithms and hardware for ranging DSP.
5) **Accuracy:** The accuracy with which the sensor position is obtained is one of the most important characteristics of ranging/localization systems. Obtaining the location data in the indoor environments faces severe challenges due to multipath effects. Hence, it is crucial that the system limits the impact of multipath effects and other environmental noises in order to achieve high accuracy, which requires DSP.

In an ideal world, the localization system should be able to pinpoint the user or object to within 10cm accuracy.

6) **Scalability:** Highly scalable IoT networks and WSNs are key enablers of the promise of one trillion IoT-connected devices. As a result, it is critical to consider the bandwidth, network, energy, and hardware implications of ensuring high scalability in the WSNs and the base stations.

7) **Infrastructure requirements:** One of the basic requirements for wide-scale adoption of ranging/localization systems is to rely on a technology that is readily available within the sensor nodes, therefore no additional hardware on the sensors and the base station is required. In order to achieve wide adoption of the ranging/localization technology, this is crucial. It is therefore necessary to develop localization systems that can operate smoothly on the existing infrastructure, such as smartphones, WSNs, and base stations. In most cases, WiFi is the most prevalent technology, which is readily available in various environments. In addition, visible light and Bluetooth are two other possible technologies to consider for wide adoption.

8) **Privacy and security:** With the exponential growth in the number of WSNs and IoT networks, and the potential for intruders to access the data, security has become a major concern for users. Therefore the WSNs and the IoT networks must be equipped with secure wireless connectivity and geolocation data collection.

4.4 Ranging and Localization Technologies

In this section, a wide variety of existing ranging/localization technologies presented in the literature will be covered. In addition, both the network-level and circuit-level details and requirements of the presented systems will be discussed.

4.4.1 Bluetooth

The Bluetooth Low Energy technology, or BLE, is a wireless communication technology that can be used to track the location of people, assets and devices in the indoor environment. Bluetooth technology is widespread and compatible with so many of today's devices, making it a ubiquitous technology in indoor spaces. A BLE-enabled device can transmit data via radio waves, just like WiFi and UWB. In a basic localization system, through using a Bluetooth receiver, e.g. a smartphone, a Bluetooth receiver was employed to measure the RSSI of the Bluetooth signal from fixed beacons. As another option, fixed anchors can measure the RSSI of the Bluetooth signal transmitted by the moving device, also called a tag. An RSSI-based method typically has an accuracy level of a few meters and is commonly used to detect whether assets or people are present in a room [84]. This method has a few shortcomings, including accuracy and privacy concerns. There have been efforts to enhance BLE RSSI-based ranging in indoor environments by combining RSSI information with ToF [85]. In the latest release of the BLE standard, Bluetooth 5.1, the standard specification introduces fine-grained positioning features in this wireless standard, which prove essential to context- and location-based applications within the IoT networks [86]. The standard employs two new signal processing techniques to determine the AoA and AoD of a

transmitted signal. Combined with distance estimation [87] [88], the AoD and AoA techniques aim to help pinpoint the precise location of a device.

Additional BLE-compliant works have been proposed in the literature for ranging application. A phase-based ranging system leveraging the tone extension in a BLE 5.1 packet was presented in [89] that utilizes BLE channel hopping to exchange tones in the entire 2.4GHz ISM band to mitigate multipath fading problem. This system can be potentially widely adopted and scaled due to its standard compliance and narrow bandwidth requirement. Moreover, the phase-based ranging can be done even on BLE advertising events, meaning secure ranging could be achieved without requiring pairing to the (commonly unknown) anchors with the sensor nodes. There are a few drawbacks to this method, despite its high spectral efficiency: 1) the ranging system faces a range ambiguity which depends on the frequency spacing of the transmitted tones; 2) multipath fading in indoor environments can cause severe ranging performance degradation; and 3) measuring the phase in the baseband DSP can potentially be power-hungry and pose additional hardware cost.

4.4.2 WiFi

WLAN, also known as IEEE 802.11 or WiFi, operates in the ISM frequency band and is mainly used for providing wireless connectivity and access to the Internet for multiple devices in a private, public, or business environment. IEEE 802.11ah (primarily designed for IoT services) has enhanced WiFi's range to approximately 1km from 100m [15], which is primarily optimized for IoT. The majority of consumer electronic devices, such as smartphones and smart watches, are equipped with WiFi, making this a prime candidate for

localization [90] [91] [92]. In such systems, the already existing wireless access points can be used as anchors for signal collection [92], allowing basic localization systems to be configured without the need for additional infrastructure. The simplicity of RSSI has led to its widespread adoption as a ranging and localization technique in WiFi networks; however, the accuracy of such systems is usually limited to a few meters, which does not suffice for public safety applications that require precise location information. Additionally, RSSI measurements for indoor environments have significantly lower accuracy. In [92] a new approach for mitigating multipath effects was presented that utilized the RSSI info in conjunction with the AoA to estimate the most likely position of the sensor node.

WiFi networks rely on OFDM modulation schemes for data transmission, which demand complex and power hungry analog and digital circuit implementation both on the transmitter and the receiver ends, primarily due to the stringent linearity specs dictated by the 802.11 standard. Therefore, even with WiFi's wide adoption in the existing environments, it might not be very suitable for energy-restricted WSNs.

4.4.3 UWB

A UWB system transmits ultra-short pulses that have a period smaller than 1ns and a large bandwidth (>500MHz), in the frequency range from 3.1GHz to 10.6GHz, using a very low duty cycle [93] which results in reduced power consumption. Historically, this technology has been used mainly for short-range communications, such as PC peripherals and other indoor applications. Specifically, UWB technology has proved to be particularly advantageous for indoor localization since it is immune to interference (due to its unique signal type and spectrum characteristics), while the UWB signal (particularly low

frequencies included in the UWB spectrum) can penetrate a variety of materials, including walls. Moreover, as the UWB pulses have a very short duration, they are less susceptible to multipath effects, allowing the identification of the main path even in the presence of multipath signals, and accurately estimating the signal ToF, which has been shown capable of achieving localization accuracy as good as 10cm [94]. The slow pace of UWB standard development has limited its adoption in consumer electronic devices and sensor nodes in particular. UWB localization networks are comparatively scalable for IoT applications and prior analysis has demonstrated that up to approximately 6000 tags can be handled by a single cell [95].

4.4.4 ZigBee

The ZigBee technology is based on the IEEE 802.15.4 standard, which focuses on delivering low cost, low data rate, and energy efficient personal area networks [96]. The ZigBee protocol serves as the foundation of wireless sensor networks and it defines the higher levels of the stack. While ZigBee's Network Layer manages multi-hop routing and network organization, the Application Layer handles distributed communication and applications development. The ZigBee protocol is beneficial for locating sensors in a WSN, but is not widely adopted in the majority of user devices and sensor nodes, so it is not a good choice for pinpointing widescale IoT networks.

4.4.5 NB-IoT

The Third Generation Partnership Project (3GPP) released its release 13 introducing Narrow-Band-IoT (NB-IoT) in 2016. NB-IoT operates in the licensed spectrum as opposed to other LPWAN technologies, such as Sigfox and LoRaWAN. As a result, this wireless

technology is becoming increasingly popular among providers over other LPWANs. NB-IoT, for instance, may be deployed with existing LTE infrastructure, allowing existing LTE service providers to quickly and efficiently adopt widescale NB-IoT networks. By introducing the Observed Time Difference of Arrival (OTDoA) in Release 14, 3GPP introduced NB-IoT localization [97]. The NB-IoT can also use a number of Received Signal Strength (RSS)-based localization approaches in addition to timing-based approaches [98]. Though NB-IoT is still in its infancy and still in its development phase, it would be hard to consider it as the most efficient solution for localization in IoT networks. The reason for this mainly stems from the strict NB-IoT requirements, which translate into complex circuit implementations with drastically higher power consumption levels than those being adopted in energy-autonomous wireless networks.

4.4.6 LoRaWAN

Essentially, LoRaWAN is a proprietary Medium Access Control (MAC) protocol, which sits on top of the LoRa physical layer, which uses Chirp Spread Spectrum (CSS) technology. Several commercial LPWAN platforms have already implemented LoRaWAN as a way to connect large scale IoT networks with long-range and low data-rate communications. LoRa technology differs from other IoT technologies in its use of CSS modulation, a spread spectrum technique by which the signal is modulated by linear-frequency-modulated sinusoidal pulses, known for its immunity to interference, multipath and Doppler effects. Considering these features, CSS is an ideal geolocation technology, particularly for devices traveling at high speeds. Since the server and the device are located at such a long distance (around 2-5 km in urban areas/15 km in suburbs), multipath resolution becomes more

challenging, thereby reducing the accuracy of LoRaWAN geolocation. Recently an ultra-high resolution time-stamp attached to each received LoRa data packet has been introduced by LoRa for TDoA-based localization; however, fine-grained indoor accuracy cannot be achieved with such system unless additional monitors are deployed in the indoor environment where the WSNs of interest are located [99]. Nevertheless, hybrid approaches such as combining the location data from GPS and LoRa networks for delivering enhanced accuracy was presented in the literature [99].

4.4.7 RADAR

Although radar is mostly known for its use in military applications, it is also used for ranging and target tracking in outdoor environments for a wide variety of applications such as surveillance, autonomous vehicles, military, security, smart cities, etc.. By estimating the round-trip time of flight (RToF) in time or frequency domain the target distance is determined. There are several techniques available in the literature to measure the RToF:

1) **Frequency Modulated Continuous Wave (FMCW) Radar:** This approach transmits a chirp signal and mixes the reflected wave with a local copy of the TX signal, resulting in a low-frequency tone. The center frequency of the baseband tone is proportional to the RToF (τ) and can be extracted through FFT to estimate the target distance [100] [101], Figure 4.5. In this approach, the ranging resolution is inversely proportional to the chirp bandwidth, thus demanding large bandwidth for high accuracy applications. In contrast to the other types of radar, the FMCW radar

circuit implementation is on the whole simpler and uses less power, primarily because of the low baseband frequency.

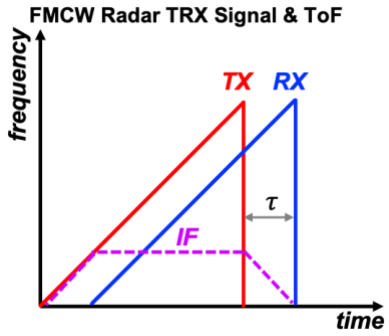


Figure 4.5 FMCW Radar RToF measurement concept

2) **Pulsed Radar:** This approach measures the RToF in the time domain by transmitting a short duration pulsed tone (typically <1ns) and calculating the time delay between the transmit pulse and the return pulse waveforms [102], Figure 4.6. Pulsed radar resolution is proportional to pulse duration, calling for very short pulses for improved ranging resolution. Another attribute of the pulsed radars is their relatively large IF bandwidth, which is equal to the pulse bandwidth, which can be power-hungry for high resolution applications.

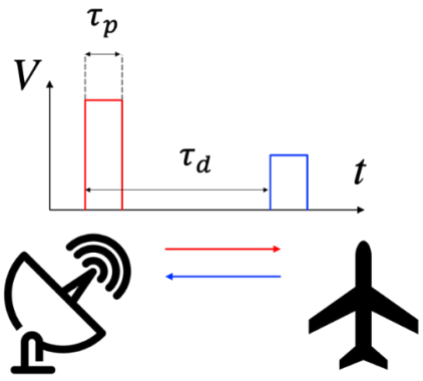


Figure 4.6 Pulsed radar basic operation

4.4.8 Visible light

The Visible Light Communication (VLC) technology [103] is a fast and cost-effective method of transmitting data by using visible light between 400THz and 800THz, primarily modulated and emitted by Light Emitting Diodes (LEDs). Localization techniques based on visible light use light sensors to locate and track LEDs. By using the LEDs (which behave like iBeacons), they are able to transmit a signal that can be picked up by the receiver/sensor to help locate sensor nodes. AoA is generally regarded as the most accurate localization method for visible light [103] [104]. One of the advantages of visible light based localization is its wide dissemination (perhaps even more widespread than WiFi). One of the fundamental limitations of this scheme is that line of sight between the LED and the sensor(s) is required. Another major drawback of this method is the additional costs associated with light sensor in the WSNs.

4.5 Case Study: FSK Phase-Based Ranging

As discussed earlier, energy efficiency plays a vital role in massive IoT networks with millions of connected WSNs, since utilizing batteries in such immense scale is not feasible or cost-efficient. Thus, it is imperative to develop an energy-cautious design methodology for ranging and localization circuits in massive IoT networks, which is empowered by deep understanding of the design trade-offs. In this section, a closer look is taken into phase-based ranging which is embedded in an FSK-modulated radio. The circuit implementation

requirements along with the effect of the receiver circuit's non-idealities on the ranging performance is studied and simulated.

4.5.1 Operating Principle

As shown in Figure 4.7, in an FSK ranging scheme two slightly shifted tones, $f_c \pm \Delta f$, are sequentially transmitted from the node side and received by the anchor. The phase-synchronized receiver can down-convert and extract the phase information in the tones:

$$\theta_i = (-1)^i \, 2\pi\Delta f \frac{r}{c} + 2\pi f_c \frac{r}{c} \quad (i = 1, 2)$$

Where c is the speed of light and r is the distance between the asset and the anchor. Thus, r can be inferred from the phase difference between the two tones:

$$\Delta\theta = \theta_2 - \theta_1 = 4\pi\Delta f \frac{r}{c}$$

$$r = \frac{c \, \Delta\theta}{4\pi\Delta f}$$

From the above equation, it is surmised that the maximum range unambiguity in FSK ranging does not depend on f_c and solely depends on FSK bandwidth, which is: $c/(2\Delta f)$.

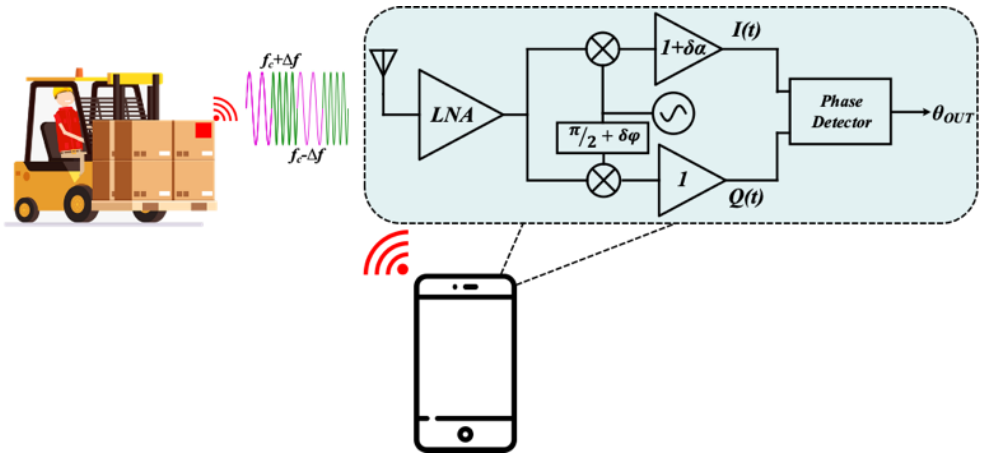


Figure 4.7 Asset tracking through FSK ranging

In order to quantify the ranging error performance, the Cramer-Rao Lower Bound (CRLB) for FSK phase-based ranging is defined as [105]:

$$\sigma_d \geq \frac{c}{2}\sqrt{\frac{1}{8\pi^2(f_c^2+\Delta f^2)\,SNR\;2\Delta f\;T_0}}$$

Where *SNR* is the baseband signal-to-noise ratio and T_0 is the duration of signal observation window, which is assumed to be $1/(2\Delta f)$ for the rest of the thesis.

4.5.2 Receiver Design Trade-Offs

In energy-constrained applications such as ranging in WSNs, usually receiver performance is exchanged for lower power consumption. However, degraded receiver performance affects the baseband SNR adversely and will corrupt ranging accuracy. Thus, understanding the design trade-offs in FSK receivers and their effect on ranging accuracy is a key enabler of ULP design for high accuracy ranging applications in IoT networks. The effect of FSK receiver nonidealities on BER performance is discussed in [106]. Below, the impact of various receiver nonidealities on baseband noise and SNR is discussed and finally a relation between phase-based ranging CRLB and receiver impairments is explored.

1) **Receiver Noise:** The receiver's noise is added to the signal along the receive chain and contributes to baseband SNR degradation. Assuming the FSK symbol rate is R_b, carrier-to-noise ratio (CNR) is ρ, and the receiver's noise factor is F_{RF}, the resulting noise power is:

$$P_{n,RF} = \frac{R_b^2}{\rho}F_{RF}$$

2) **Phase Noise:** The LO phase noise (PN) can be traded for higher energy-efficiency in ULP radio design and directly impacts the receiver performance. Thus, the influence

should be understood deeply to achieve the best performance without giving up energy-efficiency. The noise power contributed to the baseband signal by LO PN is a function of data-rate (R_b), PN ($\mathcal{L}\{\omega_{offset}\}$), PN offset frequency ($\omega_{offset}$), and a constant value (K_0):

$$P_{n,PN} = \omega_{offset}^2 10^{\frac{\mathcal{L}\{\omega_{offset}\}}{10}}(R_b + K_0)$$

3) ***IQ* Mismatch:** The imbalance in the *I* and *Q* paths in the receiver further deteriorates the output SNR by contributing to the receiver's output noise. If the gain and phase mismatch in the *I* and *Q* paths are $\delta\alpha$ and $\delta\varphi$, respectively, the degraded receiver noise can be quantified as:

$$P_{n,RF,imbalance} = \frac{R_b^2}{\rho} F_{RF} \frac{1 + (1+\delta\alpha)^2}{2(1+\delta\alpha)\cos(\delta\varphi)}$$

To better understand the trade-offs between receiver specifications–such as noise, *IQ* imbalance, and LO phase noise–and output SNR, we unify the output SNR equation. The total output noise power is the sum of the last two equations:

$$P_{n,total} = \frac{R_b^2}{\rho} F_{RF} \frac{1 + (1+\delta\alpha)^2}{2(1+\delta\alpha)\cos(\delta\varphi)} + \omega_{offset}^2 10^{\frac{\mathcal{L}\{\omega_{offset}\}}{10}}(R_b + K_{LO})$$

For the purpose of simplicity, if assumed *I* and *Q* signal paths in the receiver match perfectly, the overall SNR can be calculated as:

$$SNR = \frac{P_{SIG}}{P_{n,total}} = \frac{(2\pi\Delta f)^2}{\omega_{offset}^2 10^{\frac{\mathcal{L}\{\omega_{offset}\}}{10}}(R_b + K_{LO}) + \frac{R_b^2}{\rho} F_{RF}}$$

By substituting the equation above into the CRLB equation, depending on the significance of the noise contribution from each of the RX non-idealities, the relationships between

phase-based ranging CRLB and design parameters can be summarized as shown in Table 4.1.

Table 4.1 Summary of CRLB dependence on receiver design parameters

Design Parameter	**Dominant Noise Source**	
	RX Thermal Noise	***Phase Noise***
Data Rate	CRLB $\propto R_b$	CRLB $\propto \sqrt{R_b}$
Noise Factor	CRLB $\propto \sqrt{F_{RF}}$	Independent
CNR	CRLB $\propto \rho$	Independent
Phase Noise	Independent	CRLB $\propto \sqrt{10^{\frac{\mathcal{L}\{\omega_{offset}\}}{10}}}$

4.5.3 Simulation Results

In order to better understand and visualize the previously discussed trade-offs in FSK receiver design for ranging, MATLAB simulations have been performed simulating CRLB based on the equations discussed in the previous section along with the specifications summarized in Table 4.2. Figure 4.8 shows the simulated CRLB vs. symbol rate and PN for the discussed model. As implied in Table 4.1, when the receiver performance is limited by thermal noise, *i.e.* the left region on the plot, CRLB $\propto R_b$. On the right side of the plot on Figure 4.8, where the RX performance is PN limited, CRLB $\propto \sqrt{R_b}$. LO PN is directly related to the receiver's power consumption, thus the PN in ULP receivers shall not be ignored by the designer. For instance on Figure 4.8, for a fixed CRLB requirement, the designer can give up ranging latency to achieve lower power consumption by halving the symbol rate on design point A and choosing a 3dB worse LO phase noise to reach design point B.

Table 4.2 Simulation parameters

Design Spec	Value
F_{RF}	10
f_c	915MHz
Δf	1MHz
R_b	2Mbps
CNR	30dB
$\mathcal{L}\{\omega_{offset}\}$	–120dBc/Hz
ω_{offset}	500kHz

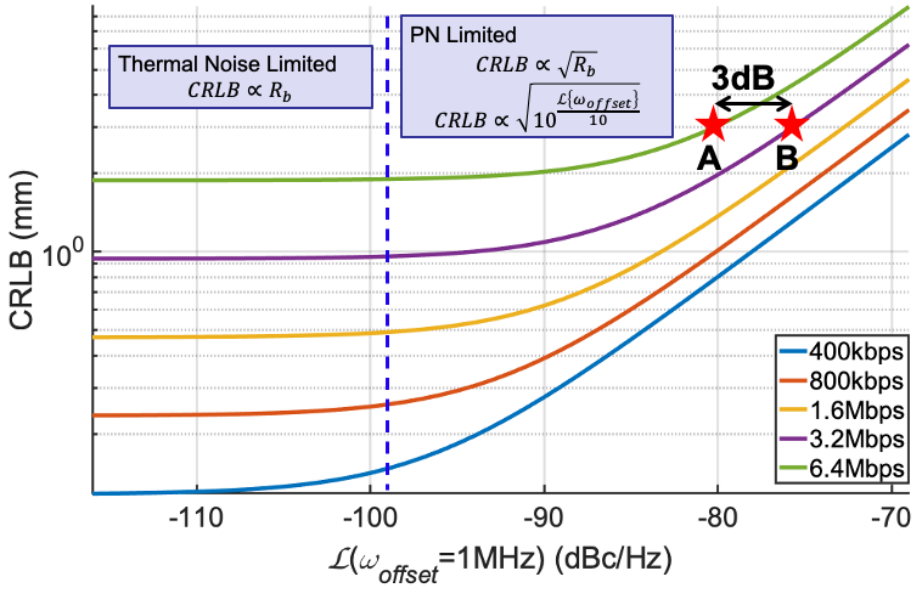


Figure 4.8 FSK phase-based ranging CRLB vs. RX phase noise for different symbol rates

Furthermore, the ranging CRLB was simulated vs. a receiver's noise figure (NF) and CNR, as shown in Figure 4.9. The plot consists of two major regions: thermal noise limited region on the left and phase noise limited region, on the right side. It can be deduced from Figure 4.9 that for ULP receiver design in the thermal noise limited region, in which achieving low RX NF is challenging given the limited power budget, the performance burden on the

battery-powered ULP receiver can be shifted to the IoT gateway transmitter, by trading RX NF for CNR 1dB/1dB.

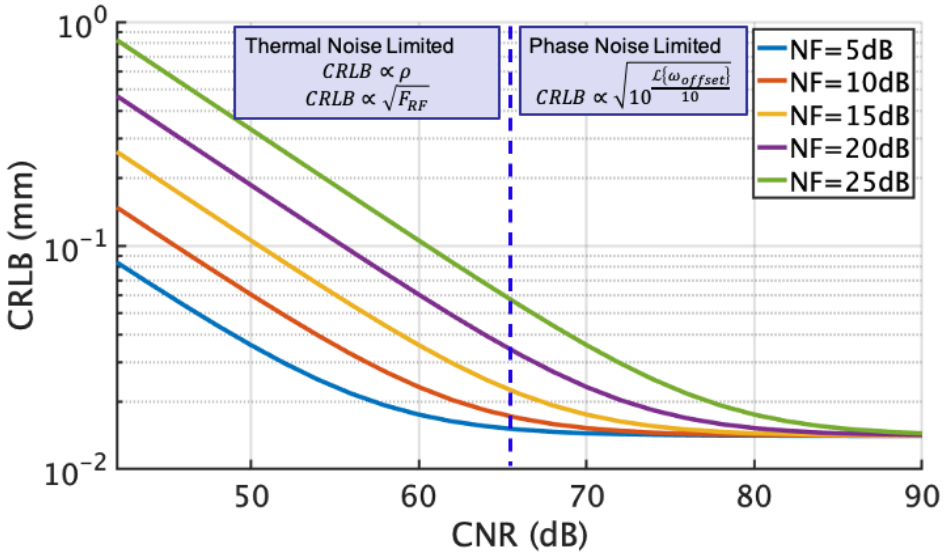


Figure 4.9 FSK phase-based ranging CRLB vs. CNR for different RX noise figure values

Most importantly, receiver NF and PN are directly in trade-off with power dissipation. Thus, in ULP ranging applications, it is essential to have an in-depth understanding of the ranging performance relation with RX PN and NF, and ensure maximal energy-efficiency for a desired CRLB requirement by avoiding overdesigning and comprehending the noise contributors limiting the ranging performance. Figure 4.10 shows the simulated CRLB for different PN and NF values, along with the regions in which highlights the dominant noise contributor.

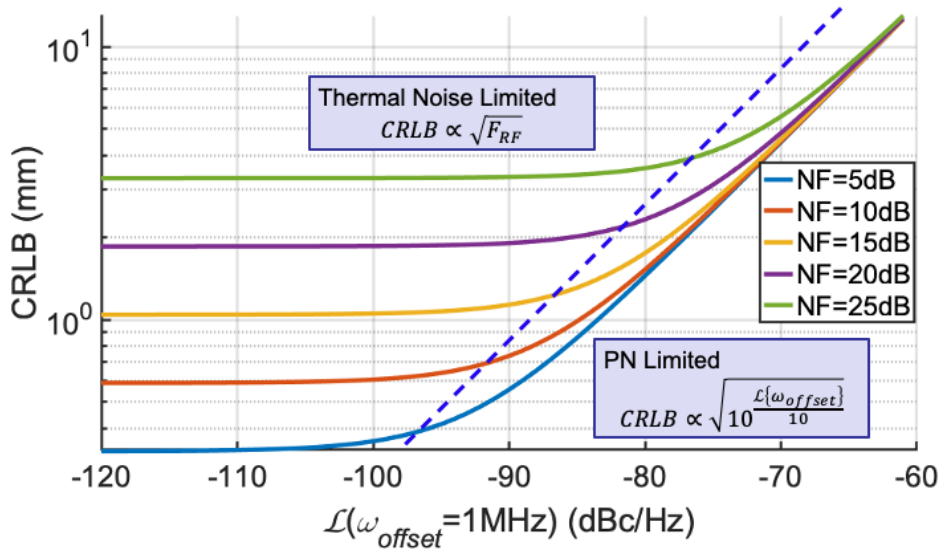


Figure 4.10 FSK phase-based ranging CRLB vs. RX phase noise with different noise figure values

4.6 Summary and Comparison

The following section summarizes the discussions on the previous sections of the different techniques and technologies for ranging and localization. In Table 4.3 we compare the various aspects of the presented technologies with an emphasis on adoption in the IoT realm. Radar ranging schemes fail to scale flexibly due to their large bandwidth requirement along with their relatively high operating frequency, which necessitates higher current consumption in the sensor nodes. Moreover, due to their dependence on additional modules for wireless communication in the WSN, they cause a cost overhead, which prevents the WSNs from being widely adopted.

Bluetooth can potentially be an optimum solution for the IoT networks due to its wide adoption by the users and its comparatively low power consumption compared to the other wireless standards.

Despite its widespread adoption, WiFi is not suitable for energy-restricted WSNs due to the fairly high power consumption, complex modulation scheme, and low accuracy.

LPWAN technologies such as LoRaWAN and NB-IoT could be attractive options for long-range applications. However, NB-IoT is the better choice due to its compatibility with the LTE infrastructure and better scalability, compared with LoRaWAN.

Table 4.3 Summary and comparison table

Technology	**Technique**	**IoT Compatibility**					
		Energy-Efficiency	Communication capability	Scalability	Added Infrastructure	Max Range	Accuracy
Bluetooth	RSSI	✓	✓	✓	✗	100m	~1m
Bluetooth	AoD	✓	✓	✓	✗	100m	~1m
Bluetooth	AoA	✓	✓	✓	✗	100m	~1m
WiFi	RSSI	✗	✓	✓	✗	50–100m	~1m
WiFi	AoA + RSSI	✗	✓	✓	✗	50–100m	~50cm
UWB	TDoA	✓	✓	✓	✓	40m	~30cm
NB-IoT	RSSI	✗	✓	✓	✗	1km/10km	N/A
LoRaWAN	RSSI	✓	✓	✓	✓	5km/15km	~400m
FMCW Radar	RToF	✗	✗	✗	✓	<100m	~5cm
Pulsed Radar	RToF	✗	✗	✗	✓	<100m	~5cm
Visible Light	AoA	✗	✗	✓	✓	<10m	~50cm

Chapter 5:

A 50mW Fully-Integrated PLL-Less Millimeter-Scale 60GHz FMCW Radar Transceiver in BiCMOS 130nm

5.1 Introduction

It is almost certain that the IoT will not achieve the lofty projections on the timeline initially made. Early expectations in 2012 of over one trillion connected devices by 2020 has reduced to an estimate of less than 2.5 billion in recent studies [107]. A major reason for this decrease is the power consumption of wireless sensors has failed to scale fast enough. While some sensors have just begun to reach the ultra-low power class, such as temperature and pressure sensors [13], ranging and velocity sensors have failed to do so, despite their enormous potential in wireless telemetry IoT solutions, including applications in autonomous driving, smart city, health-care, consumer goods, security, and defense. However, several challenges have traditionally made the design of low-power sensors difficult, and thus slowed down their widespread adoption into these fields. First, to achieve high resolution detection, mm-wave transmission must be used, for which very few low-power techniques exist. Second,

extensive back-end signal processing is generally required, which must be done off-chip, limiting integration size. Finally, no end-to-end system approach exists for energy-efficient and miniature-sized wireless sensors, making each design custom and expensive. A mm-scale, energy-efficient, wireless ranging sensor capable of operating ranging for IoT applications would result in an increased number of IoT devices.

During the past decade, mm-wave radar sensors have been increasingly investigated for short range sensing applications such as gesture recognition, automotive radars, occupancy detection, and health monitoring [108] [109] [102]. However, due to their larger than cm-scale form factor and high-power consumption, these solutions fail to fit into the demands of the new generation of emerging massive IoT networks.

Although the previous work on mm-wave radars and IoT sensors have achieved appealing performances, there is not a comprehensive, fully integrated end-to-end solution with high energy efficiency which fills the gap between these two areas and fits into the continuously growing IoT market. In this chapter, we have proposed and designed a compact, fully integrated, energy-efficient mm-scale range sensor.

In order to comply with mm-scale size limitation for IoT sensor nodes and achieve high detection resolution, *i.e.* bandwidth, an efficient, mm-wave radar is introduced. So as to maximize the efficiency, a Frequency Modulated Continuous Wave (FMCW) radar has been proposed, due to its following unique features:

1) **Constant Envelope Modulation:** Since FMCW is a constant-envelope modulation, the transmitter linearity requirement is relaxed, enabling transmitter design with

enhanced efficiency, primarily because using non-linear power amplifiers are feasible for this modulation scheme.

2) **Simple Modulation:** Unlike pulsed or Ultra-Wide-Band radars, which require very narrow pulses in the time domain to achieve high resolution (tens to hundreds of pico-seconds), FMCW radars have a relatively simple modulation scheme involving a continuous linear chirp signal, hence can be generated using an open-loop scheme.
3) **Low IF Bandwidth:** Pulsed radars commonly require several GHz of IF bandwidth and consume high active power, whereas FMCW radars commonly have limited IF bandwidth (~100kHz to tens of Mega-Hertz for short range radars), allowing for much less power dissipation in the FMCW receiver's IF chain.

5.2 Fundamentals of FMCW Radar

FMCW radars operate based on observing a target's round-trip time-of-flight (t_d), as show in Figure 5.1. The transmitter sends out a linear chirp which is delayed and reflected back by a target. One can detect the target distance by measuring target time of flight from the resulting beat frequency, f_{IF}:

$$f_{IF}(t) = f_{TX}(t) - f_{RX}(t) = f_{TX}(t) - f_{TX}(t - t_d) = f_0 \propto t_d$$

$$f_{IF} = \frac{2d_{target}}{c} \times \frac{BW_{chirp}}{T_{chirp}}$$

Where d_{target} is target distance, c is the light speed, BW_{chirp} is the chirp bandwidth, and T_{chirp} is chirp period. Provided that the transmitted chirp is linear in time, the beat frequency is constant, hence generating a low-frequency tone in the baseband.

Moreover, the range resolution (Δd) of the FMCW radar depends on the transmitted chirp bandwidth:

$$\Delta d = \frac{c}{2BW_{chirp}}$$

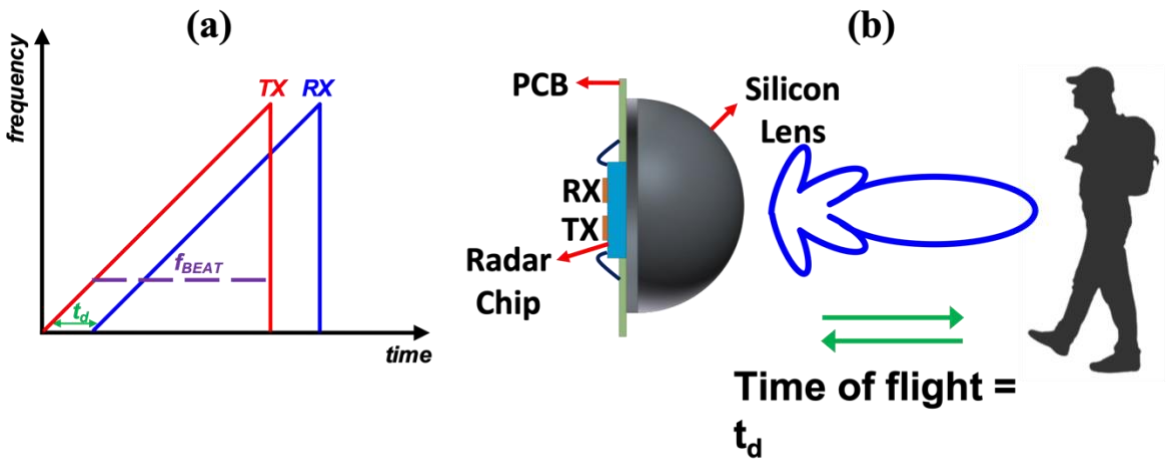


Figure 5.1 (a) FMCW radar operation principle by comparing TX and RX chirps. (b) View of radar detection system on top of a silicon dielectric lens, detecting a target.

PLLs are commonly adopted to generate linear chirps [110], but their implementation is power-hungry and not suited for cubic-mm sensors. Another approach to overcome the issue is pre-distorting the VCO to compensate for non-linearity in the VCO profile [111] [112]. Nonetheless, this method requires a high performance digital-to-analog converter, which is not in harmony with an energy-efficient system solution.

5.3 Effect of Chirp Non-Linearity

As discussed in the previous section, with a perfectly linear chirp being transmitted and received in the FMCW radar, a low-frequency tone will be generated at IF. In this section, we will look into the effect of nonlinearities in chirp generation and its implications on the IF signal. In case of a linear chirp:

$$f_{TX}(t) = a_0 + a_1 t \;\rightarrow\; f_{IF}(t) = f_{TX}(t) - f_{TX}(t - t_d) = a_1 t_d$$

In this case, the phase of the IF signal, which is a tone, is changing linearly with time:

$$\phi_{IF}(t) = 2\pi \int f_{IF}(\tau)\, d\tau = 2\pi(a_1 t_d)t + \alpha_0$$

As can be seen, the phase of the IF tone is linearly related to time in case of a linear chirp. Next, let's assume the transmitted chirp has a nonlinearity (consider second order polynomial for simplicity), the TX chirp signal could be written as:

$$f_{TX}(t) = a_0 + (a_1 + a_2 t)t$$

And thus, the IF signal can be written as:

$$f_{IF}(t) = f_{TX}(t) - f_{TX}(t - t_d) = (a_1 + a_2 t)t_d$$

In this scenario, the IF beat frequency is no longer a clean tone and it is spread in the spectrum. In this specific case of quadratic chirp nonlinearity, the resulting IF signal is a linear chirp itself, Figure 5.2. This chirp nonlinearity, which in most cases stems from the

VCO, degrades the target range detection accuracy. Thus, achieving a linear chirp for an FMCW radar is vital for an accurate radar system.

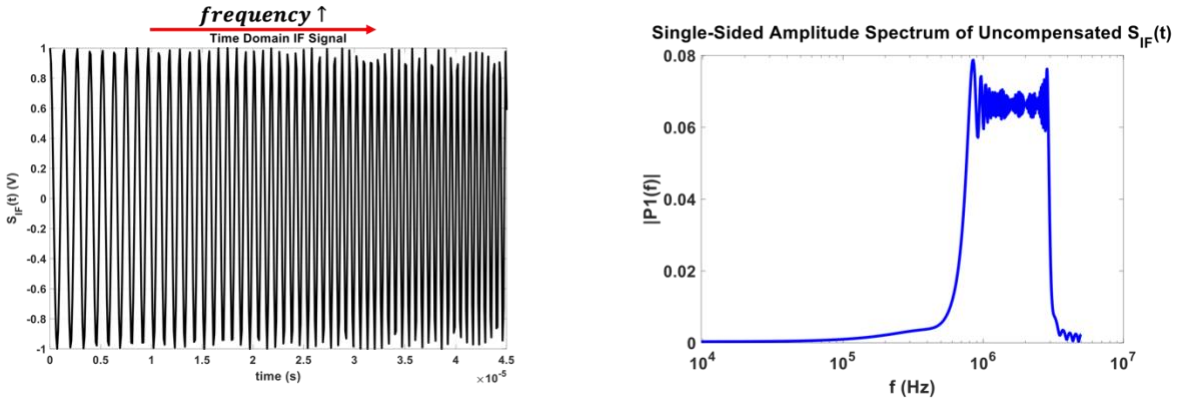


Figure 5.2 Effect of chirp nonlinearity on IF signal in transient and frequency domain

5.4 Chirp Nonlinearity Correction

From revisiting the equations in the previous section, the IF signal's phase can be written as:

$$\phi_{IF}(t) = 2\pi \int f_{IF}(\tau)\, d\tau = 2\pi t_d(a_1 t + a_2 t^2) + \alpha_0$$

With the nonlinear chirp, the IF signal's phase is no longer changing linearly with time and has a quadratic relation in this specific case. In [113] it was shown that chirp nonlinearity can be compensated using software post-processing, by re-sampling the IF signal in such a manner that the phase of the spread IF signal follows that of a tone. If we compare the IF signal's phase in case of a linear and a nonlinear chirp signal at their sampling instances–T_s and T_s', respectively–and equate them:

$$\phi_L[n] = 2\pi t_d a_1 n T_s,\ \phi_{NL}[n] = 2\pi t_d(a_1 + a_2 n T_s')n T_s'$$

$$2\pi t_d a_1 n T_s = 2\pi t_d(a_1 + a_2 t)t$$

Now if we solve for *t* (on the right side), we can calculate the new sampling instances such that the phase of the re-sampled IF signal imitates that of a tone signal at IF and thus be able to de-spread the IF signal in the frequency domain, Figure 5.3.

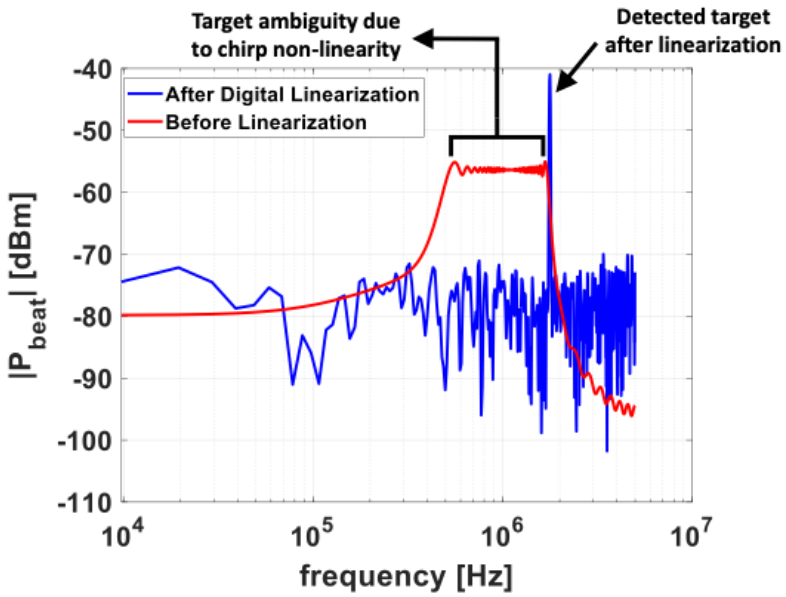


Figure 5.3 IF signal spectrum before and after nonlinearity correction

This method has been leveraged in [114] for THz imaging, but has a few shortcomings. First, the system is not fully integrated and requires off-chip software processing. Second, the nonlinear compensation algorithm is complex, requiring a powerful processor to compute. Third, the targets are detected via Fast Fourier Transform (FFT), which similarly requires too much computing power for a low power integrated solution. This limits the flexibility of the design to be adopted in massive IoT sensor ecosystems.

The objective of this work is to address all of the current shortcomings in previous FMCW sensors by adopting a system, circuit, and antenna co-design to build an end-to-end radar system with significantly lower power dissipation compared to the state of the art.

5.5 System Architecture

A block diagram of the proposed FMCW transceiver is shown in Figure 5.4. A nonlinear chirp is generated using an open loop VCO, which is divided between the transmitter's power amplifier (PA) and the LO buffer stage driving the mixer switches, using a Wilkinson power divider. A single-ended PA transmits the chirp signal through an on-chip single-ended slot antenna. The transmitter and receiver are simultaneously active in the FMCW radar, which results in significant leakage from the transmitter to the receiver, and the RX RF frontend constantly experiences an in-band blocker, which generates a low-frequency blocker term at the IF. A passive mixer-first receiver architecture was adopted for enhanced linearity and low-power consumption, followed by a bandpass filter and IF amplifier stages that attenuate the undesired low-frequency components from the TRX coupling and amplify the desired signals.

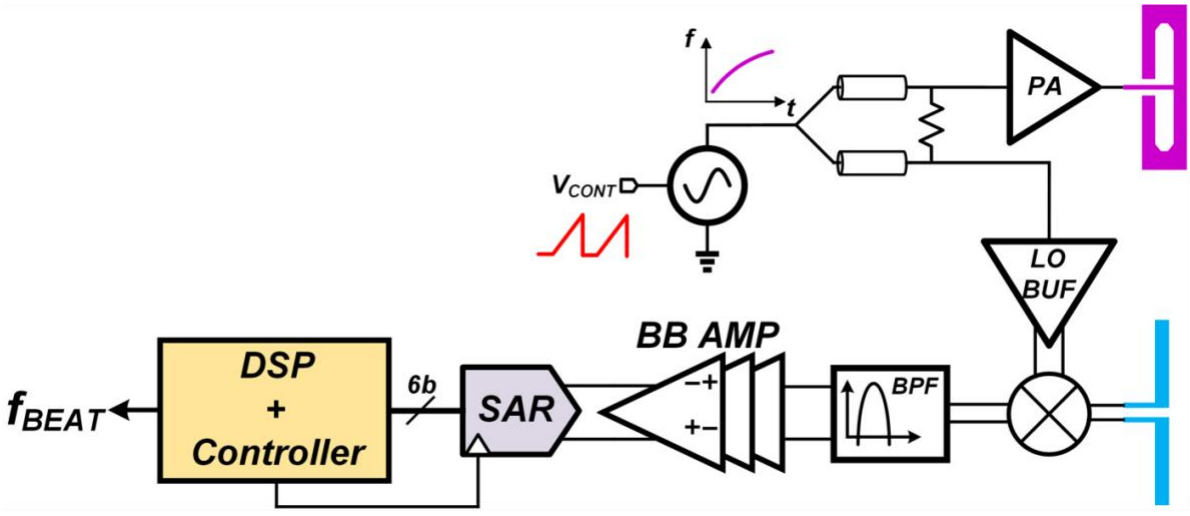


Figure 5.4 FMCW transceiver block diagram

The analog IF output is then quantized through a 6-bit SAR ADC. In the proposed FMCW transceiver, the IF signal re-sampling is implemented at the ADC to correct for chirp nonlinearity, where the ADC's sampling clock is gated by a DSP controller to select the appropriate IF samples. Through the application of ADC-assisted chirp nonlinearity compensation scheme, the distorted IF signal spectrum is reconstructed and an IF tone is recovered for target detection. The final step of the process consists of extracting the tone frequency of the compensated IF signal for range determination using an integrated and power-efficient DSP unit.

5.6 Low-Power Circuit Design

The mm-wave and low frequency blocks in the FMCW transceiver were designed with the main goal of power efficiency, while satisfying the desired performance metrics such as transmit power, RX noise figure, and RX linearity. A 130nm BiCMOS process was chosen for this design to leverage high f_T/f_{MAX} values in BJT devices for enhanced current efficiency at mm-wave for power generation and amplification. In the following sections, the design of the transmitter and the receiver blocks are discussed in detail, respectively.

5.6.1 Transmitter Design

A schematic diagram of the transmitter is shown in Figure 5.5. The transmission starts with chirp synthesis with a bandwidth larger than 4GHz. At mm-wave frequencies, the Colpitts oscillator has a wider tuning range compared to the other commonly used topologies, which is primarily due to the smaller parasitic capacitance contribution of the active devices to the

LC-tank [115]. For that purpose, a differential Colpitts VCO with a wide tuning range and a supply voltage of 3V was designed. Additionally, to enhance the power-efficiency, a current-reused cascode common-base buffer is designed, which amplifies the VCO output and isolates the resonant tank from the output loadings. Moreover, due to short range operation, the VCO phase noise requirement is relaxed in FMCW radars [116] (PN<-70dBc/Hz at 1MHz offset in this design), freeing room to trade phase noise with power efficiency. The nonlinear chirp is generated by feeding a ramp signal with a period of 100μs to the VCO's control voltage. One side of the differential VCO was connected to a GSG pad for testing and characterization purposes, while the other side was connected to a Wilkinson power divider which feeds the LO buffer and PA stages.

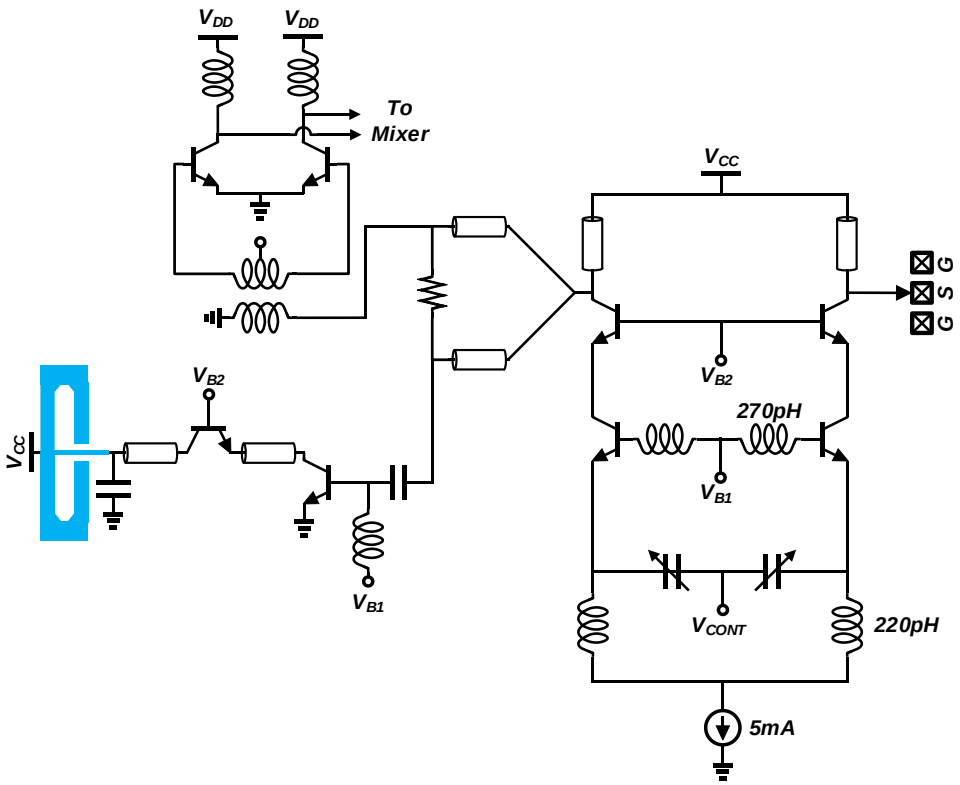


Figure 5.5 FMCW transmitter schematic diagram

Radars using FMCW technology use chirp modulation, a constant-envelope modulation that does not have strict linearity requirements. This implies the possibility of adopting nonlinear PA classes with substantially higher Power Added Efficiency (PAE). In order to obtain adequate power gain and PAE with minimum area overhead, a single stage cascode class B power amplifier stage using a 3V supply was designed. The PA was designed for an output power >4dBm and a power gain better than 12dB in the linear region, across the 58GHz–63GHz frequency band. Lastly, to ensure maximum Equivalent Isotropically Radiated Power (EIRP) at the transmitter output, an on-chip single-ended slot antenna was co-designed with the PA stage.

Finally, a differential buffer stage using a common-source topology was designed to amplify the generated chirp and drive the mixer switches on the receiver. The buffer stage was designed using a 1.2V supply voltage and leverages a balun at the input for single-ended to differential conversion.

5.6.2 Receiver Design

This section focuses on co-design of RX antenna and a mixer-first receiver chain to minimize power consumption without sacrificing noise and linearity performance. While using an LNA as the first stage provides superior noise performance, compared to a passive-mixer-first architecture, it suffers from poor RX linearity and can cause severe degradation to system operation due to the strong in-band leakage from the TX antenna. Thus, a passive mixer first architecture is designed to achieve high linearity low noise figure, and efficient filtering of leakage from TX antenna. A schematic diagram of the designed

receiver is visualized in Figure 5.6. A double-balanced passive mixer was co-designed with an on-chip dipole antenna to enable fully differential operation and optimum receiver noise figure over the 58GHz–63GHz frequency band. To enable robust operation with 5m of maximum range, a receiver noise figure better than 20dB was desired.

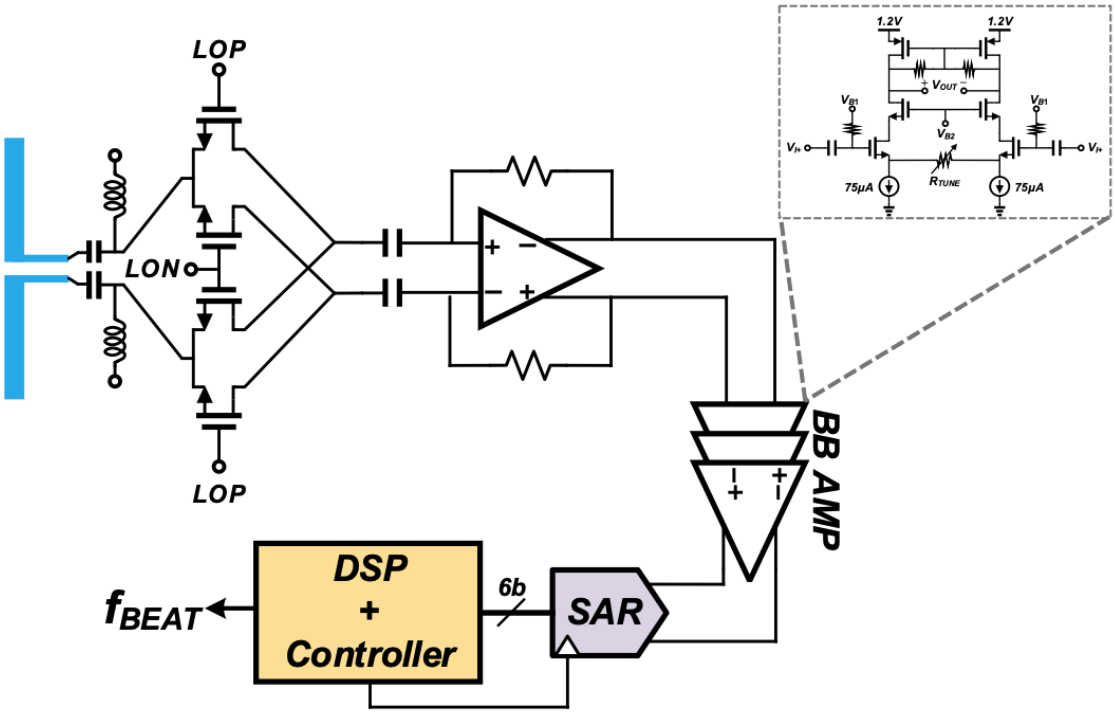


Figure 5.6 Schematic diagram of the FMCW receiver

Immediately after the mixer stage, a high-pass filter stage was employed to eliminate the low-frequency terms caused by the undesired TX to RX antenna leakage, followed by three amplifier stages with programmable gains from 40dB–80dB. The IF bandwidth is dictated by the chirp's ramp rate as well as the maximum range which the FMCW transceiver is supposed to measure successfully. In this design, a maximum range of 5 meters was desired,

resulting in a maximum IF frequency of 5MHz, thus the IF amplifiers were designed with a passband from 200kHz–5MHz.

A differential 6b asynchronous SAR ADC with a sampling frequency of 10MHz and clock gating was employed to compensate for the chirp nonlinearity at baseband. In addition, to implement the chirp nonlinearity correction DSP with minimal power and area overhead, the nonlinearity correction mechanism was co-designed with the VCO. In this step, the VCO was designed carefully with sufficient bandwidth such that the nonlinearity in the VCO's frequency vs control voltage profile is concave in the frequency band of interest.

5.7 Circuit Simulation Results

The FMCW transceiver chip was design and taped out in a 130nm BiCMOS process, Figure 5.7, and occupies 4.84mm^2 area–including the on-chip TX and RX antennas.

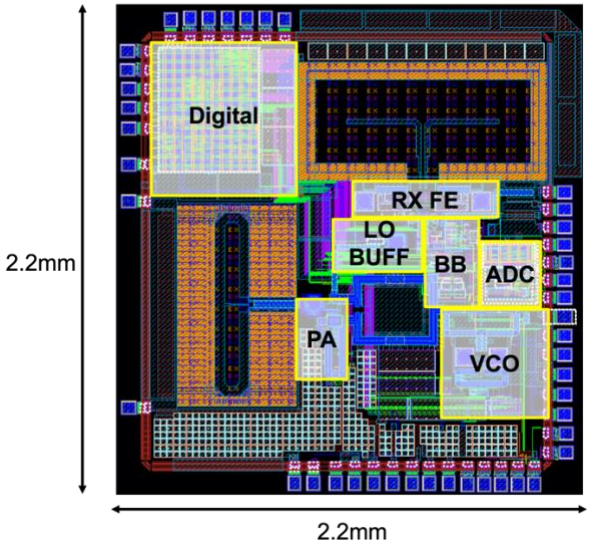


Figure 5.7 FMCW transceiver chip layout

The mm-wave circuit blocks in this chip were designed and simulated with their layout parasitics extracted in Cadence and HFSS, for the active p-cells and passive structures, respectively. Based on the simulation results for the VCO, the oscillation frequency changes from 58GHz–64.5GHz when sweeping VCO control voltage from 0.5V-2.6V, Figure 5.8.

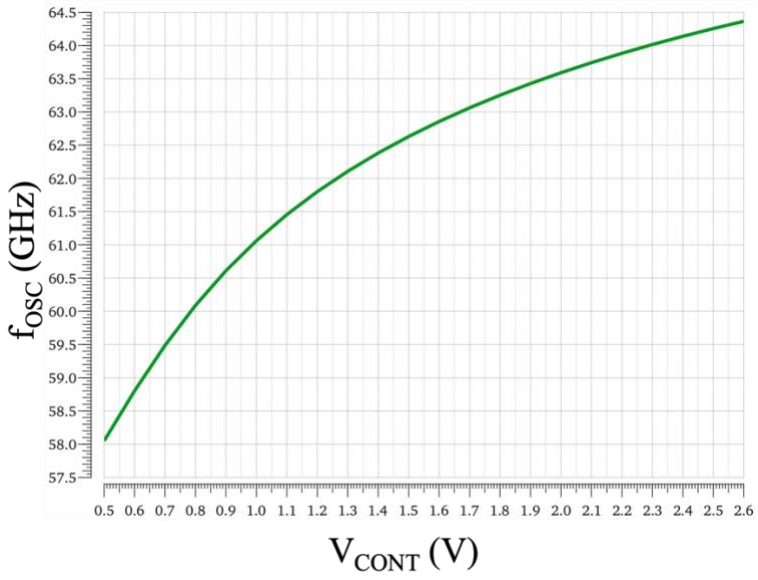


Figure 5.8 Colpitts VCO output frequency vs control voltage

Moreover, according to the simulations the Colpitts VCO has an output power higher than -1.4dBm across the 58GHz–64.5GHz frequency band, while consuming 20mW active power from a 3V supply, Figure 5.9. Additionally, based on HFSS simulations, the Wilkinson power divider has 0.5dB extra insertion loss, which does not significantly affect the transmitter efficiency since it is before the PA stage.

The PA stage was simulated in cadence with its parasitics extracted in HFSS. According to the post-layout simulation results, which include the antenna, the PA consistently provides an output power greater than 4.5dBm with 14dB gain in the linear region across the 55GHz–

63GHz frequency band, with a peak PAE of 20% and 18mW power consumption, Figure 5.10.

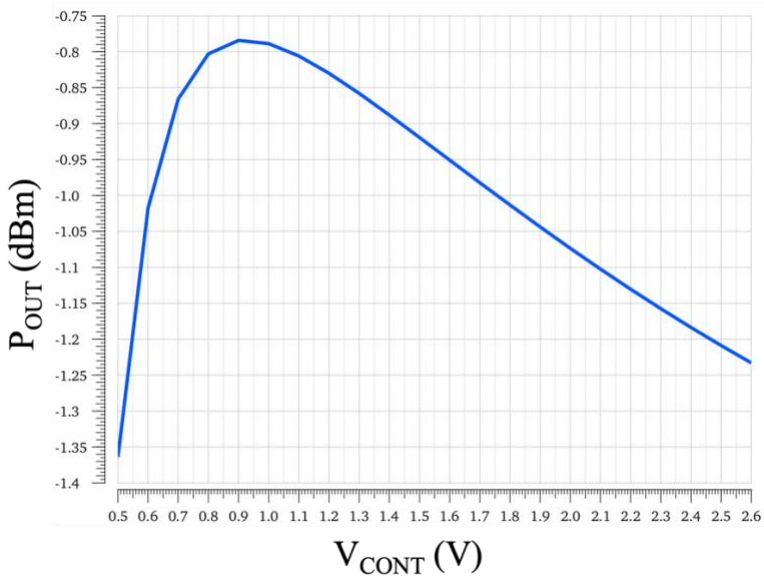


Figure 5.9 VCO output power across the tuning range

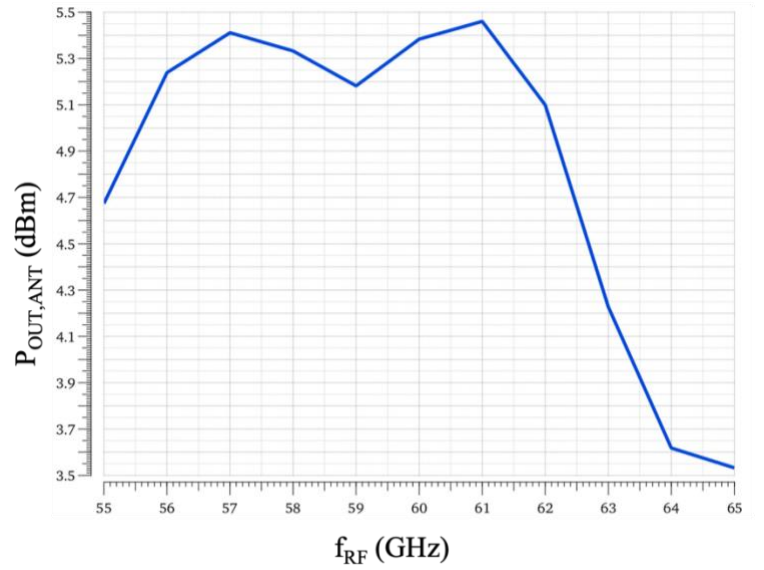


Figure 5.10 Power amplifier output power vs center frequency

The LO buffer stage consumes 4.5mW of active power from a 1.2V supply, while providing 6dB power gain and 0dBm output power.

The RF frontend was simulated along with the dipole antenna, resulting in 18dB noise figure and input IIP_3 of -13dBm. The IIP_3 spec is primarily mandated by the PA output power and the coupling between the TX and RX antennas. With 4.5dBm output power and 20dB isolation between the TRX antennas, the designed RX will have an additional 2.5dB margin for linearity.

Finally, a power consumption breakdown of the designed FMCW chip is shown in Figure 5.11. As expected, a major portion of the power consumption is dedicated to mm-wave power generation and amplification in the VCO and PA stages.

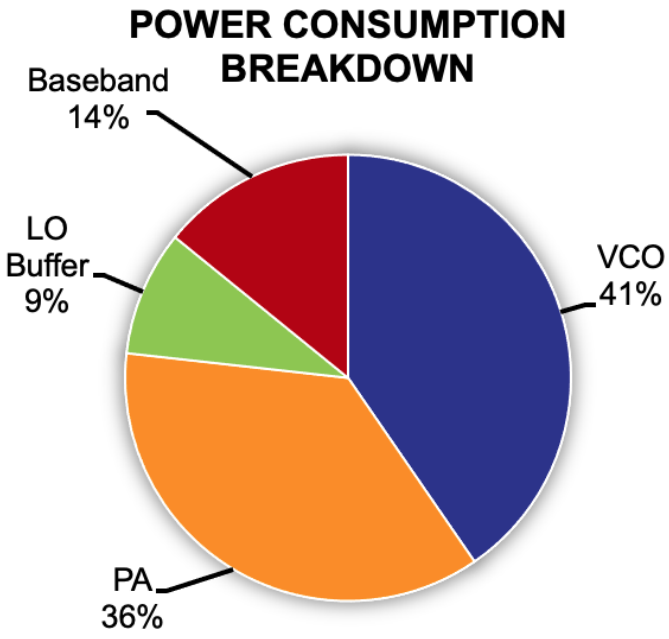


Figure 5.11 FMCW transceiver power consumption breakdown

5.8 Antenna Design and Simulation

According to state of the art, a typical on-chip antenna operating at 60GHz achieves only 10% efficiency and -4.4dBi gain [117], due to the various loss mechanisms in the silicon substrate, such as low electric resistivity (~10Ω.cm) and high dielectric constant (ε_r=11.9), Figure 5.12. In this design, we have designed a dipole and a slot antenna for the fully-integrated FMCW transceiver. A dipole antenna has been used for the receiver because of its low input impedance at resonance frequency (~75 Ω) and differential feed, which is suitable for low-noise differential receivers. Similarly, a slot antenna has been opted for the transmitter due to its compact size, compared to patch antennas, and single-ended feed, to be simply fed by the single-ended PA stage.

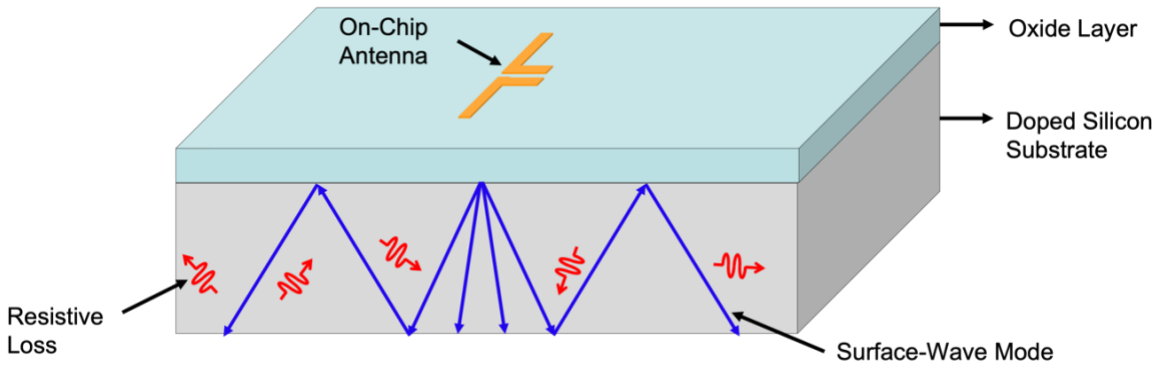
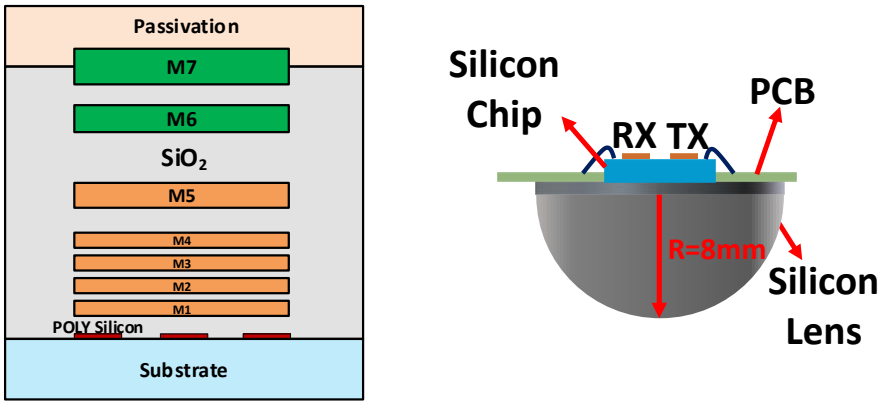


Figure 5.12 Electromagnetic wave loss mechanisms in silicon substrate

In Figure 5.13 the cross section view of the 130nm technology metal stack is shown. The slot antenna is designed using M1-M7 and occupies 1030µm×630µm, including the surrounding ground plane.



(a) (b)

Figure 5.13 (a) 130nm BiCMOS process cross-section view, (b) High resistivity silicon dielectric lens attached to chip backside

The RF feed is composed of M7, while M1-M7 are utilized and connected using arrays of metal vias in the optimally-sized ground plane to maximize radiation efficiency. The dipole antenna occupies 1315µm×624µm and only uses the top metal layer (M7). Furthermore, in order to suppress the undesirable coupling between TX and RX, the dipole antenna is shielded with a ground plane using M1-M7 metal layers. The dipole antenna is horizontally polarized, while the slot antenna is vertically polarized. Therefore, the TX and RX antennas should be placed orthogonally in order to maintain their polarization matching. Moreover, in order to suppress the lossy substrate modes, we have attached the silicon substrate to a high resistivity silicon dielectric lens, Figure 5.13. Finally, in order to maximize the gain of both antennas and the isolation between TX and RX antennas simultaneously, the position of TX and RX antennas on the chip has been optimized in HFSS. The overall 3D geometry, including the on-chip antennas and the silicon lens is shown in Figure 5.14.

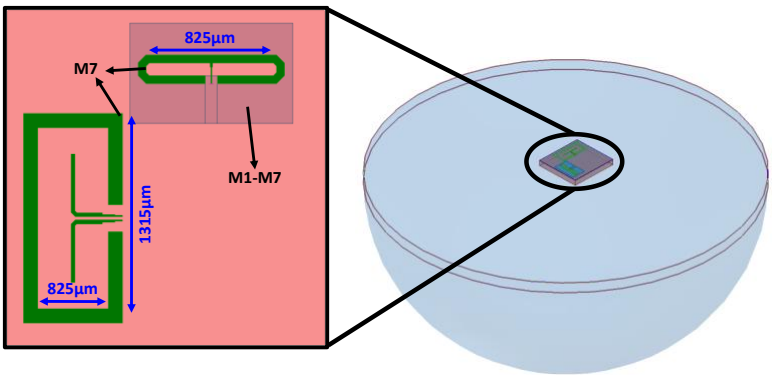


Figure 5.14 HFSS geometry 3D model including the chip and silicon lens.

ANSYS Electronics Desktop is used for the design and optimization of the antennas. Using the aforementioned dimensions, resonant frequency of the slot antenna is found to be 60GHz with approximately 6.75GHz bandwidth (11.25%). The proposed geometry provides 150Ω input impedance (at the resonant frequency), which was matched to PA stage. Similarly, dipole antenna's resonant frequency is obtained to be 60GHz with 17 GHz bandwidth (28.33%) and an input impedance of 70Ω. Figure 5.15 summarizes the simulated S-parameters for the TX/RX antennas. As can be observed, the proposed antenna geometry provides a minimum of 21dB isolation between TX and RX across the band.

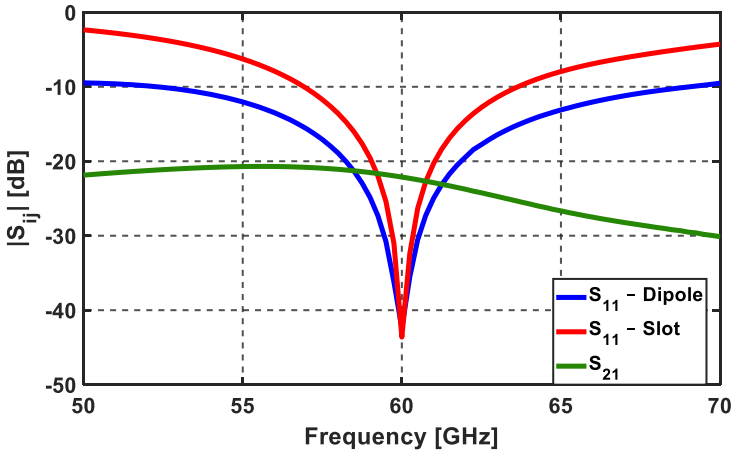


Figure 5.15 Simulated S-Parameters of the antennas

Figure 5.16 depicts the simulated radiation pattern and the gain of TX/RX antennas. The slot antenna offers 6dBi gain, while the dipole antenna's gain is around 5.7dBi [24] [23]. The radiation gain in each antenna has been improved more than 10dB compared to prior work in [117].

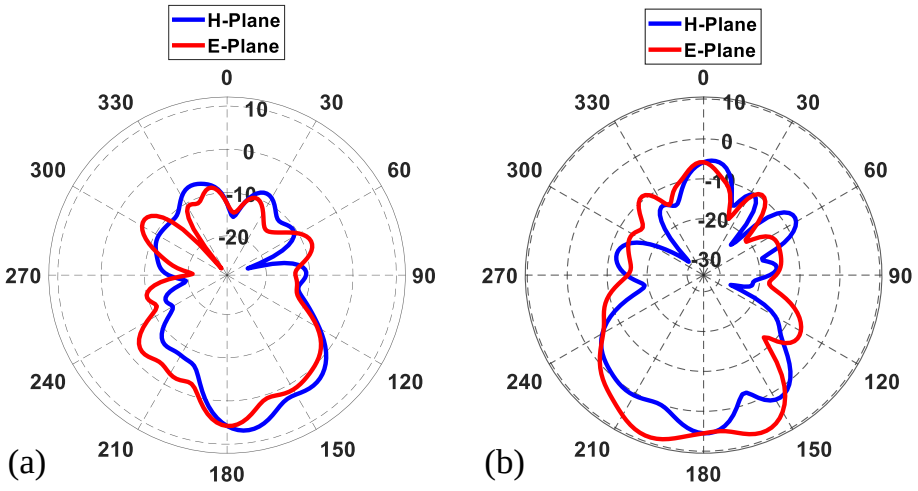


Figure 5.16 Simulated radiation pattern, (a) dipole antenna and (b) slot antenna

Based on simulation results, the slot antenna and dipole antenna provide 41.3% and 39% radiation efficiency, respectively, which is improved more than twice compared to previous on-chip antennas [117]. Additionally, the achieved gain is improved more than 1dB compared to those reported in [118] and [119], using a dielectric resonator antenna and off-chip antenna with plastic lens, respectively.

5.9 Conclusion

A fully-integrated PLL-less FMCW radar transceiver chip with end-to-end operation was designed for mm-scale IoT applications. A new area- and energy-efficient chirp nonlinearity correction technique was implemented for accurate target detection, which was enabled through the co-design of transmitter and receiver DSP blocks. The transceiver RF frontend blocks were co-designed with the TX and RX antennas to achieve optimum efficiency and noise performance. This work achieves >5GHz operating bandwidth at 60GHz, resulting in 3cm range resolution). The PA consistently delivers >4.5dBm power to the TX antenna and the RX has a noise figure of 18dB, resulting in a -88dBm RX sensitivity. The transceiver chip consumes 50mW of active power from 1.2V and 3V supply voltages. This work is compared with state of the are in Table 5.1.

Table 5.1 Performance comparison table

	This Work	Mostajeran TMTT 2019	Mostajeran JSSC 2017	Ozturk TMTT 2017	Kankuppe TMTT 2021
Center Frequency	60GHz	220GHz	170GHz	60GHz	61.5GHz
Radiated Power	4.5dBm	-4.6dBm	-1	6.4dBm	8.1dBm
EIRP	11dBm	14dBm	16.2dBm	21.4dBm	14.6dBm
Total DC Power	50mW	87mW	67mW	520mW	62mW
Range Resolution	3cm	2.7mm	7mm	2.8cm	4.3cm
RX NF	18dB	29dB	25.8dB	8dB	10.5dB
Technology	BiCMOS 130nm	BiCMOS 55nm	BiCMOS 130nm	BiCMOS 130nm	CMOS 28nm
Antenna Type	On-chip with silicon lens	On-chip with silicon lens	On-chip with silicon lens	Off-chip with plastic lens	Off-chip patch
Architecture	Open-loop VCO	Open-loop VCO	Open-loop VCO	PLL-based	PLL-based

Chapter 6:

Conclusion and Future Directions

6.1 Summary of Contributions

During recent years, the Internet-of-Things (IoT) has been rapidly evolving. The IoT technology will continue to revolutionize how we interact with our surrounding environment, transforming everyday objects into smarter devices. There have been billions of connected "smart" things deployed worldwide to date. It is expected that the number of connected smart devices will rise aggressively over the coming years and decades, eventually leading to a world of one trillion connected smart devices.

With limited resources such as energy budgets and congested spectrums, IoT networks of this scale face several challenges that can potentially delay delivering the eventual promise of one-trillion connected IoT devices. First, battery lifespan exhibits a critical barrier to scaling IoT devices. Replacing batteries on a trillion-sensor scale is a logistically prohibitive feat. The

designers have been continuously pushing for designing low-power radios with extended communication ranges that enable energy-autonomy in the WSNs.

Second, radio coexistence has been one of the primary limitations in low-power radios for highly scalable IoT networks. Ensuring interference tolerance in the ULP receivers is the gateway to large-scale IoT networks. However, it mandates high power consumption that reduces the WSN's battery lifespan.

Third, small form factors can make a significant difference in the deployment of WSNs and pave the way for the trillion-sensor network. However, shrinking the WSN form factors can degrade the sensor's performance, as some sensors and radios bulky off-chip components to achieve high performance.

The main objective of this thesis is to develop wireless solutions for communications and sensing that simultaneously achieve energy-efficient operation, extended communication range, millimeter-scale form factors, and high interference tolerance for the Internet of Things applications.

One of the major contributions of this thesis is introduction of a novel dual-chirp modulation scheme and development of a prototype Dual-Chirp On-Off-Keying modulated receiver, that simultaneously achieves ultra-low power consumption, extended communication range, and high tolerance for in-band and out-of-band interference. The receiver achieved -103dBm sensitivity at 2.5kb/s data-rate, while only consuming 110µW of average power with 50% bit-level duty-cycling. Moreover, the receiver can reject interference signals as high as 40dBc. This

work proves the effectiveness of the proposed DC-OOK modulation scheme for achieving low-power operation and high blocker tolerance.

Another major contribution of this dissertation is introducing a blocker-tolerant chirp-OOK modulated receiver that leverages a novel chirped N-path filter with a time-varying narrowband frequency response that filters a wideband chirp. The receiver adopted a mixer-first architecture for low power operation. By using the chirped N-path filter, the receiver suppresses in-band/out-of-band interference. The receiver was fabricated in a CMOS 65nm process and achieves -88dBm sensitivity at 5kb/s data-rate while consuming 320µW active power.

Finally, I presented a fully integrated millimeter-scale PLL-less FMCW transceiver operating at 60GHz that enables energy-efficient range detection in miniaturized WSNs. The transmitter and the receiver were codesigned to enable energy-efficient chirp linearization at the low-frequency baseband ADC, to eliminate the power-hungry phase locked loop for linear chirp generation. This prototype adopted on-chip antennas along with a silicon dielectric lens to maximize the antenna radiation gains and minimize signal trace losses at millimeter-wave frequencies. The FMCW transceiver consumes 50mW of active power, with a range resolution of 3cm and a maximum target detection range of 5 meters.

6.2 Future Directions

As the number of WSNs in the IoT networks continue to grow, there is a huge potential demand for exploring and developing novel and efficient wireless solutions for IoT applications. There are several directions that can be explored as an extended future work for the current thesis.

1) Chirp and Dual-Chirp Modulated Receivers:

Detecting and demodulating chirp-modulated messages requires packet synchronization between the transmitter and the receiver. In the DC-OOK modulated receiver we presented a practical method for packet synchronization in the time domain, which employed sliding chirps. However, this method can increase the receiver latency and directly trades off receiver sensitivity with latency. One possible direction is to develop fast and efficient synchronization schemes in the frequency domain, rather than time domain, with the assistance of energy-efficient integrated DSP.

Another potential direction for the chirp modulated receivers is revisiting the chirp demodulation. In chapter 2 and 3 I presented receivers with time domain chirp demodulation; however, energy-efficient DSP solutions with frequency domain chirp demodulation could potentially offer superior sensitivity and blocker rejection performance.

2) Chirp-Modulated Transmitters:

In this dissertation I have mostly focused on developing ULP receiver solutions operating with chirp modulation. However, generating and transmitting chirp-modulated RF signals is a major challenge, especially for IoT networks. One possible future direction could be exploring and developing energy-efficient chirp synthesizers and chirp transmitters.

3) Ranging and Localization Solutions:

High-accuracy ranging has been an area which has been dominated by high-power and high-performance millimeter-wave radars, that are primarily used in autonomous vehicles. In this thesis I developed an energy-efficient and high-accuracy FMCW transceiver; however, there are potential direction that can be explored to further enhance the performance. One direction could be developing analog or digital blocks on-chip for pre-distorting the open-loop VCO to maximize the baseband signal's SNR and thus radar accuracy.

In the localization area, there has been a lot of prior research on the algorithm and signal processing side for enhancing the accuracy of localization for various modulations such as FSK phase-based modulation. However, the RF receiver implementation requirements and their effect on localization accuracy are barely considered. A potential future direction could be developing an FSK-modulated receiver for phase-based

ranging by codesigning the DSP algorithms and circuits with the RF receiver to maximize end-to-end receiver efficiency and accuracy.

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