Wireless Testing of Integrated Circuits

by

Dae Young Lee

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2012

Doctoral Committee:

Professor John P. Hayes, Co-Chair
Assistant Professor David D. Wentzloff, Co-Chair
Emeritus Professor David J. Anderson
Associate Professor Michael P. Flynn

© Dae Young Lee

2012

To My Family

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my parents, sister, and her husband. I could only successfully finish my graduate study with their strong and constant support. I want to express my sincere gratitude and appreciation to my advisors Prof. John P. Hayes and Prof. David D. Wentzloff for their support, encouragement and guidance for these past four years. It is very special to have two advisors, and I was given a great opportunity to have a good relationship with them. I also would like to extend my sincere gratitude to my other committee members, Prof. Michael P. Flynn and Prof. David J. Anderson, for devoting their time to review this thesis and advising me with valuable suggestions.

I would like to acknowledge my colleagues for constructive and insightful discussions. I have not directly collaborated with them but I greatly appreciate their assistance. I thank Dr. Youngmin Park, Sangwook Han, Jonathan K. Brown, Seunghyun Oh, Kuo-Ken Huang, Osama Ullah Khan, Muhammad Faisal, Nathan Roberts, Elnaz Ansari, and Ryan Rogel. I also express my thank to Dr. Geonwook Yoo, Dr. Kenneth Zick, Chien-Chih Yu, Armin Alaghi, Te-Hsuan Chen, Dr. Jerry Kao, Gwanghyeon Baek, Yonghyun Shim, Dr. Junseok Heo, Yongjun Park, Hyo Gyuem Rhew, and Hyun Kum.

Excellent support from the staff is greatly appreciated. I would like to thank Joel VanLaven for his CAD tool support. I also thank Beth Stalnaker, Deborah Swartz, Melanie Caughey, Denise DuPrie, and Fran Doman for administrative support throughout

my graduate career. I wish to acknowledge the Samsung Scholarship, the Defense Advanced Research Projects Agency (DARPA), and the Alexander von Humboldt Foundation for funding this research.

ABSTRACT

Wireless Testing of Integrated Circuits

by

Dae Young Lee

Co-Chairs: John P. Hayes and David D. Wentzloff

Integrated circuits (ICs) are usually tested during manufacture by means of automatic testing equipment (ATE) employing probe cards and needles that make repeated physical contact with the ICs under test. Such direct-contact probing is very costly and imposes limitations on the use of ATE. For example, the probe needles must be frequently cleaned or replaced, and some emerging technologies such as three-dimensional ICs cannot be probed at all. As an alternative to conventional probe-card testing, wireless testing has been proposed. It mitigates many of the foregoing problems by replacing probe needles and contact points with wireless communication circuits. However, wireless testing also raises new problems which are poorly understood such as: What is the most suitable wireless communication technique to employ, and how well does it work in practice?

This dissertation addresses the design and implementation of circuits to support wireless testing of ICs. Various wireless testing methods are investigated and evaluated with respect to their practicality. The research focuses on near-field capacitive communication because of its efficiency over the very short ranges needed during IC manufacture. A new capacitive channel model including chip separation, cross-talk, and misalignment effects is proposed and validated using electro-magnetic simulation studies to provide the intuitions for efficient antenna and circuit design. We propose a compact clock and data recovery architecture to avoid a dedicated clock channel. An analytical model which predicts the DC-level fluctuation due to the capacitive channel is presented. Based on this model, feed-forward clock selection is designed to enhance performance. A method to select proper channel termination is discussed to maximize the channel efficiency for return-to-zero signaling.

Two prototype ICs incorporating wireless testing systems were fabricated and tested with the proposed methods of testing digital circuits. Both successfully demonstrated gigahertz communication speeds with a bit-error rate less than 10^{-11}. A third prototype IC containing analog voltage measurement circuits was implemented to determine the feasibility of wirelessly testing analog circuits. The fabricated prototype achieved satisfactory voltage measurement with 1 mV resolution. Our work demonstrates the validity of the proposed models and the feasibility of near-field capacitive communication for wireless testing of ICs.

TABLE OF CONTENTS

DEDICATION ... ii

ACKNOWLEDGEMENTS ... iii

ABSTRACT ... v

LIST OF FIGURES ... ix

LIST OF TABLES ... xiv

LIST OF APPENDICES ... xv

CHAPTER

I. Introduction ... 1

1.1. Motivation ... 1
1.2. Communication technologies for wireless testing ... 6
1.2.1. Near-field vs. RF communication ... 8
1.2.2. Inductive and capacitive coupling ... 10
1.3. Related work ... 15
1.3.1. Wireless testing of digital ICs ... 15
1.3.2. Wireless testing of analog ICs ... 17
1.3.3. Wireless interconnect for 3D ICs ... 18
1.4. Thesis outline ... 20

II. Capacitively-Coupled Channel for Wireless Testing ... 23

2.1. Introduction ... 23
2.2. Coupling techniques for wireless testing ... 24
2.3. Circuit model of capacitive coupling ... 26
2.4. Cross-talk analysis ... 30
2.5. Misalignment tolerance ... 33
2.6. Summary ... 35

III. Single-Channel Capacitive Link for Wireless Testing ... 37

3.1. Introduction ... 37

3.2. Channel modeling and modulation 40
3.2.1. Capacitive channel model 40
3.2.2. Pulse width modulation..45
3.2.3. Estimation of pulse-width variation....................................47
3.3. Overall architecture..51
3.3.1. PWM transmitter..51
3.3.2. DLL-based receiver 53
3.3.3. Feed-forward clock selector..57
3.4. Communication link measurement results....................................60
3.5. Summary..63

IV. Non-Contact I/O Pad for Wafer-Level Testing 64

4.1. Introduction..64
4.2. Channel model for RZ signaling..67
4.3. Overall architecture..70
4.3.1. Transmitter with adjustable power....................................70
4.3.2. Receiver pre-amplifier and hysteresis comparator 72
4.3.3. Receiver demodulator 75
4.4. Electrical alignment markers 78
4.5. Communication link measurement results....................................81
4.6. Summary..85

V. On-Chip Wireless Voltage Measurement 86

5.1. Introduction..86
5.2. Integrating ADC..90
5.3. Wireless voltage measurement architecture....................................92
5.4. Prototype implementation..93
5.5. Prototype measurement results 96
5.6. Summary..102

VI. Contributions and Future Work..104

6.1. Thesis contributions..104
6.2. Suggestions for future work..107

APPENDICES..110

BIBLIOGRAPHY 120

LIST OF FIGURES

Figure

1.1 (a) IC probe card [58], and (b) Advantest T7723 mixed signal test equipment [1] 3

1.2 Trends in (a) number of I/O pins, and (b) I/O data rates predicted in [72] 4

1.3 Illustration of near-field and far-field solutions 7

1.4 Near-field and far-field boundary based on [26] 8

1.5 Simulated magnetic field magnitude *H* as a function of distance *R* from the source 9

1.6 Equivalent circuit models for (a) coupled inductors [50], and (b) coupled capacitors 11

1.7 3D models of (a) on-chip inductor, and (b) on-chip capacitor 12

1.8 Simulated frequency response with 20 µm communication distance for (a) coupled inductors, and (b) coupled capacitors 13

1.9 Prototypes of wireless testing: (a) capacitive wafer-level probing [12], and (b) inductively-coupled non-contact probecard [71] 16

1.10 (a) Data rates, and (b) communication distance of selected prior 3D on-chip communication links 19

2.1 Simulated coupled capacitor model with fringing capacitance 27

2.2 More accurate on-chip capacitor model with current return paths 29

2.3 On-chip 3D model of capacitive coupling 29

2.4 Gain vs. plate separation for capacitive coupling 30

2.5 Cross-talk model for on-chip capacitive coupling 31

2.6 Simulated capacitance vs. plate separation 32

2.7 Gain comparison with cross-talk effects 33

2.8 Coupling capacitance vs. misalignment 34

2.9 Gain vs. misalignment 34

2.10 Proposed wireless tester 35

3.1 Proposed capacitively-coupled wireless IC testing with bond pads compatible with standard I/O cells 38

3.2 Lumped circuit model of a capacitive channel between a DUT and ATE 40

3.3 Frequency response of the proposed voltage transfer model 41

3.4 3D model for EM simulation by HFSS v11 43

3.5 Spice simulated frequency response of a channel with the proposed lumped model 44

3.6 PWM bit symbols for ‘0’ and ‘1’ 46

3.7 Illustration of signal level fluctuation, (a) DC-balanced 50% duty-cycled signals, (b) DC-unbalanced PWM signals with ‘0011’ 46

3.8 PWM signals passed through a capacitive channel 47

3.9 DC offsets from the center level for PWM signals (T = 1 ns, α = 0.25) 48

3.10 Matlab simulation results of (a) the maximum pulse-width variation, and (b) the number of pulses to achieve the maximum variation (T = 1 ns, α = 0.25) ... 49

3.11 PWM modulator with an XOR-based edge combiner 51

3.12 Symbol generation for data ‘010’ 52

3.13 Output pad driver with a tri-state inverter 52

3.14 Overall block diagram of the proposed DLL-based bit-slicing receiver 53

3.15 Schematic of the 2-stage receiver amplifier 53

3.16 (a) Block diagram of the DLL, and (b) operation of bit-slicing with multi-phase clocks 54

3.17 Phase-locking characteristics of (a) conventional PFD, and (b) proposed 1-cycle PD 56

3.18 Measurement results from the implemented DLL: (a) step response, and (b) in/output PWM waveforms 57

3.19 Feed-forward dynamic clock selector for signal-level fluctuation 58

3.20 Measured pulse-width changes due to signal level fluctuation 58

3.21 Die photomicrograph of the TX and RX pads 60

3.22 Test setup for the prototype link 61

3.23 Measured eye-diagram of (a) TX PWM signals, and (b) RX output 61

4.1 Capacitively-coupled wireless testing system 67

4.2 PPM with RZ signaling 68

4.3 Capacitive channel model with the termination resistor R_t 68

4.4 Channel gain and DC fluctuation factor with various R_t values at 1 GHz 69

4.5 Simulated waveforms. PPM RZ signals are generated from PWM signals with a terminated capacitive channel 70

4.6 Block diagram of TX and RX 71

4.7 (a) Schematic of the PWM modulator, (b) TX tri-state driver with thick-oxide devices MOS_33 71

4.8 Schematic of the RX amplifier with a hysteresis comparator 72

4.9 Potential positive feedback from unwanted coupling between the RX pad and AC-coupling capacitor 73

4.10 PWM signals regenerated from PPM RZ signals with the hysteresis comparator 74

4.11 Two bit-decision schemes with symbol ‘1’: (a) falling edge detection, and (b) counter-based detector 75

4.12 Two bit-decision schemes with a bubble-type error: (a) falling edge detection makes wrong bit decision, but (b) counter-based detector suppresses the error 76

4.13 Two types of electrical alignment markers: (a) negative marker, and (b) positive marker 77

4.14 (a) Schematic of capacitance measurement circuits, and (b) alignment mechanism 77

4.15 Measured relative capacitance change without rotation misalignment from (a) negative *x*-marker, and (b) positive *y*-marker 79

4.16 Measured relative capacitance change with rotation misalignment from (a) negative *x*-marker, and (b) positive *y*-marker 79

4.17 Die photomicrograph of the prototype chip 81

4.18 Test setup with a micro-manipulator 81

4.19 Test chip surface profile measured by a Dektak 6M surface profiler 82

4.20 Measured BER vs. minimum pulse distance t (T = 1 ns) 83

4.21 Measured BER vs. (a) pad separation, and (b) *x*- and *y*-misalignment 84

5.1 Possible implementations of analog IC testing 89

5.2 (a) Schematic of a single-slope ADC, and (b) its timing diagram 91

5.3 Schematic of the prototype voltage measurement circuits 94

5.4 Schematic of the static comparator 94

5.5 Schematic of the UWB pulse generator 95

5.6 Timing diagram of the prototype 95

5.7 Die photomicrograph of the prototype 97

5.8 Test setup 97

5.9 (a) Capacitive coupling between a wireless probe pad and an RF probe, and (b) measured UWB pulse 98

5.10 Histograms of three different wireless measurement setups with V_{in} = 600 mV 99

5.11 Measured t_c with V_{in} from 600 mV to 855 mV with 1 mV step 99

5.12 Measured DNL for (a) wired setup, and (b) wireless setup 101

5.13 (a) Measured INL, and (b) INL added by the wireless channel 101

A.1 Elemental electric dipole 112

A.2 Near-field and far-field boundary based on [18] 114

B.1 Illustration of 16B/20B encoding and CDR by a PLL [83] 116

B.2 Power spectral density of 1 Gbps random PWM signals..................................117

LIST OF TABLES

Table

1.1 Measurement parameters for IC testing 2

2.1 Performance comparison of various prior chip-level wireless communication systems 25

2.2 Extracted passive element values from EM simulation with 10 µm separation .32

3.1 Detailed passive element values from EM simulation with 12 µm spacing 44

3.2 Performance summary of the 1st prototype chip 62

4.1 Simulated coupling capacitance and oscillation frequency 79

4.2 Performance summary of the 2nd prototype chip 85

LIST OF APPENDICES

Appendix

A. Near-field basics 111

B. Clock data recovery with PWM...115

Chapter I

Introduction

In this chapter, we briefly discuss the background of wireless integrated circuit (IC) testing. Also, we review existing research on wireless testing, and discuss on-chip interconnect for three dimensional ICs (3D ICs) for comparison. Some of the material in this chapter appears in [45].

1.1 Motivation

Generally, testing is proving the functional correctness of a product [4]. Testing of ICs can be regarded as a set of tasks to check the functionality of ICs. In modern IC manufacturing, testing is not limited to the final check for functionality. Rather, engineers perform multiple tests between all the major production stages to reduce overall manufacturing cost by removing defective products before each stage.

IC testing methods can be categorized by their input and output signal types as shown in Table 1.1, which include digital and analog. For digital circuits, functionality is tested with a set of digital test patterns, and the output results are collected by automatic test equipment (ATE) to match them with the desired responses (signatures). In addition, operating frequency and power consumption are measured to check the performance of

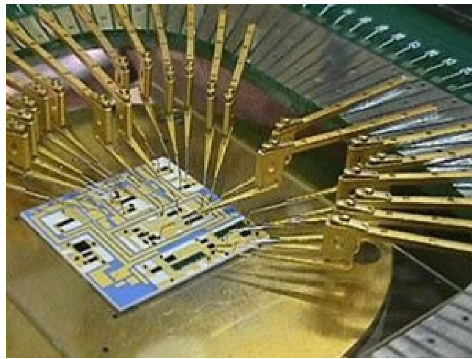
Table 1.1 Measurement parameters for IC testing.

Functional test		Characterization	
Digital test	**Analog test**	**Manufacturing steps**	**In-field monitoring**
• Digital outputs • Frequency • Power consumption	• Analog outputs • Frequency • Power Consumption • Gain • Linearity • Noise	• Device mismatch • V_{th} • Temperature • Leakage current • Parasitic	• NBTI • Soft error • Temperature • Leakage current

digital ICs. For analog circuits, various analog or continuous parameters are measured with analog test inputs to check their functionality. If the performance of a device under test (DUT) meets the desired specifications, it passes the test. Thus, analog testing can be regarded as a performance measurement rather than matching measured outputs to signatures. The parameters typically measured in analog testing are voltage, current, gain, operation frequency, mismatch, and linearity [62].

Testing is not confined to functionality checking only. Process characterization is another important test requirement for IC production. Characterization attempts to quantify the performance of a manufactured IC. It is usually applied to a new design or process technology. Using specially designed circuits, which differ from these of the final product, these circuits are designed to accurately represent key analog or digital parameters of the product.

In this thesis, we refer to characterization after manufacturing as on-line monitoring to avoid ambiguity. Dimension mismatch, threshold voltage, temperature, leakage current,



(a)

(b)

Figure 1.1 (a) IC probe card [58], and (b) Advantest T7723 mixed-signal test equipment [1].

parasitic capacitance and inductance, and doping fluctuation are measured before and after the manufacturing process. Negative bias temperature instability (NBTI) and soft-errors can be monitored later in the field.

In practice, the foregoing testing methods may be combined in various ways to ensure the functionality of the ICs. Additionally, since the overall cost can be reduced if we can find defective devices earlier, testing must be performed between the major manufacturing steps. However, recent advances in IC technology dramatically increase the density of transistors in ICs, resulting in a steady increase in IC complexity and thus an increase in testing costs [72][73]

One conventional way to reduce growing IC testing cost is the automation of testing. ATE is a general and highly automated tool for IC testing. It transmits test input patterns to the DUTs and collects responses for comparison. The ATE is usually equipped with a probe card which consists of multiple probe tips and interface circuits that form a direct electrical connection between I/O pads on the DUT and ATE, as depicted in Figure 1.1. Since probe tips make physical contacts with the DUT, they are usually designed to have sufficient elasticity so as not to deform the DUT [24][76]. The

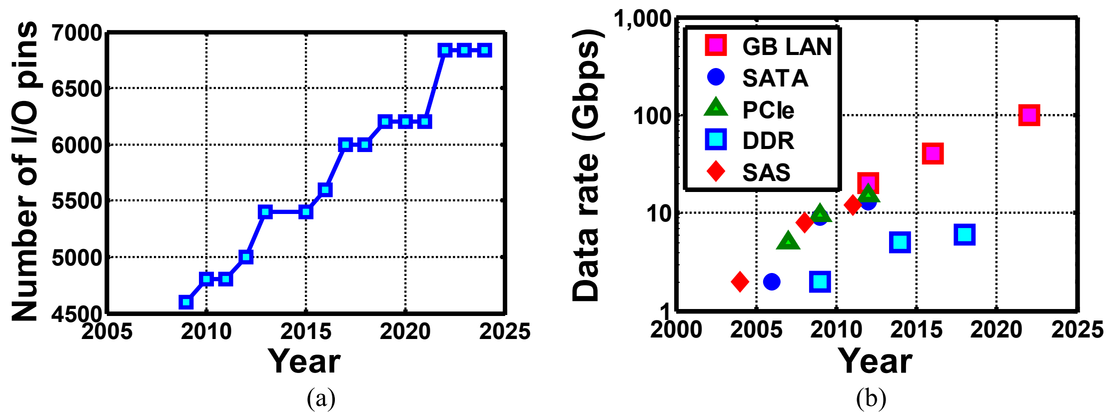


Figure 1.2 Trends in (a) number of I/O pins and (b) I/O data rate predicted in [72].

same ATE can be used for different DUTs by replacing probe cards. Analog probe cards are more complex than digital, since they must support more accurate impedance matching and higher operating frequency [77].

However, conventional probe cards and probing methods have numerous drawbacks. As chips get more highly integrated, the number of their I/O pads tends to increase, as shown in Figure 1.2. Although ball grid array (BGA) and flip-chip technology provide more pins, the number of pins is still limited. Thus, the size and pitch of the probe needles used for testing should get smaller to integrate more pins in a given area. The small size of bonding pads and solder balls causes problems in wafer-level testing [46]. For such small contact points and probe needles, even minor physical damage from contact can cause significant probe deformation. In addition, accumulated debris on the probe tips interferes with testing by increasing the resistance from probe to wafer surface. The debris can be removed with an abrasive cleaner, but that can damage the probe needles.

Increasing demand for devices with multiple chips such as system-in-packages (SIPs), multi-chip modules (MCMs), and three-dimensional ICs (3D ICs) makes testing

with direct-contact probe cards more difficult since conventionally the probe cards do not support the flexible location of contact points [2]. They are unsuitable for parallel testing of multiple dies for the same reason. Additionally, through-silicon vias (TSVs) and micro-bumps for 3D ICs are more difficult to test with conventional probe cards than standard I/O pads because of their size and pitch [6]. Wireless testing is also advantageous for 3D ICs due to the fragility of TSVs and micro-bumps [46].

The limitations of direct-contact testing mostly derive from the physical contact between the wafer and the probe needles. If we could completely replace physical contacts with wireless communication, the foregoing problems could be greatly alleviated [45]. Wireless testing supports the flexibility of contact location as well, making both SIP testing and parallel testing possible.

Wireless testing requires additional circuits and antennas on the die, which should not consume too much chip area. Additionally, the functionality of the original device should not be affected by the components added for testing. Electrical power also needs to be delivered wirelessly to completely remove wired lines during testing. However, as long as the number of signal pads is a significant fraction of the total number of I/O pads, wireless testing of signal pads with wired power can still be beneficial due to the significant reduction of the overall touch-down force. In addition, the data rate needs to be sufficiently high to support at-speed testing for state-of-the-art I/O technologies with gigahertz communication [68][72].

Wireless testing has been proposed previously [10][67]. Practical implementations can be found in [12][22][23][30][31][35][55][56][59][69][71][84][85], which analyze and demonstrate the feasibility of wireless IC testing through either

inductive or capacitive coupling. Also, the wireless technology suitable for testing can be applied to other applications such as chip-to-chip communication [11][14] [20][39][50]][70], package-to-board communication [7][24][40][41][42][87], wireless bio-medical implantable devices [3], and body area networks (BANs) [36][48][76][78][89]. These require short-range and low-power wireless communication technology, which is essential to wireless testing. A more detailed review of existing research will be presented in Section 1.3.

Our goal is to design wireless IC testing systems compatible with today's scaling trends. Non-contact probes can mitigate or even get rid of the problems related to physically contacting probe tips. These probes are used in a very short communication range down to tens of micrometer to achieve high efficiency, and their data rates are up to 1 Gbps to provide sufficient bandwidth for at-speed testing [68].

1.2 Communication Technologies for Wireless Testing

Three major communication methods are potentially suitable for wireless testing of ICs:

- Radio frequency (RF)
- Near field
- Optical

In this thesis, we use the term "RF communication" for far-field communication, and the term "near-field communication" only when discussing capacitive and inductive coupling by quasi-static electromagnetic field radiation. Optical communication transmits signals and power via light at very high frequencies.

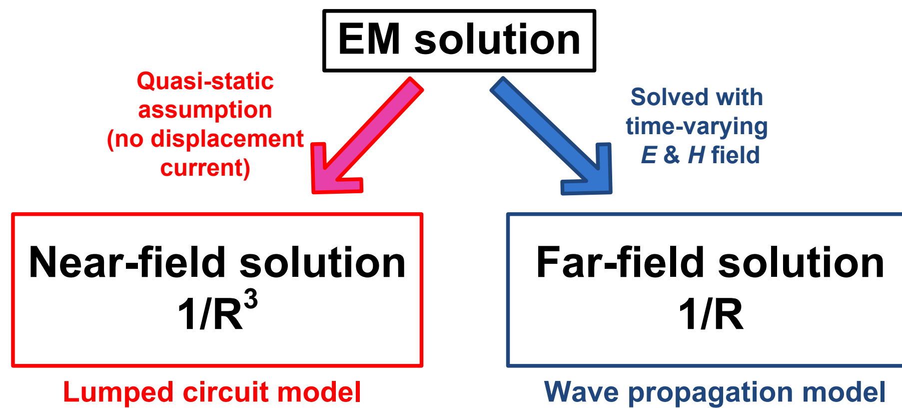


Figure 1.3 Illustration of near-field and far-field solutions.

RF is widely used today in various forms of wireless communication. There has been some research on its use for wireless testing [59]. Since RF requires integrated RF circuits for transmitters and receivers on a DUT, the size of the RF circuits and antennas is of utmost importance. Often modulation is needed to avoid interference from another channel. RF provides long communication range, but its silicon area overhead, including antenna and circuits, is considerable [16][38][59].

In contrast to RF, near-field communication does not use wave propagation. Instead, it transfers energy through a quasi-static electromagnetic field. This enables the communicating circuits to consume relatively low power, and eliminates wave propagation effects like fading, reflection and phase shifting. If the distance between the transceivers is very small, near-field communication may be more efficient than RF communication due to its weak inter-channel interference [43][45].

Optical signals, which consist of high-frequency electromagnetic fields, are relatively immune to noise and interference, so one can detect optical signals without complex modulation and amplifier circuits. However, owing to the difficulty of

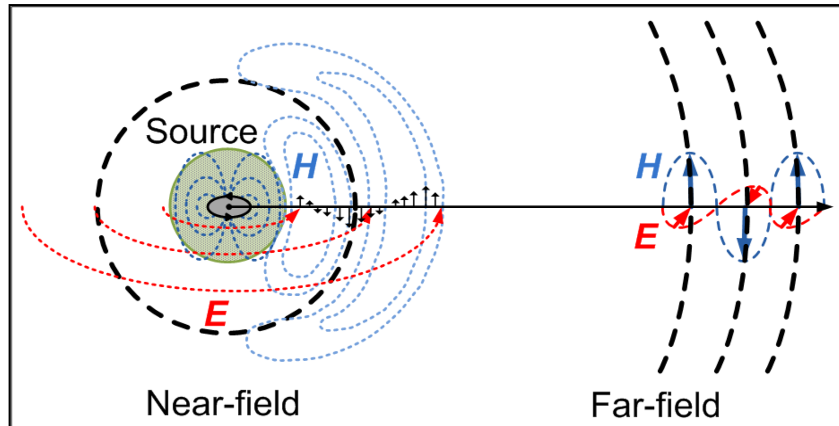


Figure 1.4 Near-field and far-field boundary based on [26].

integrating optics with conventional CMOS processes and the high cost for its fabrication, optical communication seems unsuitable for wireless testing [43][49].

Taking into account circuit size, including on-chip antennas, power consumption, compatibility with conventional CMOS process technology and the distance between transceivers, RF communication and near-field communication are the most appropriate candidates for the wireless testing application. Both can be easily fabricated with conventional CMOS technology and provide reasonable communication range for testing purposes.

1.2.1 Near-Field vs. RF Communication

RF and near-field communication seem like distinct technologies, but both stem from the same fundamental electromagnetic effects, as shown in Figure 1.4. Whether to use near-field modeling or not is decided by the distance from the radiation source, and the frequency used. At a fixed frequency, most of the energy radiates through a quasi-static field near the source, but electromagnetic wave propagation is the major means of

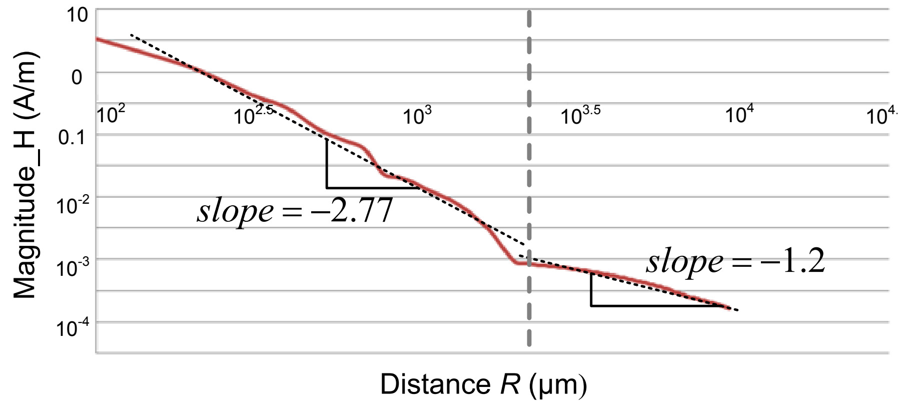


Figure 1.5 Simulated magnetic field magnitude H as a function of distance R from the source.

energy transfer in the far-field zone as depicted in Figure 1.4. In this section, we present the results of simulation experiments, which indicate that both near-field and RF communication co-exist by showing a gradual transition between the near field and far field. For details on near-field theory, see the Appendix A.

Figure 1.5 shows the simulated magnitude of the magnetic field H with increasing distance R from a 3D inductor used in a chip-to-chip communication transceiver circuit that we designed with IBM 0.13 μm technology. Ansoft's HFSS v10 is used for the H field simulation. At a certain point, we observe that the slope of attenuation changes from –2.77 to –1.2, which represents approximately $1/R^3$ attenuation in the near field and $1/R$ in the far field. This plot shows that even the inductor, which is used for near-field coupling in general, can generate a far-field electromagnetic wave. There are little errors due to the idealized assumption that the dimension of an inductor is infinitesimal. On the far-field side, we can see gradual changes in the slope of the H field since the expression for magnetic intensity contains all lower or higher order terms, not only$1/R^3$ or $1/R$.

The various existing wireless communication technologies require quite different antenna designs. Generally, RF antennas have a linear shape of size proportional to the wavelength of an RF carrier, which should have good directivity [8]. Capacitors and inductors used as near-field antennas are sometimes called transducers or electrodes. Since both near-field and RF communication experience a rapid drop in power with increasing distance, the communication distance plays a critical role in deciding signal strength in wireless testing. Fortunately, conventional ATE performs touch-downs on the target wafer with an accuracy measured in micrometers [44], and thus we can use very short communication distance to maximize efficiency. Because electromagnetic energy is mostly delivered by quasi-static radiation over such a short distance, the antenna should be a kind of inductor or capacitor rather than a conventional RF antenna.

For efficient RF communication, even a carrier frequency up to tens of gigahertz necessitates millimeter-sized antennas which are too large to be implemented on a chip. Moreover, due to the propagating wave characteristics of electromagnetic field such as fading, reflection and multipath degradation, the required circuit size and complexity for RF communication must be substantial [16][38][59].

1.2.2 Inductive and Capacitive Coupling

There are two main kinds of near-field phenomena: inductive coupling and capacitive coupling. Each coupling method can be seen as the dual of the other. Equivalent circuit models for an on-chip inductor [50] and a capacitor are shown in Figure 1.6.

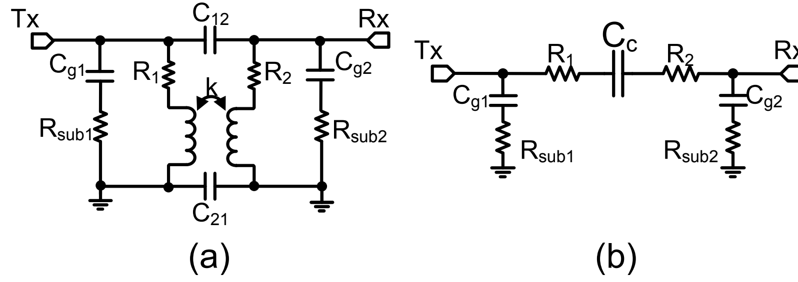


Figure 1.6 Equivalent circuit models for (a) coupled inductors [50], and (b) coupled capacitors.

We can derive the gain of each coupled channel as follows. C_g represents the capacitance between metal and substrate. For inductive coupling, the capacitances C_{12} and C_{21} between the two inductors can be ignored because they are relatively small. Substrate resistance R_{sub1} and R_{sub2} are ignored in both cases as well. If the load impedance R_L is on the receiver node, the gain of the inductively coupled channel is as follows [50].

$$\frac{V_{Rx}}{V_{Tx}} = \frac{j\omega k\sqrt{L_1 L_2}}{1 + j\omega C_{g2} R_2} \cdot \frac{1}{R_L(1-\omega^2 L_1 C_1) + R_1 + j\omega(C_1 R_1 R_L + L_1)} \tag{1.1}$$

For capacitive coupling, the corresponding equation is

$$\frac{V_{Rx}}{V_{Tx}} = \frac{j\omega R_L C_C}{1 + j\omega R_L (C_{g2} + C_C) + (R_1 + R_2) C_C (j\omega - \omega^2 R_L C_{g2})} \tag{1.2}$$

These analytical models give us some useful insight into the design of on-chip coupled inductors and capacitors. High gain can be achieved by a large coupling coefficient k for coupled inductors, which highly depends on the number of turns, the area of the coils, and the distance between the two inductors. For capacitive coupling, a large coupling capacitance C_c leads to high gain. Permittivity, capacitor area, and plate

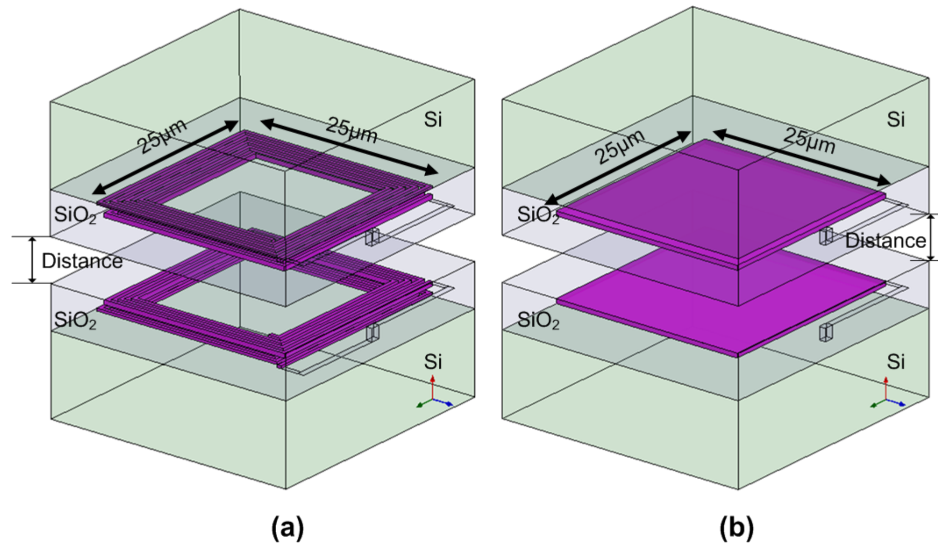


Figure 1.7 3D models of (a) on-chip inductor, and (b) on-chip capacitor.

separation are factors that decide coupling capacitance. Because high-permittivity materials entail additional cost, from a design point of view inductively coupled communication provides more options to increase gain. For example, increasing the number of turns is an efficient means to get a stronger signal.

Based on the foregoing model, the coupling capacitance can be maximized by using large metal plates with small separation. The inductive coupling coefficient can be increased when larger coils with more turns and shorter separation distance are used. The coupled inductors and capacitors in Figure 1.7 are both of size 30 μm × 30 μm with 20 μm spacing, and were simulated with Ansoft's HFSS v11. For each case, the voltage gain was measured, which is the output voltage divided by the input voltage. The results of a frequency response simulation employing simple 3D on-chip models are given in Figure 1.8. As expected, inductive coupling shows a resonant peak in voltage gain, but the gain for capacitive coupling monotonically increases and has a resonant peak at a very high off-scale frequency. To maximize efficiency, it is desirable to use the resonant frequency

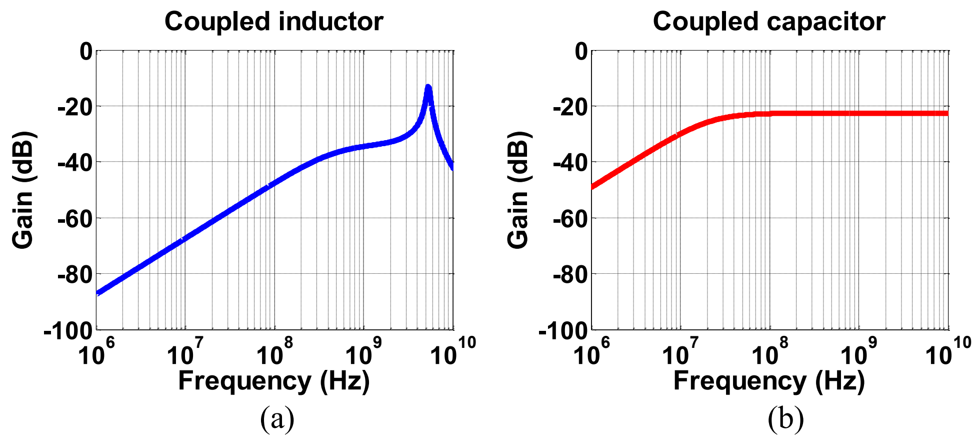


Figure 1.8 Simulated frequency response with 20 μm communication distance for (a) coupled inductors, and (b) coupled capacitors.

in inductive coupling. For capacitive coupling, using a higher frequency is better in most cases.

Inductive coupling appears to have several advantages, even though the design and characterization of on-chip inductors are complicated, First, it is driven by current change, which is not limited by supply voltage and is easily provided by current-generating circuits. Therefore, the scaling down of supply voltage and physical size of devices do not diminish signal strength. Second, almost no high permeability material is used in conventional CMOS processes; only eddy currents generated by high conductivity material affect the magnetic field, and are not significant. Metal wires in a conventional CMOS process do not contribute to eddy currents, in general, due to their narrow shapes. In addition, the coupling coefficient of inductive coupling can be increased by using higher number of turns. The increased driving strength is beneficial especially for 3D IC testing since it can transmit data through the substrate with sufficient coupling coefficient.

Capacitive coupling is another option for wireless testing owing to the easy implementation of capacitors: small pieces of top-layer metal can form capacitors between a wireless probe and a device on a wafer [10][34][69]. In addition, since a capacitor performs like a short circuit at high frequency, capacitive coupling is good for applications that need a high data rate. As shown in Figure 1.8, a capacitively-coupled channel does not have a resonant peak in the frequency range below 10 GHz. A key advantage of capacitive coupling is that it enables the reuse of bond pads as antennas. This greatly relaxes area constraint of added wireless circuits.

Because of the longer communication distance of inductive coupling, it is attractive for SIP and MCM testing; it provides significantly longer communication range than capacitive coupling. For the same reason, those testing nodes can be used for on-line monitoring after production. For example, built-in-self-test (BIST) circuits and on-chip characterization circuits, which usually have poor accessibility from outside a die or package, can be accessed with inductively-coupled wireless testing nodes. For conventional wafer-level testing, capacitive coupling can be used as well, since there is no interfering material, and the communication distance can be kept as short as the passivation thickness (less than tens of micrometers). These factors relax the main drawbacks of capacitive coupling significantly in terms of signal strength. The gain of capacitive coupling is sufficiently high for such a short distance. Therefore, capacitive coupling is also attractive for wireless testing of non-stacked chips. We conclude that near-field communication via both inductive coupling and capacitive coupling is the most promising technology for wireless testing, primarily due to its small circuit area and low power consumption.

1.3 Related Work

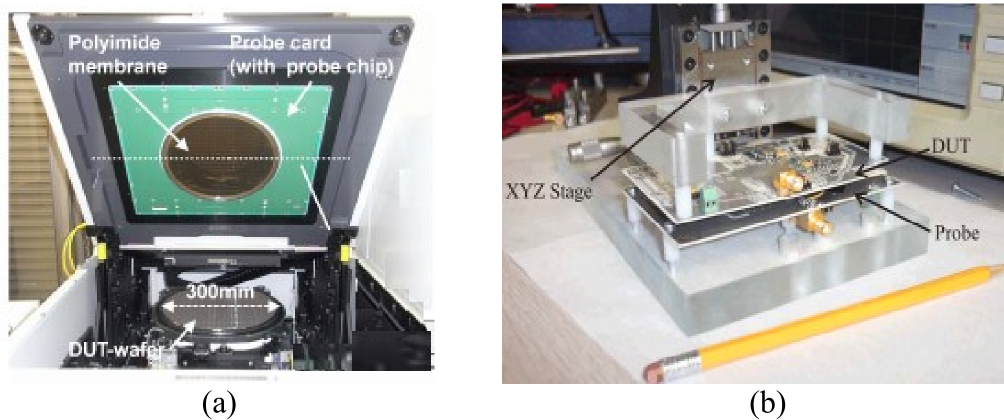
This section summarizes related research on wireless testing. Wireless functionality testing for digital and analog ICs and wireless characterization circuits is covered. Chip-to-chip communication work is also discussed, where the goal is to check the feasibility of short-range and low-power wireless communication rather than testing.

1.3.1 Wireless Testing of Digital ICs

The concept of wireless testing through near-field communication was proposed in [10][67]. Salzman and Knight studied capacitive coupling as a communication channel to address the problems of testing a multi-chip package (MCP). Known good dies (KGDs) should be selected before assembly to reduce manufacturing cost. However, conventional testing methods using probe tips are not effective for MCP testing because they do not support flexible contact point location. Through capacitive coupling, MCPs can be tested before assembly without wired connections. In addition, chip-to-chip communication and wireless power transfer through capacitive coupling are proposed in [11].

Wireless wafer probing of ICs is also discussed in [10]. That work utilizes capacitive coupling as a communication channel, which leads to simpler designs in terms of the antenna structure. Since a capacitively-coupled channel can be formed with two top metal plates, it relaxes the design constraints more than inductive coupling approaches. However, follow-up research for wireless testing has not been reported and no implementation of the work is given in [10].

The more practical circuit design and implementation aspects of wireless wafer-level testing via capacitive coupling are demonstrated in [12][30][31][71]. Photographs



(a) (b)

Figure 1.9 Prototypes of wireless testing: (a) capacitive wafer-level probing [12], and (b) inductively-coupled non-contact probecard [71].

of two prototypes from [12] and [71] are shown in Figure 1.9. Wireless test probes were implemented on a membrane flexible circuit board (FCB) [12] and printed circuit board (PCB) [30][31]. Both show that capacitive coupling can achieve reliable gigahertz communication over a short communication range. In [69], capacitive coupling is formed between slightly shorter probe needles and standard I/O compatible on-chip pads to transmit data. Feasibility with cross-talk effects is discussed, but no bit-error rate performance is reported, and the achieved data rate is very low compared to other near-field communication work.

Sellathamby et al. proposed a method of wireless testing and presented some experimental results in [71]. They give a detailed discussion of implementing wireless wafer-level testing. Near-field communication through two coupled inductors is proposed with simulation and measurement results. Their paper [71] also contains analysis of crosstalk from adjacent channels, and channel characterization results with antenna misalignments and varying communication distance.

Moore et al. present JTAG-compatible wireless testing circuits for SIP testing in [56]. Compared to wafer-level testing, their implementation contains an extra wireless communication module for signaling between a DUT and the ATE. This wireless module collects signals from multiple dies in a SIP and serializes them for transmission to the ATE. The authors propose wireless SIP testing and present measurement results from implemented designs, but the information given about the implemented circuits is limited.

A more detailed analytical approach to channel modeling and the specification of a receiver can be found in [84]. This paper describes an ultra-wide band (UWB) transmitter and receiver using inductive coupling for wireless wafer-level testing. A transformer circuit model for an inductively-coupled channel with various design parameters such as communication range and misalignment is proposed. The circuit design includes a UWB transmitter and a low-noise amplifier (LNA) for the receiver.

In contrast to prior research, wireless testing with RF communication is studied in [22][59]. In [59], two transmitter/receiver architectures are presented: on-off keying with frequency modulation and an image rejection architecture. The communication range is much longer than others with near-field communication, but the size of the RF antenna is substantial. Also, the design requires a special IC process (InGaP/GaAs).

1.3.2 Wireless Testing of Analog ICs

Analog testing using wireless communication also has been proposed by several groups. Yoshida et al. describe a wireless voltage regulator using inductive coupling [85]. Although it is not yet fully developed into a complete testing system and it requires an

accurate on-chip reference voltage for each DUT, it shows the feasibility of wireless testing of analog ICs.

In [55][79], the feasibility of wireless on-chip characterization is also discussed. The simulated ring oscillator circuits generate RF signals which vary with the capacitance and resistance at the output node. By measuring the frequency of these RF signals, capacitance and resistance on the DUT can be determined. The proposed on-chip wireless characterization circuits can be purely contactless thanks to RF power transfer with a rectifier and voltage doubling circuits.

Measuring the matching of physical devices with RF signals has also been proposed [59]. Since the receiver architecture is based on symmetric circuit components, the resulting RF signal can be a good way to measure DUT process variation.

1.3.3 Wireless Interconnect for 3D ICs

An application similar to wireless testing in terms of range, power consumption, and circuit size is on-chip wireless interconnect for 3D ICs. Although it has fundamental differences from wireless testing such as design symmetry between transceivers, it is helpful in understanding wireless communication technologies used in short range data transfer. Its communication range R is confined to tens of micrometers, and it consumes low power and small area. Recent work on chip-to-chip communication reveals that it can achieve data rates up to 10 GHz via near-field methods [14][15][17][20][41][42][50-54][70].

Both inductive and capacitive coupling have been proposed for chip-to-chip communication. In [51], a data transfer rate of 1 Tbps with 1,024 inductively coupled

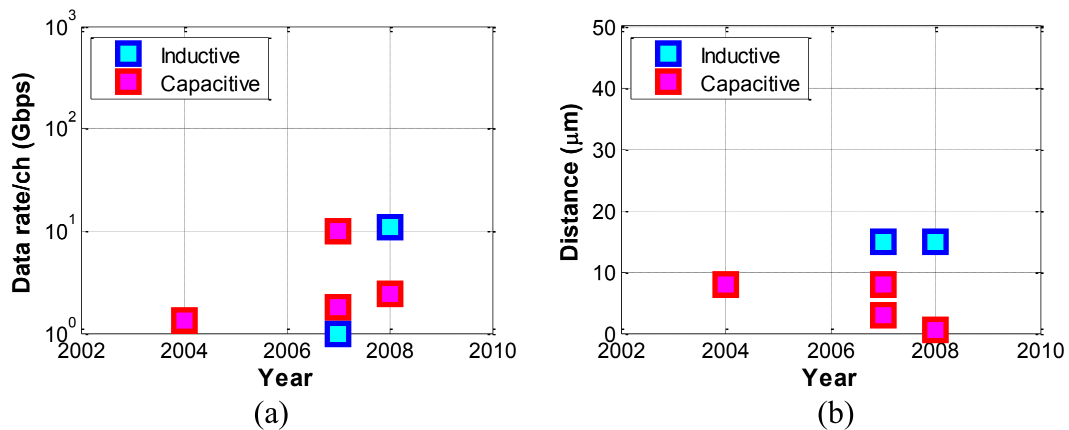


Figure 1.10 (a) Data rates, and (b) communication distance of selected prior 3D on-chip communication links.

channels and 4-phase TDMA is demonstrated. To achieve such a high data rate with very low bit-error rate (BER) less than 10^{-12}, a dynamic comparator is used in the receiver, which has very high gain, but requires precise clock alignment. An extra set of transmitter, receiver, and channel circuits is used for clock transfer. Since accurate clock phase alignment is essential for a dynamic comparator, phase adjustment and clock synchronization are critical design issues with this approach. Utilizing a few large inductors with bit serialization has been proposed in [53] to reduce the area consumption. The receiver is based on an asynchronous comparator, which doesn't require a precisely aligned clock, and a 1:16 bit-serializer is used to achieve 6.4 Gbps burst mode transmission.

Other designs for capacitive coupling can be found in [15][17][20]. In [20], a partitioned mini-pad design is proposed to resolve misalignment issues, and capacitive sensor circuits are employed for misalignment measurement. A dynamic comparator is used for data recovery. More capacitive communication designs can be found in [17]. Two different designs with amplitude modulation and pulse modulation are presented and

compared. The modulated signals are recovered with a non-clocking sense amplifier. Fazzi et al. propose an asynchronous bidirectional transceiver, which achieves the highest data rate at low power consumption [15]. Their most significant performance improvement is mainly due to very close separation between two metal plates and their use of a special process technology.

Figure 1.10 compares several recent chip-to-chip communication designs in terms of data rate and communication distance. It shows that most near-field prototypes can achieve a data rate of up to 10 Gbps with less than 20 μm communication distance. Assuming a communication distance of about 10 μm, this result validates the conclusion that near-field communication is suitable for gigabit communication for wireless IC testing.

1.4 Thesis Outline

The main contribution of this dissertation research is to demonstrate the feasibility of wireless IC testing via near-field capacitive communication, which mitigates many of the problems associated with conventional probe card based testing. Various wireless testing methods are investigated and evaluated with respect to their practicality. The research then focuses on near-field capacitive communication because of its efficiency over the very short ranges needed during IC manufacture. Several prototype chips were fabricated and tested to validate the proposed wireless methods of testing ICs.

In Chapter 2, we propose a new capacitive coupling model for wireless IC testing. We analyze the advantages and disadvantages of capacitive coupling compared to inductive coupling. Then, the more accurate lumped circuit model of capacitive coupling

is discussed. The conventional channel model of capacitive coupling only employs a capacitive voltage divider, which has high-pass characteristics. The proposed lumped model considers the separate ATE and DUT grounds and gives more accurate frequency response for capacitively-coupled channels. In addition, the effect of misalignment and cross-talk from adjacent channels is analyzed.

Chapter 3 presents a prototype capacitively-coupled communication link for wireless IC testing based on the proposed channel model. It has two unique features: first, it reuses the antenna as a bond pad after testing since the I/O bond pad is suitable for capacitive coupling due to its shape. Second, it delivers both clock and data signals at the same time through a single wireless channel. The interconnection complexity, especially at the ATE side, may cause significant timing uncertainty. The self-clocked pulse-width modulation (PWM) signals in the prototype enable a relatively simple clock and data recovery (CDR) architecture, and there is no need for an additional clock channel for retiming.

In Chapter 4, the second prototype of capacitive links is discussed. It includes the effect of electro-static discharge (ESD) protection circuits on the receiver side, and measurement results from a die-level experiment are presented. The new prototype supports adjustable transmitter power and pulse position modulation (PPM) with return-to-zero (RZ) signaling. The reduced channel gain due to the ESD protection circuits can be compensated by raised transmitter power. PPM RZ signals provide a simple CDR as well, and enable flexible symbol design with a counter-based majority voting demodulator. Electrical alignment measurement circuits are also implemented to assist fine die-level alignment.

In Chapter 5, a prototype design of analog voltage measurement circuits that use capacitive coupling is discussed. The prototype wirelessly delivers voltage measured on-chip to a tester with two UWB pulses. Due to the high accuracy of off-chip timing measuring equipment, the on-chip circuitry can be relatively compact and simple. The impact of the wireless channel on non-linearity and distortion is evaluated and compared to the wired case.

The contributions of this thesis and suggestions for future work are outlined in Chapter 6. The major contributions include a new capacitive channel model accounting for the effects of cross-talk, DC-level fluctuation, and misalignment; a compact CDR architecture for wireless IC testing; two fabricated test chips to validate our models and architecture; and a method of on-chip analog voltage measurement. Wireless power transfer for IC testing, wireless built-in-self-test (BIST) circuits, and automatic control of wireless circuits for testing ICs are suggested as topics for future research.

Chapter II

Capacitively-Coupled Channel for Wireless Testing

In this chapter, wireless testing of integrated circuits (ICs) via capacitive coupling is evaluated by means of several analytical models. As we have seen in the previous chapter, despite the fact that direct-contact probing is the standard testing practice in the IC industry, this approach is likely to become less effective and more costly in the future. We propose wireless testing via capacitive coupling to minimize the additional area for antennas. The material in this chapter appears in [34].

2.1 Introduction

Since probe tips physically touch down on a wafer, they undergo contact point deformation and debris accumulates on the probe tips [44]. Scaling trends also make probe card testing less suitable for future ICs. As devices scale down, the size and pitch of I/O pads gradually shrink as well, requiring very small contact points. Higher I/O signal frequency is also problematic for probe-card testing. To minimize the time spent on the ATE, at-speed testing is desirable. However, scaling trends require very high I/O frequency for at-speed testing [72]. High-frequency probe tips need careful characterization for impedance matching, which is yet another cost-increasing factor.

Wireless wafer-level testing has been proposed as an alternative, where the goal is to replace physical contact points (bond pads) with wireless channels and antennas. Both digital and analog signals can be transmitted through the wireless channels. Power can also be delivered either via wireless communication or wired power lines. By reducing or eliminating physical touch-downs, many of the problems associated with direct-contact probing can be greatly alleviated.

We present several new analytical models for on-chip capacitive coupling. They can be used for channel performance prediction and antenna design. Based on these models, cross-talk and misalignment can be analyzed as well. This chapter is organized as follows. In Section 2.2, capacitive and inductive coupling are compared. Analytical models for capacitive-coupled test channels are presented in Section 2.3. Cross-talk from adjacent channels is discussed in Section 2.4. Misalignment simulation results are given in Section 2.5. Finally, Section 2.6 presents our conclusions on the feasibility of capacitively-coupled wireless testing.

2.2 Coupling Techniques for Wireless Testing

Wafer-level testing requires very short communication range, making it well-suited to near-field methods. As noted earlier, a wafer and a tester can be as close as a few micrometers. Near-field antennas are more efficient than the linear-shaped antennas needed for RF communication in the near-field zone. In addition, near-field communication does not suffer from wave propagation effects like reflection and multi-path delay, which also require complex and power-consuming circuits.

Table 2.1 Performance comparison of various prior chip-level wireless communication systems.

	Gu *et al.*, 2007 ISSCC [17]	Daito *et al.*, 2010 ISSCC [12]	Kim *et al.*, 2010 3DIC [31]	Miura *et al.*, 2011 ISSCC [54]
Basic technology	Capacitive	Capacitive	Capacitive	Inductive
Application	Chip-to-chip	IC Testing	IC Testing	Chip-to-chip
Energy/bit	0.27pJ/b	2pJ/b	0.47pJ/b	0.145pJ/b
Data rate/channel	10Gbs/ch	1Gbs/ch	15Gbs/ch	1.1Gbs/ch
BER	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$
Process	0.18μm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Range *R*	3μm	4μm	4μm	20μm
Size of channel	2x48x18 $μm^2$	80x80 $μm^2$	80x80 $μm^2$	2x110x110 $μm^2$

We decided to focus on capacitive coupling for our wireless wafer-level testing study. The antennas for capacitive communication can be formed with a simple planar shape in the top metal layer, which reduces the design complexity significantly. Also, we already have shown in Chapter 1 that the capacitive coupling provides sufficient gain with a very short communication distance. A comparison of relevant previously published work is presented in Table 2.1. Capacitive coupling can achieve very high data rate with face-to-face chip stacking because the communication distance can be shorter than 5 μm. Also, capacitive antennas can be reused for wirebonding after testing so that area consumption is minimized. Inductive coupling, on the other hand, can achieve a longer communication range, but consumes more area for coils [54]. All capacitive techniques can achieve data rates higher than 1 Gbps with very low BER due to the relatively short communication distance. Together, these examples support the case for capacitive coupling in wireless wafer-level testing.

2.3 Circuit Model of Capacitive Coupling

Two capacitively-coupled metal plates can be modeled by the following ideal capacitance model.

$$C = \varepsilon \frac{A}{R} \tag{2.1}$$

where A is the capacitor area, R is the plate separation, and ε is the permittivity of medium. This is a simplified model in which fringing effects along the edges of the metal plates are ignored. Thus, it is only valid when the plates are infinitesimally thin, and the separation between them is relatively small. In reality, the metal plates have a non-zero thickness that cannot be ignored in practice. This thickness contributes to fringing capacitance and increases overall capacitance between the two plates. More accurate capacitance models can be found in [47][87]. In [87], Yuan and Trick model metal plates with non-zero thickness as a combination of ideal plates and two cylindrical sidewalls. Therefore their model is only valid for when the thickness is relatively small. A capacitance model of even greater accuracy can be found in [47]. This model widens the valid thickness range by adding E-field effects from the top surface. However, compared to Yuan and Trick's model, it is an experimental model with less analytical justification.

We carried out a number of simulation experiments using Ansoft's HFSS v11, an electromagnetic field solver. With an on-chip 3D model of the coupled plates, the coupling capacitance C_c was extracted. For the simulations, two on-chip 92 μm × 52 μm sized metal plates were placed with varying separations. The HFSS-simulated results are compared with various analytical capacitance models in Figure 2.1. All capacitance models match well for separation shorter than 10 μm, but they become inaccurate above

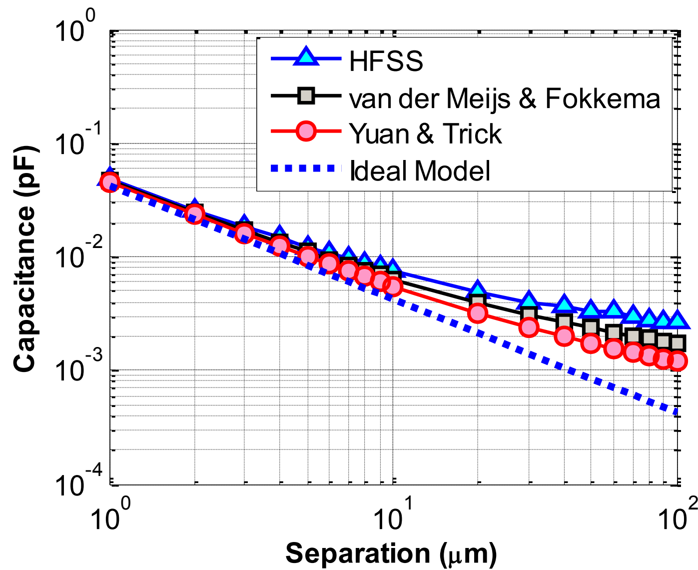


Figure 2.1 Simulated coupled capacitor model with fringing capacitance.

10 μm separation. While van der Meijs and Fokkema's model [47] yields the result closest to the extracted capacitance, the ideal plate model is still comparable with a very short separation 1/10 of the size of metal plates. In addition, since the ideal model always underestimates the capacitance, it can be used for a quick estimation of the worst-case.

Another issue for on-chip capacitance modeling is the permittivity ε of the medium between the two metal plates. Since there is no blocking material between a DUT on a wafer and the tester, the medium can be modeled as vacuum with $\varepsilon = \varepsilon_0$. In practice, the metal plates are usually implemented with the last metal layer of the IC process. There is a passivation layer above the last metal layer, which has permittivity around 3.4. Therefore, for better accuracy, the on-chip capacitive coupling model should include the effect of the passivation layer. As for the ideal capacitance model, the vacuum model can be used as the worst-case assumption for a quick estimation. Then, a more accurate model can be used for more exact analysis.

The voltage transfer function of on-chip capacitive coupling given in (1.2) can be further simplified. If the series resistance of the metal plates is ignored, the transfer function reduces to that of a voltage divider.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{C_c}{C_c + C_g} \tag{2.2}$$

Here, C_c is the coupling capacitance between the metal plates, and C_g is the capacitance to ground. As discussed, higher C_c is desirable to achieve higher voltage gain, and can be modeled with the ideal capacitance model.

The use of separate grounds for the DUT and tester are also critical in modeling. An ideal common ground is assumed for the on-chip voltage transfer function in both (1.2) and (2.2). However, in reality both chips have different grounds, and these different grounds may affect channel gain significantly. For example, if there is no closed current return path, a very large current loop will cause substantial parasitic inductance, which lowers the resonant frequency, and may render of the entire system unstable. To avoid this, AC grounds should be placed on-chip to provide current return paths for high frequency signals.

A more accurate voltage transfer function including current return paths and AC grounds can be written as follows.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{s^2 L_R C_c \left(C_R + C_g\right) + C_c}{s^2 L_R \left\{C_R \left(C_c + C_g\right) + C_c C_g\right\} + C_c + C_g} \tag{2.3}$$

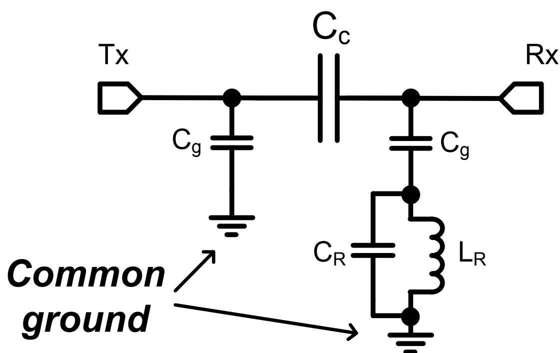


Figure 2.2 More accurate on-chip capacitor model with current return paths.

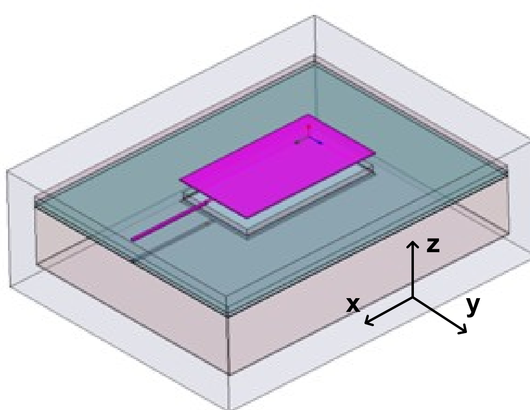


Figure 2.3 On-chip 3D model of capacitive coupling.

L_R and C_R are added parasitic inductance and capacitance from the return paths and grounds. L_R is mainly determined by wirebonding inductance and off-chip signal traces. C_R can be minimized when larger AC-ground pad and shorter separation are used. The lumped circuit model is depicted in Figure 2.2. Based on this new model, we can conclude that parasitic inductance from the current return paths should be kept as small as possible, and the capacitive coupling of the AC ground should be large enough to support good current returns. Since the combination of these parasitics can cause resonance, their poles and zeros should be shifted to very high frequencies in order not to affect the

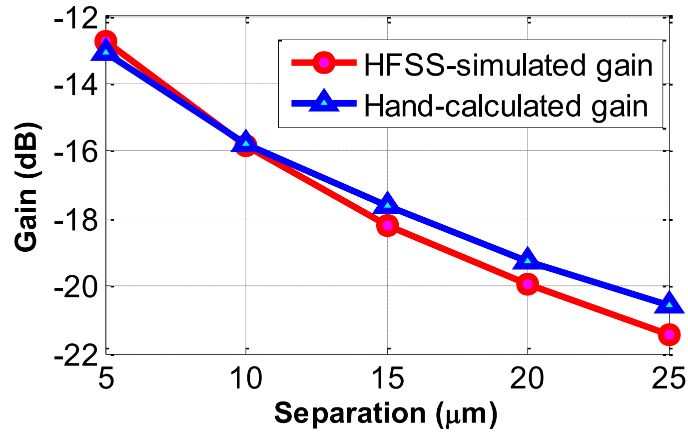


Figure 2.4 Gain vs. plate separation for capacitive coupling.

system stability. When this condition is met, the more accurate model can be approximated by the simpler voltage divider model in (2.2).

A 3D model of an on-chip capacitor with 95 μm × 52 μm metal plates shown in Figure 2.3 was simulated using HFSS v11. As Figure 2.4 shows, the HFSS-extracted gain matches well with the hand-calculated gain from an ideal plate model for small separation distances. For wider separation (over 15 μm), the difference gets larger since the ideal plate model underestimates fringing effects.

2.4 Cross-Talk Analysis

Although near-field radiation is only strong enough at very short range, cross-talk from adjacent channels is still a critical source of interference. The worst-case scenario of adjacent channel interference is depicted in Figure 2.5.

When a transmitter TX drives a target receiver RX, there are two possible interference sources from adjacent channels: one on the same chip and one on the other chip. Since a channel is configured for unidirectional communication, only one case is

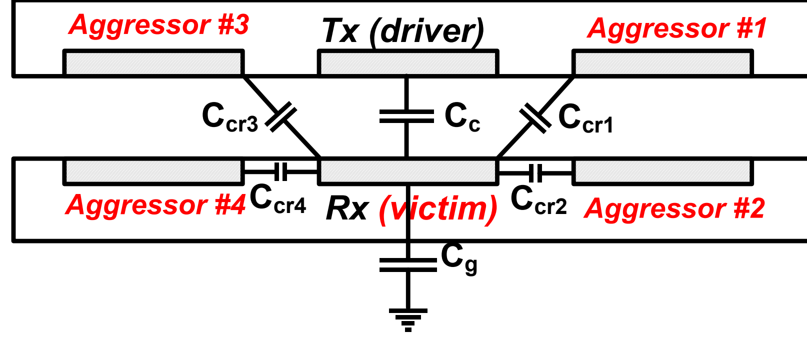


Figure 2.5 Cross-talk model for on-chip capacitive coupling.

possible at any time. Between the two cases, the aggressors from the same chip degrade channel gain more than those from the other chip due to large metal plate separation and small overlapping area. Most fringing capacitance is screened by the metal plates, and the distance to aggressors on the same chip is always shorter. Thus, the cross-talk capacitance C_{cr2} and C_{cr4} should be added to the voltage transfer function to estimate the effect of cross-talk.

If we assume the worst case, the cross-talk capacitance needs to be doubled due to the Miller effect. If the two coupled nodes switch in opposite directions at the same time, the effective coupling capacitance also is doubled. The voltage transfer function with cross-talk is then as follows.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{s^2 L_R C_c \left(C_R + C_p\right) + C_c}{s^2 L_R \left\{C_R \left(C_c + C_p\right) + C_c C_p\right\} + C_c + C_p} \tag{2.4}$$

where $C_p = C_g + 2 \cdot \left(C_{cr2} + C_{cr4}\right)$ The effect of cross-talk contributes to the overall capacitance to ground, and results in reduced voltage gain.

Fortunately, the sidewalls of the metal plates used for capacitive coupling are quite small. Fringing effects from the top and bottom sides are blocked by other metal plates if other channels are relatively close. Therefore, the cross-talk capacitance from

Table 2.2 Extracted passive element values from EM simulation with 10 μm separation.

C_c	5.43 fF
C_g	26.73 fF
C_{cr2}, C_{cr4}	0.35 fF
C_R	20.7 fF*
L_R	1 nH *

* The AC-ground pad is assumed 4× larger than a coupling pad.
* Parasitic inductance is assumed for 1-mm wire-bonding.

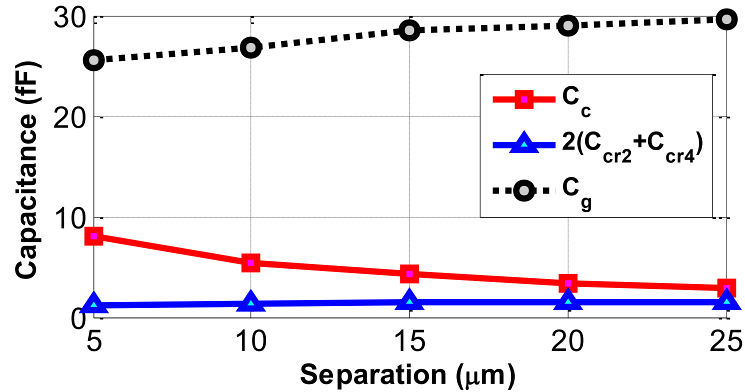


Figure 2.6 Simulated capacitance vs. plate separation.

an adjacent channel is expected to be relatively small compared to the coupling capacitance C_c and the parasitic capacitance to ground C_g. Extracted passive element values are shown in Table 2.2.

HFSS simulations were conducted for the same metal plates (95 μm × 52 μm) shown in Figure 2.3 with lateral spacing of 17 μm, which is the minimum spacing from the design rules for I/O pads. The overall capacitance from cross-talk, $2 \times (C_{cr2} + C_{cr4})$ was found to be less than 1 fF. As shown in Figure 2.6, the simulated C_c and C_g were 8 fF and 25.6 fF, respectively, at a separation of 5 μm. As expected, C_g and $C_{cr2} + C_{cr4}$ remain almost the same at wider separation. Both capacitance types increase with increasing separation due to less screening effect from metal plates on the other chip.

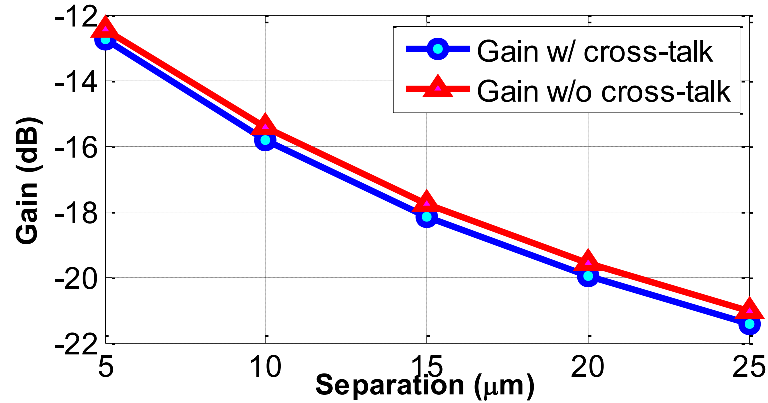


Figure 2.7 Gain comparison with cross-talk effects.

C_c continuously decreases with increasing separation.

From the simulation results in Figure 2.7, we can conclude that the effect of cross-talk is not substantial in capacitive coupling. However, since the cross-talk highly depends on metal plate size and spacing, careful analysis must be done for correct channel characterization.

2.5 Misalignment Tolerance

Since a conventional probe card tester can touch down on a wafer with micrometer precision, misalignment of the channel plates in a capacitively-coupled tester may not be a serious problem. Nevertheless, an analysis of plate alignment is still worth doing to determine the minimum lateral spacing of different channels and reduce the potential cost of high-precision alignment. Like cross-talk, misalignment manifests itself as a change in capacitance. In most cases, misalignment greatly affects coupling capacitance, and so results in gain degradation. In contrast, the parasitic capacitance to ground remains essentially unchanged.

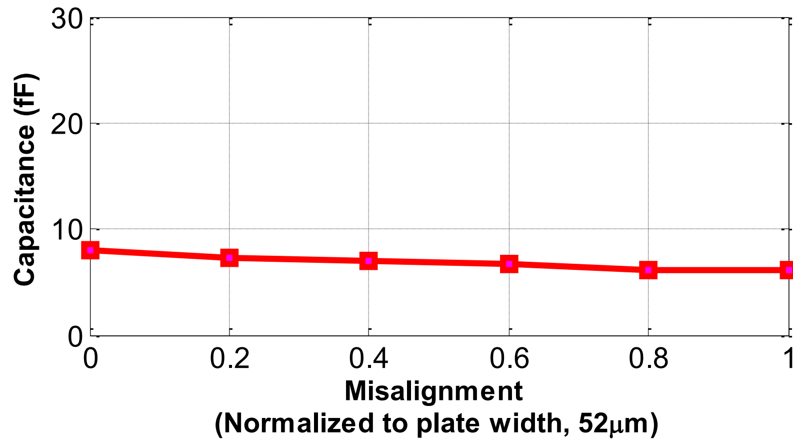


Figure 2.8 Coupling capacitance vs. misalignment.

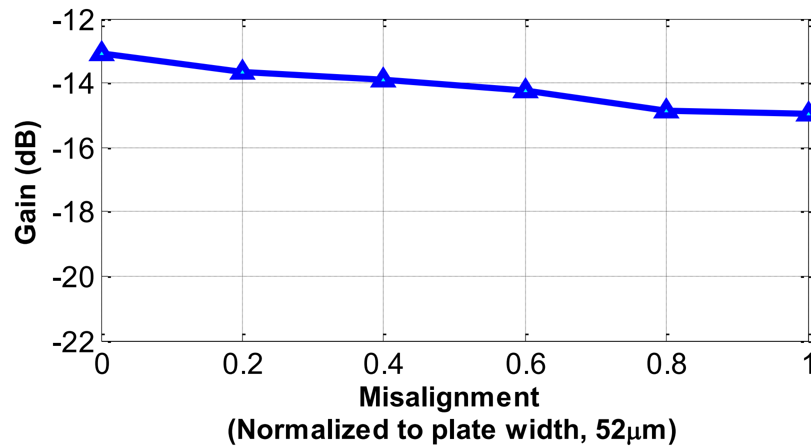


Figure 2.9 Gain vs. misalignment.

The same 3D capacitor model with 5 μm separation has been used for a HFSS simulation of misalignment. The *y*-location of the top metal plate was changed from 0 μm to 50 μm. Since the width of the metal plate is assumed to be 52 μm, a *y*-direction sweep covers most cases of misalignment. Figure 2.8 shows the simulated results. As misalignment increases, the coupling capacitance becomes smaller. However, even for 50 μm misalignment, the capacitance does not decrease significantly with no overlapping of the metal plates.

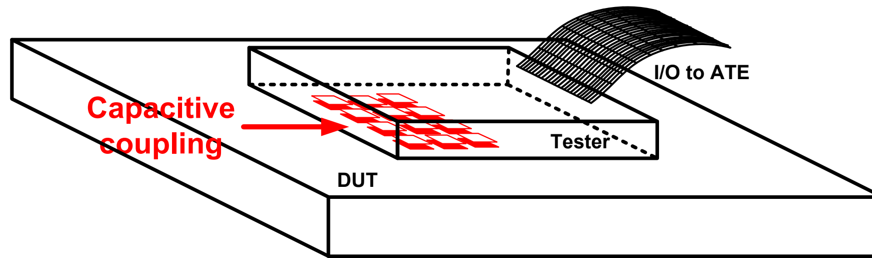


Figure 2.10 Proposed wireless tester.

Compared to the results of cross-talk simulation with similarly located plates, the coupling capacitance is quite substantial. This is believed to be because of fringing effects. There is no material which screens fringing capacitance between diagonally placed plates. Thus, the top and bottom surface of the metal plates can exhibit capacitive coupling in spite of almost no overlapping area.

The effect of misalignment on channel gain is shown in Figure 2.9. Even with the maximum misalignment, the gain decreases by only 2 dB. We can therefore conclude that a capacitively-coupled channel shows good misalignment tolerance up to the size of the metal plates.

2.6 Summary

Wireless testing is an alternative to direct-contact testing of ICs that greatly reduces the costs associated with probe employment and wear. Due to the very short communication range required, capacitive coupling seems the most feasible wireless communication technology for this application. We have presented analytical models and simulation results that support the validity of this approach. They demonstrate that the gain of a capacitively-coupled channel can be easily predicted. Moreover, our cross-talk

and misalignment results indicate that capacitive coupling experiences relatively low adjacent channel interference, and has good misalignment tolerance. In summary, capacitively-coupled wireless testing of the kind depicted in Figure 2.10 offers an attractive alternative to conventional wafer probing.

Of course, there are other issues that need to be addressed to make wireless testing at the wafer level practical. These include tester reconfiguration, wireless power transfer, and low-power test circuits. These issues can be mitigated by various circuit techniques. For example, tester reconfiguration may be implemented using a shared channel with various multiple-access schemes such as time division multiple access (TDMA) or code division multiple access (CDMA). Wireless power transfer through capacitively-coupled channels has been proposed in [11], but the deliverable power is still very limited. Therefore, we propose a hybrid approach. The data links are based on wireless communication, but the wired power connections are assumed. Although power connections usually remain wired, it is still very beneficial to reduce the number of I/O signals requiring probe touch-down [69].

Chapter III

Single-Channel Capacitive Link for Wireless Testing

This chapter presents a single-channel I/O link intended for wireless integrated circuit testing via capacitive coupling. A wireless testing system with a simple CDR architecture based on the proposed capacitive channel model is presented. DC-level fluctuation from PWM is estimated from an analytical model. The measurement data from a fabricated prototype chip validate the model and its predicted performance. The material in this chapter appears in [35].

3.1 Introduction

Wireless testing requires extra circuits and antennas on the die, which should not consume too much chip area. Additionally, the functionality of the original device should not be affected by the components added for testing. Electrical power also needs to be delivered wirelessly to completely remove wired lines during testing. However, as long as the number of signal pads is a significant fraction of the total number of I/O pads, wireless testing only of signal pads with wired power can still be beneficial due to the significant reduction of the touch-down force [69]. In addition, the data rate needs to be

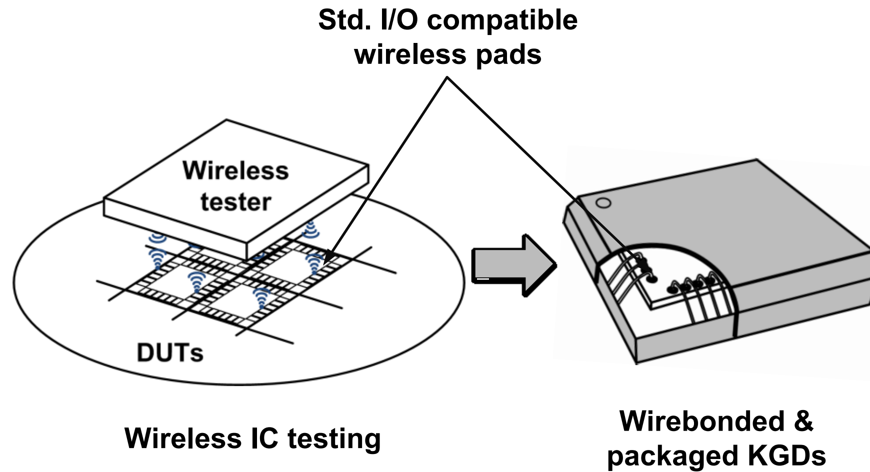


Figure 3.1 Proposed capacitively-coupled wireless IC testing with bond pads compatible with standard I/O cells.

sufficiently high to support at-speed testing for state-of-the-art I/O technologies with gigahertz communication [72].

We propose a wireless testing scheme based on capacitive coupling as shown in Figure 3.1. Although inductive coupling supports a longer communication distance, capacitive coupling is more practical for probe card replacement in ATE. First, the communication distance of wireless testing can be very short since there is only a passivation layer between a tester and DUTs, which is usually less than 10 μm thick. The channel gain of capacitive coupling is comparable to that of inductive links at such short communication distances [34]. Second, capacitive coupling can be implemented with I/O bond pads as the antennas. As depicted in Figure 3.1, if we reuse this antenna as a normal wired bond pad after wireless testing, there is no additional area requirement. In contrast, inductive coupling requires dedicated transformers, which require complex design techniques and considerable additional area.

Capacitively-coupled I/O links have been proposed for various applications: long-range on-chip communication [19][74], 3D chip-to-chip communication [15][17], and

wireless IC testing [12][30][31][34][69]. Most of them demonstrate gigahertz data rates with synchronous or asynchronous communications, but all require an additional clock channel. In order to use bond pads as antennas, single-channel communication with CDR is necessary.

To implement a single-channel link, we propose utilizing PWM to embed a clock into the data stream. Bit-slicing by multi-phase clocks generated through a delay-locked loop (DLL) can be used for data regeneration from PWM signals. However, PWM signaling introduces DC offsets at the receiver because PWM symbols are not DC-balanced. Due to limited gain and bandwidth of the receiver amplifier, the DC level fluctuation is reflected as a pulse-width change after amplification. Since PWM encodes data bits in the pulse width, this fluctuation eventually affects the bit-decisions of the receiver. In [9], ternary DC-balanced symbols are used to mitigate the DC fluctuation. However, three symbols are used to express binary numbers, which sacrifices data rate for BER reduction. The decision feedback equalization (DFE) technique was introduced in [21] to address this issue as well, but it requires power- and area-consuming analog implementation.

Instead, we propose a feed-forward clock selector, which dynamically chooses proper clocks for bit-slicing based on prior data bits. Binary symbols make the modulator on the transmitter side relatively simple. The clock selector is implemented with all-digital circuits so that it can leverage further technology scaling. The proposed prototype shows that binary PWM with the feed-forward clock selection greatly alleviates DC-balancing.

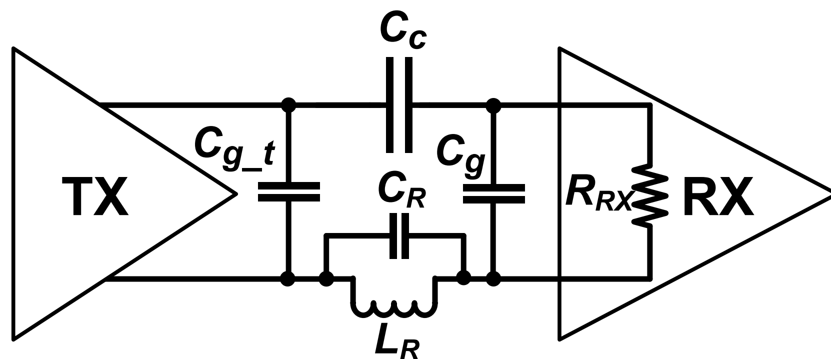


Figure 3.2 Lumped circuit model of a capacitive channel between a DUT and ATE.

A data rate up to 900 Mbps has been achieved with a prototype chip intended for capacitive wireless IC testing. A BER of $<10^{-13}$ was measured with the proposed DLL bit-slicer with feed-forward clock selection. The capacitive channel was emulated with surface-mounted capacitors on a PCB.

3.2 Channel Modeling and Modulation

This section describes an analytical lumped model for the single-channel capacitive link. The capacitive channel is simulated with an electro-magnetic (EM) simulator. In addition, PWM signaling and DC-fluctuation due to DC-unbalanced PWM will be discussed.

3.2.1 Capacitive Channel Model

The voltage transfer function of capacitive coupling can be specified with passive lumped elements as follows, where $H(s)$ is defined as V_{RX}/V_{TX}.

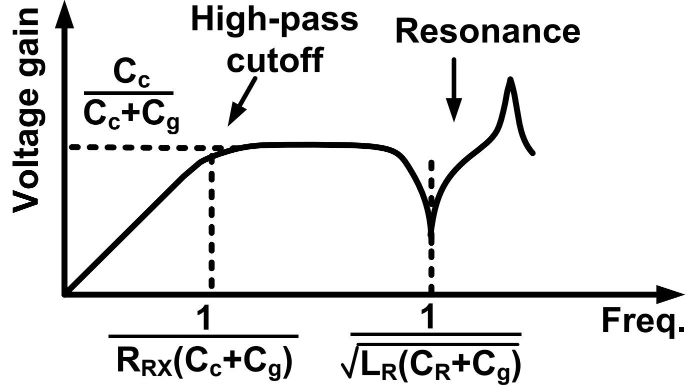


Figure 3.3 Frequency response of the proposed voltage transfer model.

$$H(s) = \frac{s\left\{s^2 L_R R_{RX} C_c \left(C_g + C_R\right) + sL_R C_c + R_{RX} C_c\right\}}{\left(\begin{array}{l} s^3 L_R R_{RX} \left\{C_R \left(C_c + C_g\right) + C_c C_g\right\} \\ \qquad\qquad + s^2 L_R \left(C_c + C_R\right) + sR_{RX} \left(C_c + C_g\right) + 1 \end{array}\right)} \tag{3.1}$$

C_c represents the coupling capacitance between a transmitter (TX) and a receiver (RX). Both transmitter and receiver ports have parasitic capacitances to ground, which are denoted as C_{g_t} and C_g in Figure 3.2. Since the DUT and ATE have different designs, these ground capacitances are different. R_{RX} is the input impedance of the receiver. C_R and L_R are parasitic elements due to current return paths. C_R is intentionally placed for AC ground coupling to reduce the effect of L_R caused by a long current return path. This model is based on (2.2), but it includes the RX input impedance, R_{RX}. To check how *H(s)* changes with different R_{RX} values, we can take the partial derivative of *H(s)* with respect to R_{RX}.

$$\frac{\partial H(s)}{\partial R_{RX}} = \frac{k}{\left(l \cdot R_{RX} + m\right)^2} \tag{3.2}$$

Here, k, l, and m are positive constants independent of R_{RX}. Since (3.2) is always positive for positive values of R_{RX}, the voltage gain of the channel monotonically increases with increasing R_{RX}. Therefore, to maximize the channel voltage gain, input impedance R_{RX} should be kept as large as possible. Assuming infinitely large R_{RX}, $H(s)$ becomes identical to (2.2).

A simplified plot of the frequency response for the model is shown in Figure 3.3. The high-pass cutoff frequency of the voltage transfer function is given by $R_{RX} \times (C_c + C_g)$. Parasitic inductance L_R contributes to resonance and makes the channel gain dramatically decrease at the resonant frequency. Small L_R is desirable for a wide frequency band around a target frequency in order to push the resonance to a very high frequency. At the same time, large C_R is preferred to mitigate the effect of L_R by canceling the resonant null. Between the first high-pass cutoff frequency and the resonant frequency, the voltage gain of the channel can be simply written as

$$H(s) = \frac{sR_{RX}C_c}{sR_{RX}(C_c + C_g) + 1} \approx \frac{C_c}{C_c + C_g} \qquad (3.3)$$

where R_{RX} is very large and parasitic effects are ignored. The voltage gain is roughly proportional to the ratio of C_c to $C_c + C_g$. Based on (3.3), C_c should be kept large enough to make the voltage gain high. Since the channel gain is a ratio of capacitances, as long as the ratio is the same, we can achieve the same channel gain with different capacitance values. Due to difficulties in alignment of the prototype ICs in our test setup, surface-mounted capacitors on a PCB were used to emulate a capacitive channel between a DUT and ATE. Because of the parasitic capacitance from package and PCB trace, the measured lowest gain of a capacitive channel for proper operation is –14 dB when we use

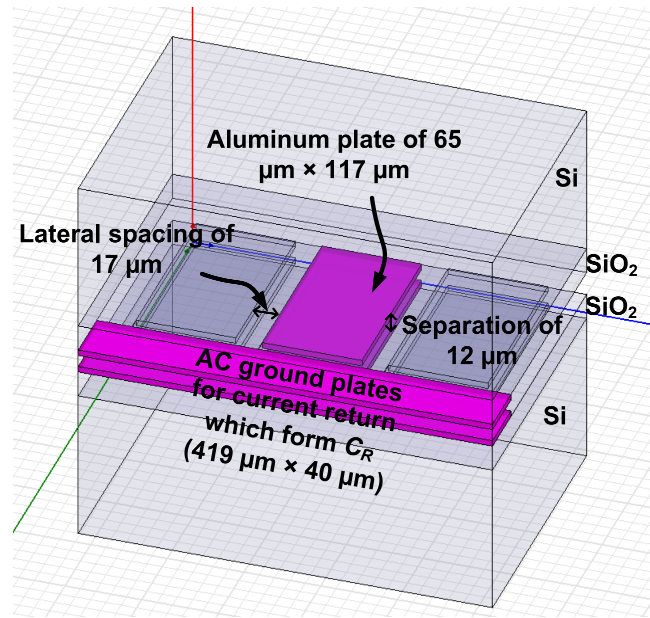


Figure 3.4 3D model for EM simulation by HFSS v11.

a 500 fF capacitor for C_c and C_g. From simulation and back calculation, an actual C_g of 2.5 pF is expected due to added parasitic capacitance.

EM simulations (using Ansoft HFSS v11) with the standard I/O 3D model were conducted to compare the measured channel gain from emulation with surface-mounted capacitors. The worst-case cross-talk scenario in Chapter 2 is also considered in the simulation. The bond pad model is made of an aluminum layer with a thickness of 4 µm and area of 65 µm × 117 µm, as shown in Figure 3.4. Adjacent channels are placed with a 17 µm lateral spacing, which is the minimum spacing allowed by the design rules for I/O pads. A long ground plate of area 40 µm × 419 µm is used to provide good AC current return paths, which reduces the effect of parasitic inductance. After wireless testing, these plates are used as shared ground strips for the standard I/O pads. The –14dB gain is equivalent to the EM simulated gain with 12 µm separation between the DUT and ATE, assuming no additional capacitive load at the input to the receiver. The gain degradation

Table 3.1 Detailed passive element values from EM simulation with 12 μm spacing.

C_c	5.58 fF
C_g	22.4 fF
C_{cr2}, C_{cr4}	0.8 fF
C_R	8 fF
L_R	1 nH *
R_{RX}	40 kΩ**

* Parasitic inductance is assumed for 1-mm wire-bonding.
** R_{RX} is limited by an on-chip series resistor for DC biasing.

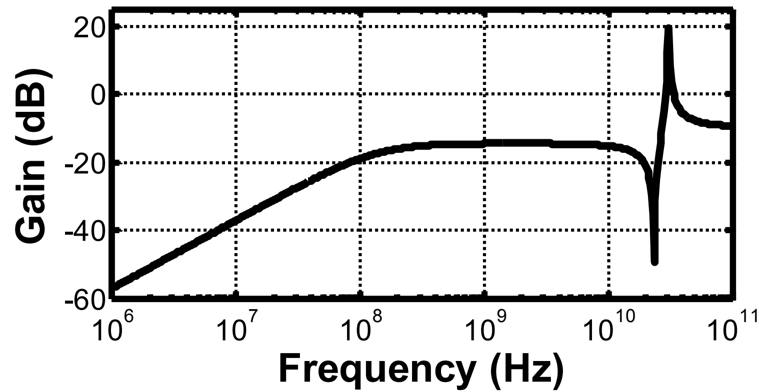


Figure 3.5 Spice simulated frequency response of a channel with a proposed lumped model.

from cross-talk was simulated as well. Cross-talk capacitance extracted from simulation results was included in the proposed lumped model, and the resulting degradation of voltage gain was calculated. The overall cross-talk capacitance of $2 \times (C_{cr2} + C_{cr4})$ is less than 1 fF, which is less than 5% of C_g, and the resulting degradation of the voltage gain is less than 1 dB. The effect of cross-talk is expected to be negligible, but it highly depends on the pad size and separation.

Extracted passive element values with 12 μm distance are shown in Table 3.1. With these values, the high-pass cutoff frequency is calculated as around 150 MHz, and the resonant frequency is calculated as 20.6 GHz. Targeting a 1 Gbps data rate for

wireless IC testing, the channel response is relatively flat around the target frequency. The simulated overall frequency response is plotted in Figure 3.5.

3.2.2 Pulse Width Modulation

For both very high-speed wired and wireless communication, synchronization is of the utmost importance since demodulation and data recovery highly depend on clock timing. For the interface from the front-end capacitive links to the ATE design, most interconnections will be implemented on PCBs or off-chip cables, which significantly contribute to parasitic capacitance and inductance. In addition, the number of I/O pins is already more than several thousand and is constantly increasing [72]. Therefore, timing uncertainty in high-speed signals for a wireless IC tester has a significant impact on reliable communication. A reference clock could be sent through an extra channel independent of the data channel to resolve timing issues, but in wireless IC testing, such an additional channel is area-consuming, and the interconnections from the added clock channel to other data channels may be unrealistic. Instead, we propose using PWM, which modulates data based on the pulse-width change. The rising edge contains clock information, and data are modulated at the location of the falling edges in the time domain. Thus we lose 50% of the signal for clock synchronization. However, the PWM simplifies the receiver design by removing the requirement of synchronization based on a complex phase-locked loop (PLL) because rising edges contain the embedded clock information. If a DLL with a positive-edge sensitive phase detector locks to a 1-cycle delayed version of the input PWM signal, proper rising edges can be used for bit-decision. Also, PWM signals are advantageous due to less cross-talk from adjacent channels. Data

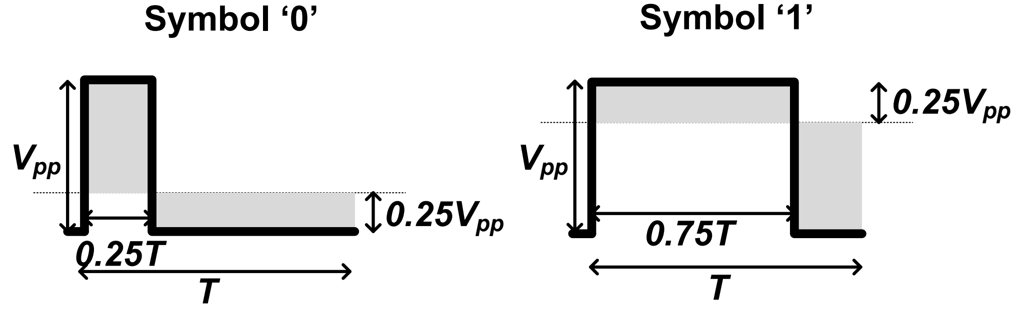


Figure 3.6 PWM bit symbols for '0' and '1'.

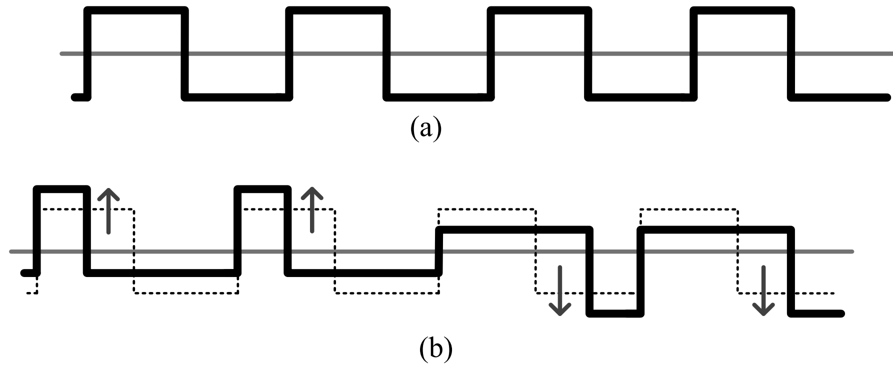


Figure 3.7 Illustration of signal level fluctuation, (a) DC-balanced 50% duty-cycled signals, (b) DC-unbalanced PWM signals with '0011'.

are encoded on the locations of falling edges, and rising edges are all synchronized in PWM signals. Therefore, there is no worst-case Miller coupling capacitance between adjacent channels due to no simultaneous switching in opposite directions. With PWM, C_g can be re-written as $C_g = C_{g_original} + C_{cr2} + C_{cr4}$, and therefore there is less cross-talk effect on the voltage gain.

The proposed bit symbols are depicted in Figure 3.6. A 25% duty cycle represents '0', and a 75% is for '1'. Since these symbols are not DC-balanced, the DC level of the received signals fluctuates with the data pattern as shown in Figure 3.7. The maximum fluctuation is analyzed in the next section. In the worst case, the signal level shifts by a maximum of $\pm 0.25V_{pp}$. Since the target data rate is 1 Gbps, the pulse width of

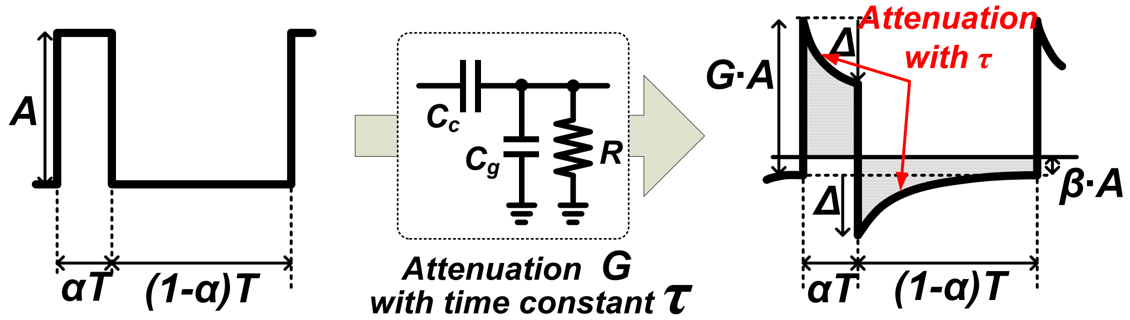


Figure 3.8 PWM signals passed through a capacitive channel.

symbol '0' is 250 ps, and the pulse width of symbol '1' is 750 ps. Due to the limited gain and bandwidth of the receiver amplifier, the DC-level fluctuation is reflected as pulse-width fluctuations after finite-bandwidth amplification.

3.2.3 Estimation of Pulse-Width Variation

The DC level of PWM signals will move up and down at the receiver depending on data values. As shown in Figure 3.8, the DC level of the original PWM symbol with 25% duty cycle is moved by $0.25V_{pp}$ from the center. Furthermore, assuming that a capacitive channel is simplified as the first-order high-pass transfer function, the DC level of PWM signals highly depends on time constant, τ. The quantity $\beta{\cdot}A$ is defined as the DC voltage level from the initial value where A is the peak-to-peak signal amplitude. The PWM signals passed through the channel decay exponentially with the first-order high-pass characteristic, and the resulting DC level sets where the integration of the symbol over one period equals zero. With these relationships, we can represent β with a duty cycle factor α, the period of the symbol T, the time constant of the channel τ, and the attenuation G as follows.

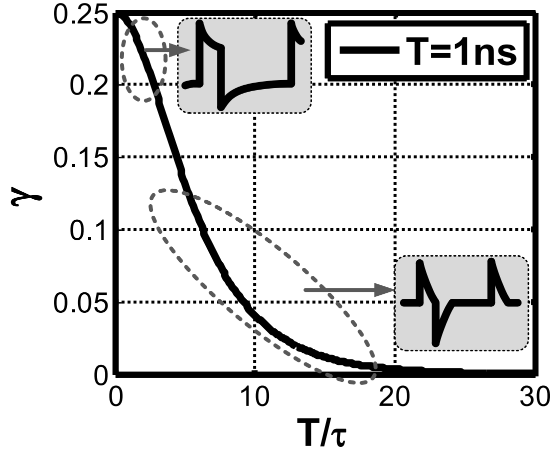


Figure 3.9 DC offsets from the center level for PWM signals (T = 1 ns, α = 0.25).

$$\beta = \frac{e^{\alpha T/\tau} - 1}{e^{T/\tau} - 1} \cdot G \tag{3.4}$$

With (3.4), we expect DC-level offsets from the center line with different T/τ values as plotted in Figure 3.9 assuming a period of T = 1 ns. The DC-offset factor γ is defined in (3.5) as a DC offset from a half of the peak-to-peak amplitude voltage, where Δ is the voltage drop of the pulse due to the high-pass characteristic of the channel in Figure 3.8.

$$\gamma = \frac{0.5 \times (\Delta + G \cdot A) - (\Delta + \beta \cdot A)}{A} \tag{3.5}$$

To estimate DC-level fluctuations, pulse-width variation was simulated in Matlab. The simulation uses an ideal low-pass amplifier with pass-band gain G and a 1.5 GHz cutoff frequency. The pulse width is measured at the output of a comparator, which has a reference voltage of 400 mV. This reference level also corresponds to the approximate threshold voltage of an inverter in 0.13 μm CMOS. To maximize the variation in the DC

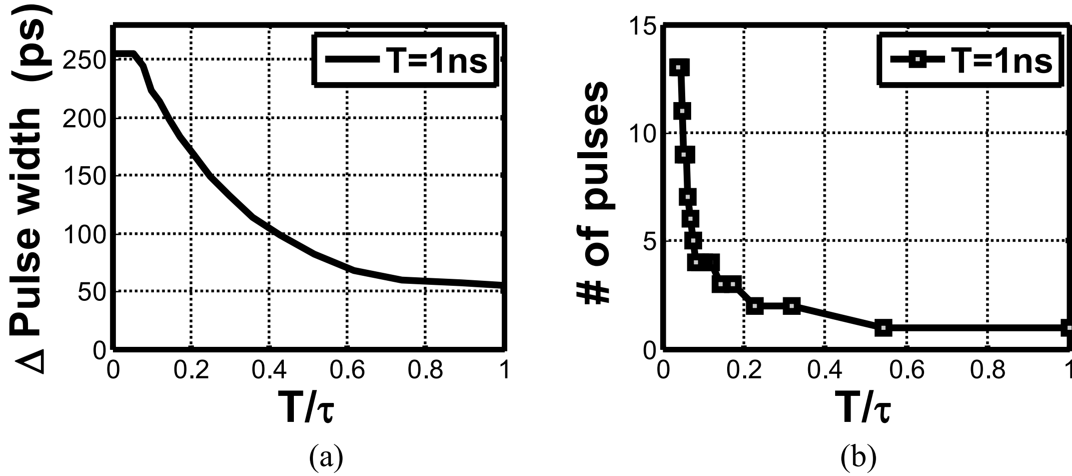


Figure 3.10 Matlab simulation results of (a) the maximum pulse-width variation, and (b) the number of pulses to achieve the maximum variation (T = 1 ns, α = 0.25).

level, a long run of '1' symbols is passed through the channel and the amplifier, followed by a run of '0' symbols.

The simulation results for varying T/τ are shown in Figure 3.10(a). If T/τ is larger than 0.8, the amplifier cannot regenerate pulse-width information since the ideal comparator cannot detect the pulse-width change. The channel is highly band-limited in this case, and the output looks like an impulse without pulse-width information. Therefore, T/τ larger than 0.8 cannot be used for PWM signals. When T/τ is smaller than 0.05, the pulse-width change saturates at the maximum value of 254 ps. Meanwhile, Figure 3.10(b) shows the number of pulses required to maximize the variation in the DC offset. It turns out that the time to achieve the maximum variation is inversely proportional to T/τ.

These observations for the maximum pulse-width variation and the number of pulses for the maximum variation can be employed to improve the BER performance of the demodulator. To mitigate the effect of pulse-width changes, we propose a feed-

forward clock selector which dynamically avoids incorrect bit decisions by predicting pulse-width changes from previous data patterns. The feed-forward clock selector was designed with the estimated variation above. A proper T/τ value for relatively simple circuit implementations is chosen based on the following strategy.

A large T/τ is not always helpful since the voltage level decays too quickly for the comparator to function correctly. In this case, the recovered PWM signals do not contain pulse-width information. As we have shown above, a T/τ of less than 0.8 is appropriate. A large T/τ sacrifices the pulse amplitude as well. A small R_{RX} value is required to increase T/τ for a fixed $C_c + C_g$ value as shown in (3.2), which means that the signals suffer from more attenuation.

However, if T/τ is too small, the output results in a large variation of pulse widths and a slow step response in the channel. Therefore, it is difficult to predict the instantaneous change of the DC level with relatively short data patterns. For example, a T/τ of less than 0.05 requires a run of more than 13 bits to have the maximum pulse-width variation. In this case, the feed-forward selector needs to store and process at least 13 bits for accurate DC-offset prediction.

Based on this analysis, a value of 0.15 was selected for T/τ considering on-chip implementation of R_{RX} and $C_c + C_g$. The trade-off between the maximum pulse-width variation and the received signal amplitude was also investigated while choosing the T/τ value. After four consecutive bits, the pulse-width change is saturated at the estimated maximum value. Although the resulting τ contributes to the pulse-width change by up to 194 ps, this effect can be minimized with a relatively simple feed-forward clock selector. The design of the feed-forward clock selector itself is discussed in a later section.

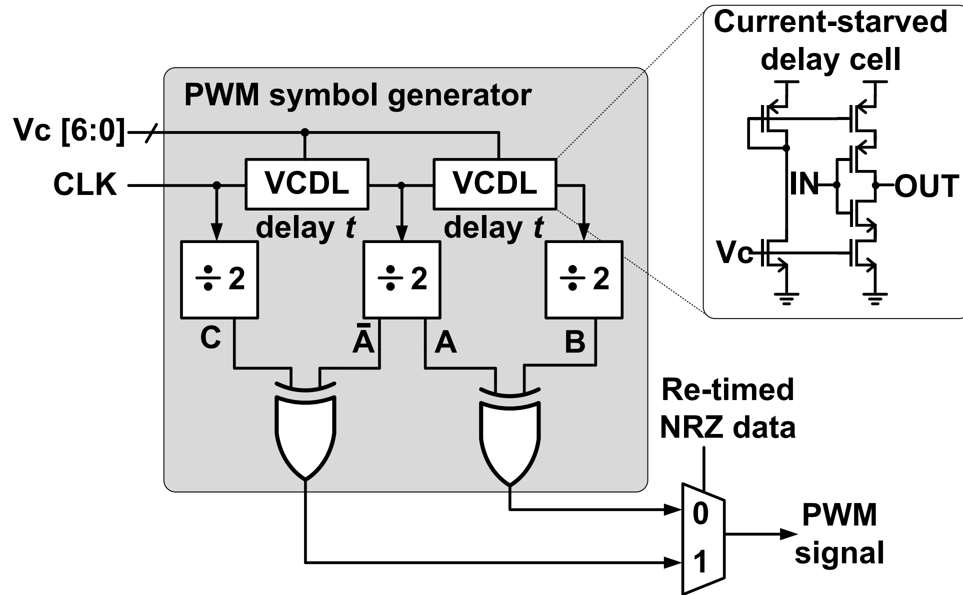


Figure 3.11 PWM modulator with an XOR-based edge combiner.

3.3 Overall Architecture

This section presents the circuit implementation of the proposed I/O link. It covers a PWM transmitter, and a DLL-based bit-slicing receiver with a 1-cycle phase detector and a feed-forward clock selector.

3.3.1 PWM Transmitter

The transmitter consists of a PWM modulator and a pad driver. Figure 3.11 describes the PWM modulator that modulates non-return-to-zero (NRZ) signals. The pad driver is shown in Figure 3.13. A conventional current-starved delay line is used to generate a fixed delay *t*, which can be tuned by a 7-bit off-chip digital code. The clock is delayed by *t* and 2*t*, and divided by two, as denoted by A and B in Figure 3.12. After delayed versions of the clock with half frequency are generated, an XOR-based edge

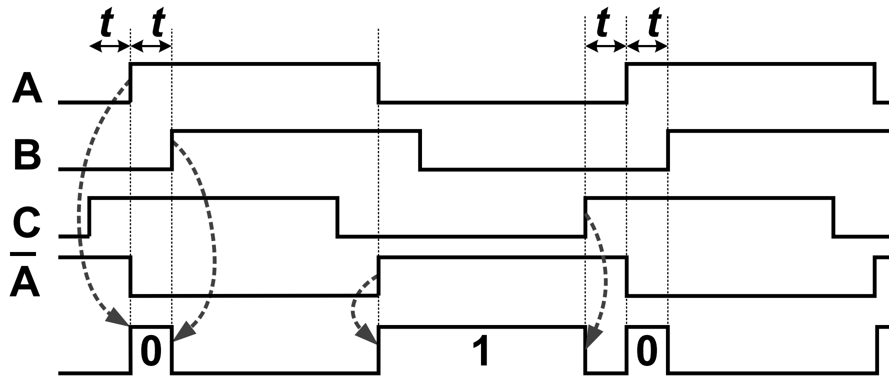


Figure 3.12 Symbol generation for data '010'.

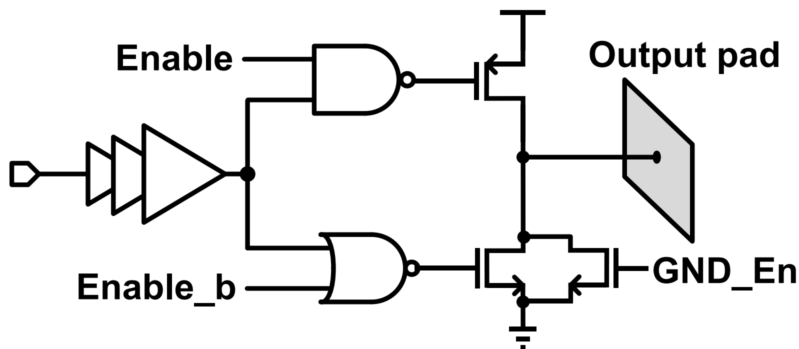


Figure 3.13 Output pad driver with a tri-state inverter.

combiner selects proper edges for PWM symbols '0' and '1'. For example, both the rising and falling edge of A and B are combined to generate symbol '0', and edges of C and Ā are selected for symbol '1'. The output multiplexer then chooses the right symbols based on the re-timed NRZ data.

The pad driver in Figure 3.13 is a digital inverter chain supporting tri-state outputs for the reconfiguration of the transmitter and receiver. It supports on, ground, and high impedance modes. When an I/O link is configured as a receiver, the pad driver is configured as high impedance so as not to affect the receiver operation. In transmit mode, a digital inverter that can drive the pad rail-to-rail is required to maximize the

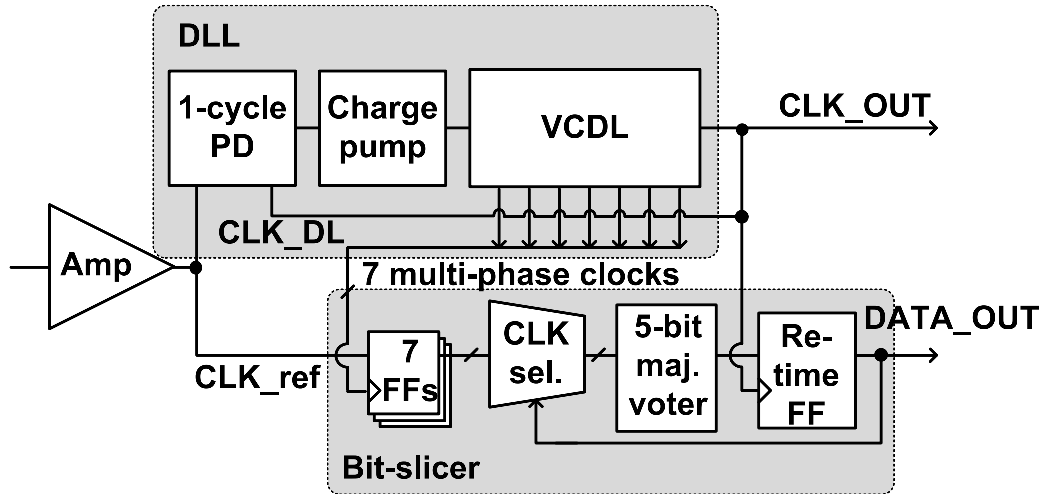


Figure 3.14 Overall block diagram of the proposed DLL-based bit-slicing receiver.

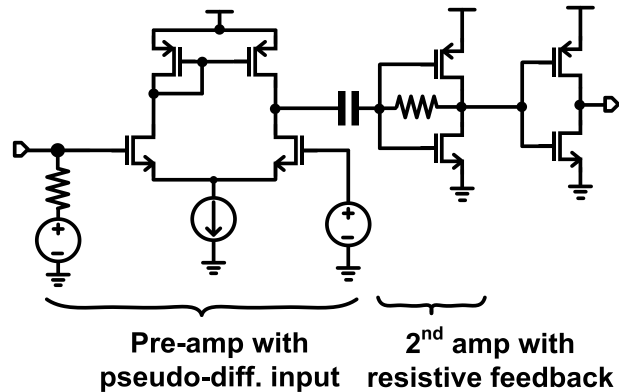
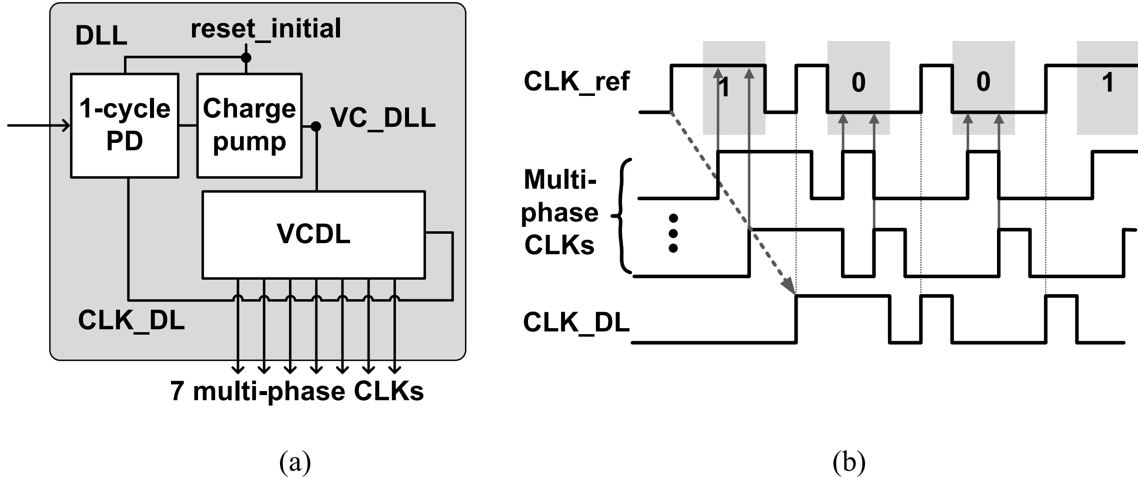


Figure 3.15 Schematic of the 2-stage receiver amplifier.

voltage at the input to a receiver. The inverters are carefully sized to drive capacitive loading from parasitic and electro-static discharge (ESD) protection circuits.

3.3.2 DLL-Based Receiver

Figure 3.14 shows the block diagram of the DLL-based receiver. It consists of a receiver amplifier, a DLL, and a bit-slicer with a feed-forward clock selector. The schematic of the receiver amplifier is given in Figure 3.15. For the PCB-level emulation of capacitive channels, only relatively large C_c and C_g are available, and they result in



(a) (b)

Figure 3.16 (a) Block diagram of the DLL, and (b) operation of bit-slicing with multi-phase clocks.

higher τ than the value estimated in the previous section. To resolve this, the amplifier consists of the low-pass pre-amplifier and the band-pass second amplifier. The high-pass cutoff frequency of the band-pass amplifier is set to the expected τ.

The input port of the pre-amplifier is directly connected to the gate of one of the input transistors to maximize the input impedance and the received signal amplitude. Since a capacitively-coupled channel model is basically a voltage divider, the input impedance of the receiver should be as large as possible to maximize received signal swings. The other input for a differential pair is grounded with an internal DC reference voltage. For the second stage, a resistive feedback inverter is used due to its self-biasing characteristic and small area consumption. The overall gain of the multi-stage amplifier is around 27.2 dB and the 3-dB bandwidth is from 150 MHz to 1.5 GHz. At the output of the amplifier, an inverter chain regenerates the amplified signals to full-swing digital signals.

The DLL-based demodulator is shown in Figure 3.16. For details of CDR with PWM, please see Appendix B. After the amplification stage reconstructs PWM signals to

rail-to-rail, a DLL locks to its 1-cycle delayed version, since a phase detector (PD) is only sensitive to rising edges. The DLL generates multi-phase delayed clocks in between the incoming signals and the 1-cycle delayed version. If we choose the proper clock edges placed in the middle of the range where data are encoded, a positive edge-sensitive flip-flop can demodulate PWM to NRZ signals. The multi-phase clocks can also be used to reduce the BER. We take 5 different phased clocks and reconstruct 5 NRZ signals used in a majority voter to determine the received bit. The overall DLL-based demodulation process is depicted in Figure 3.16.

The elements of a voltage controlled delay line (VCDL) are implemented with conventional current-starved delay cells. Generally, an XOR-based PD and VCDL with an initial delay of around one cycle can be used in order to make the DLL lock to a 1-cycle delayed version of the incoming signal. However, this approach is prone to a harmonic-locking problem, and a VCDL with a long initial delay consumes substantial area. Instead, we propose a 1-cycle PD; a modified version of a phase frequency detector (PFD), as illustrated in Figure 3.17. The PFD starts comparing phase when the rst_initial signal is deasserted. However, the proposed PD still remains off and starts its operation just after the first rising edge passes due to the added flip-flop at the bottom. It moves the locking phase from 0 to 2π, and forces the delayed output to lock to the second rising edge.

In Figure 3.17, a conventional PFD is shown that keeps pushing a delayed version of the clock forward with an UP signal. However, the proposed 1-cycle PD skips the first rising edge of the clock and delays it by asserting a DN signal, resulting in 1-cycle locking. UP and DN control signals from the proposed PD convert this phase information

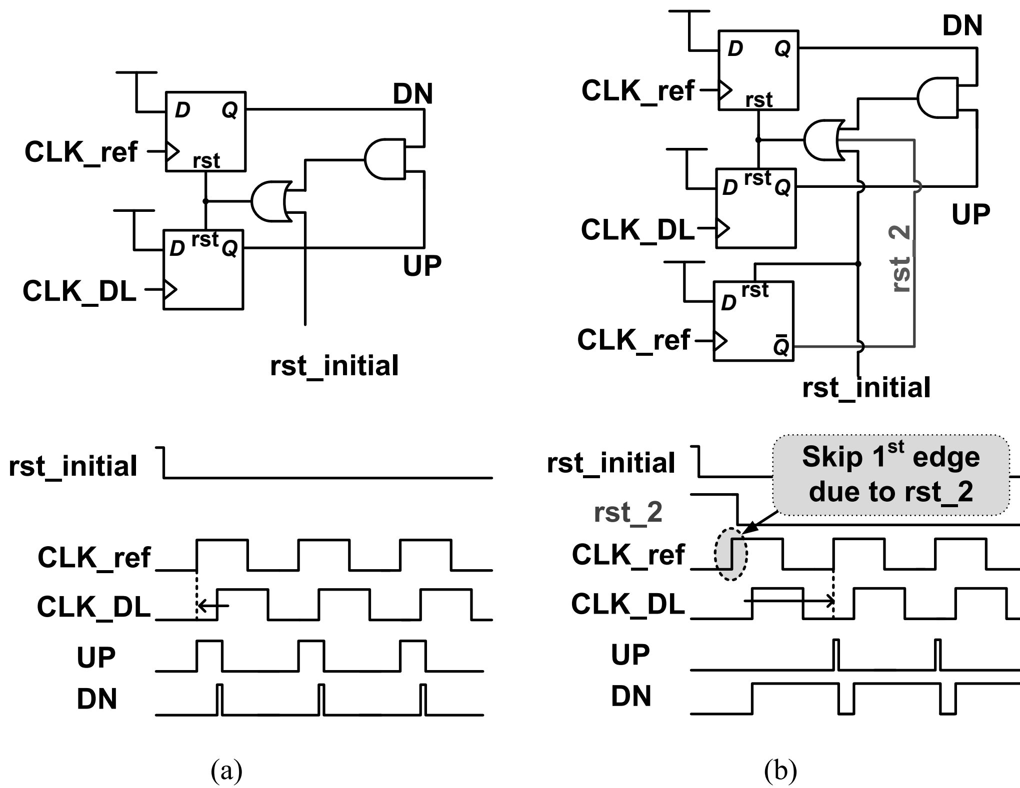
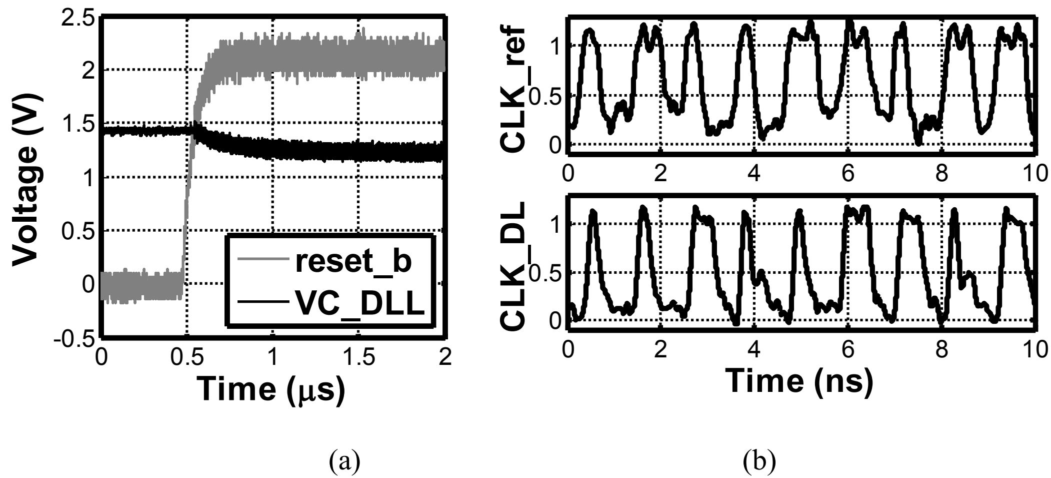


Figure 3.17 Phase-locking characteristics of (a) conventional PFD, and (b) proposed 1-cycle PD.

to voltage using the current-steering charge pump (CP) with a regulated output node, as proposed in [86], which provides low phase offset since it regulates the drain voltage of dummy switching transistors to output node voltage to maintain constant current.

Once the DLL locks to the 1-cycle delayed versions of the PWM signal, a total of seven different phased clocks are generated by the VCDL and are used for bit decisions. Among the seven outputs from the bit-slicing flip-flops, five are chosen by the feed-forward clock selector, and a bit decision is made by majority voting from these five. The loop filter is made from a 1 pF on-chip metal-insulator-metal (MIM) capacitor, and the CP is implemented with 40 μA current.

Measured results of the implemented DLL are shown in Figure 3.18. The measured locking time is 0.45 μs, and is dominated by the capacitance added to the loop



(a) (b)

Figure 3.18 Measurement results from the implemented DLL: (a) step response, and (b) in/output PWM waveforms.

filter. The bond pad, ESD protection circuits, and PCB traces contribute to the capacitance of the loop filter. However, large capacitance makes the loop more stable, and therefore enhances the disturbance-rejecting performance. Figure 3.18 also shows input and output PWM waveforms for the DLL. The input PWM signal successfully locks to its 1-cycle delayed version.

3.3.3 Feed-Forward Clock Selector

As we explained in a previous section, the pulse width of AC-coupled PWM signals starts fluctuating in response to DC-level fluctuations. This fluctuation is highly dependent on the data pattern. For example, if there are consecutive ‘0’ symbols, the signal level starts moving up. This will happen with sequences of ‘1’s in the same manner, moving the signal level down. Such fluctuation is reflected as pulse-width change after the finite-bandwidth amplification. For consecutive ‘0’s, the resulting PWM suffers from widened pulses. The increased or decreased pulse width reduces the range of successful data detection, and eventually increases the BER. Based on our transient simulations, the

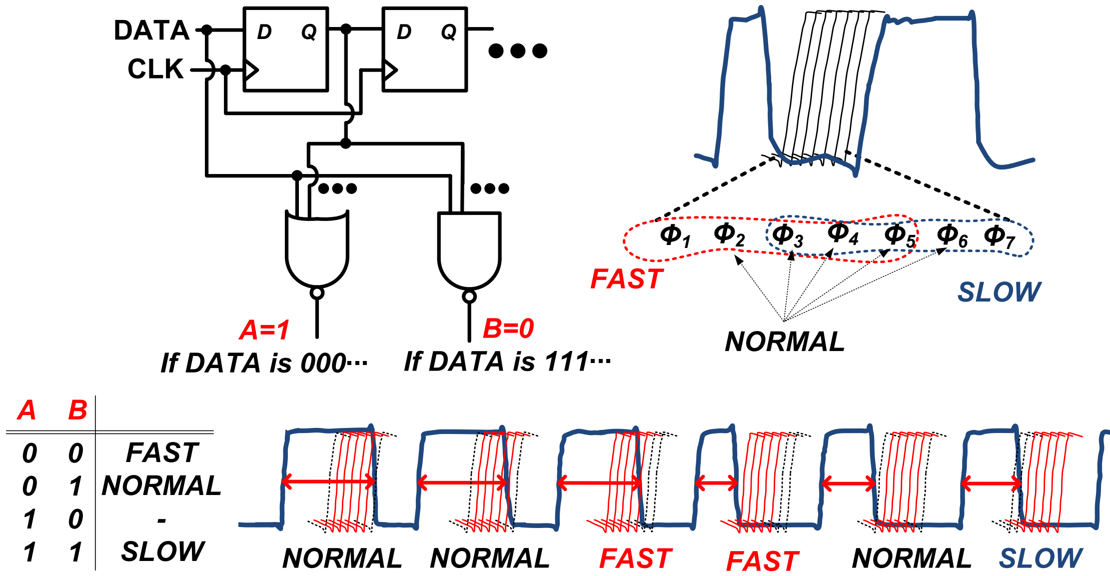


Figure 3.19 Feed-forward dynamic clock selector for signal-level fluctuation.

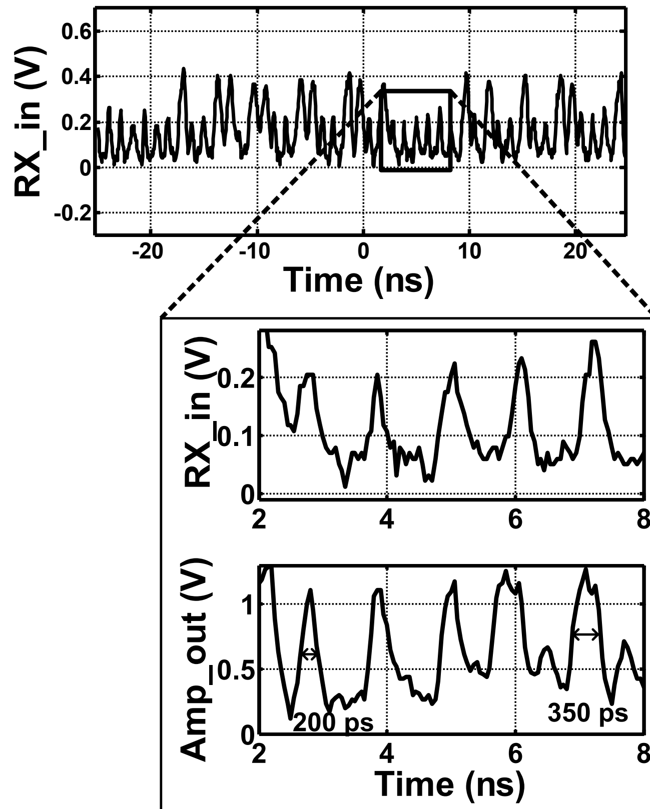


Figure 3.20 Measured pulse-width changes due to signal level fluctuation.

maximum pulse-width change is 194 ps (about 20% of the period) for consecutive runs of either '0's or '1's.

To overcome DC-level related pulse-width changes, we propose a dynamic feed-forward clock selector, which dynamically selects the clock edges for bit decision. Consecutive bits can be detected with NAND and NOR gates and flip-flops as shown in Figure 3.19. We use a total of 7 multi-phase clocks from the DLL and group them into three sub-groups, *FAST*, *NORMAL* and *SLOW*. Based on the truth table in Figure 3.19, the feed-forward selector dynamically chooses the proper sub-group. For example, if consecutive '0's are detected, it chooses *SLOW* edges. Similarly, if consecutive '1's are seen, the clocks of the FAST group are selected for bit decision. In other cases, it uses the *NORMAL* group of edges. We detect only two consecutive bits for a relatively simple circuit implementation, but based on channel response simulations two is sufficient to avoid wrong bit decision.

Simplified operation of the clock selector is depicted in Figure 3.19. If the pulse width is increased, a clock selector pushes the clock edges backward to avoid wrong bit decision, which can occur close to a falling edge. In contrast, the clock selector moves clock edges forward when the pulse gets narrow.

The proposed feed-forward clock selector can be regarded as DFE in the phase domain. However, compared to conventional DFE, it is implemented with much simpler digital circuits, which can leverage further process technology scaling to reduce silicon area and power consumption.

The measured DC-fluctuation with the capacitive channel implemented on a PCB is illustrated in Figure 3.20. Although the DC level of symbols '0' and '1' look different

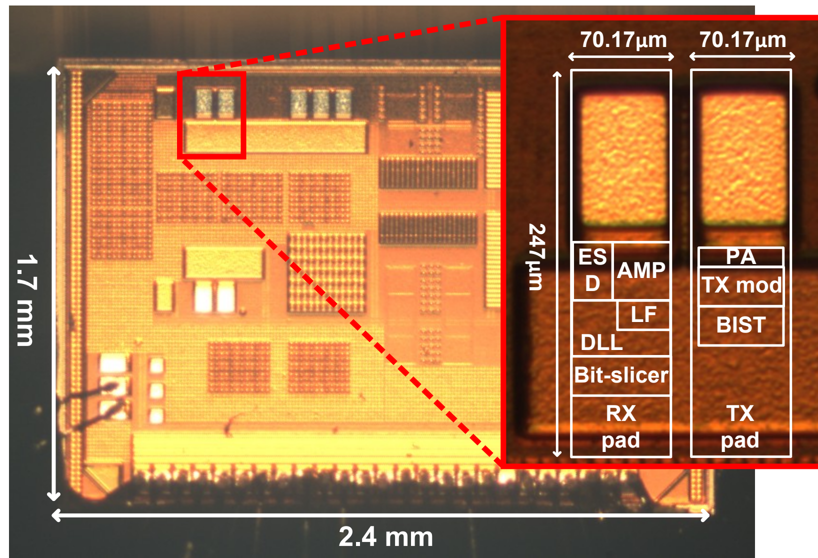


Figure 3.21 Die photomicrograph of the TX and RX pads.

from the original symbols due to the low-pass characteristic of PCB traces, the signal level obviously increases when there are consecutive ‘0’s. After amplification, this level shift is reflected as a pulse-width change. The measured maximum pulse-width change is 150 ps when there are five consecutive bits. After we have more than five identical bits, the pulse width stops increasing and remains constant. Since the measured pulse-width change of 150 ps is smaller than the expected value of 194 ps, the feed-forward clock selector successfully improved BER from 10^{-9} to 10^{-13}.

3.4 Communication Link Measurement Results

The prototype design was fabricated in a 0.13 µm standard CMOS process. The chip photomicrograph is shown in Figure 3.21. The transmitter and receiver are implemented within the boundaries of a standard I/O pad of dimension 70 µm x 247 µm. The total active silicon areas of the transmitter and receiver including ESD protection circuits are 1328 μm^2 and 5041 μm^2, respectively. The overall active area is less than half

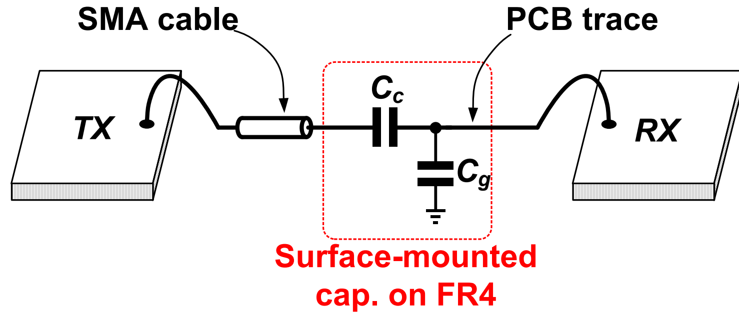
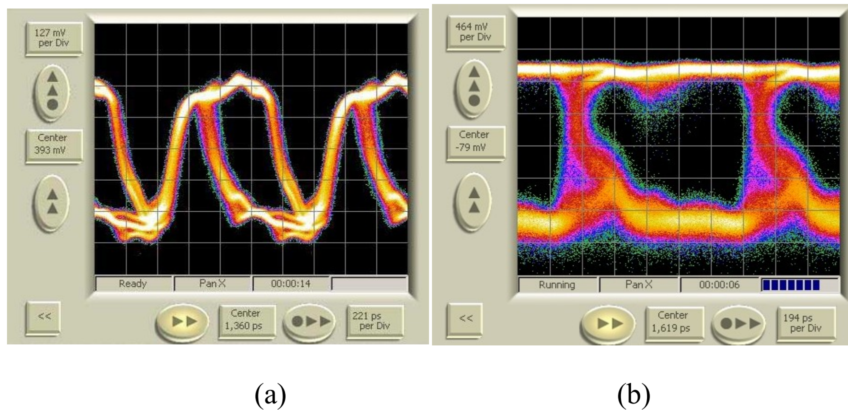


Figure 3.22 Test setup for the prototype link.



(a) (b)

Figure 3.23 Measured eye-diagram of (a) TX PWM signals, and (b) RX output.

the area of a standard I/O cell. To test the implemented I/O links, the output of the transmitter and input to the receiver were wire-bonded off-chip, and connected to a PCB. A capacitively-coupled channel was emulated with surface-mounted capacitors on the PCB, as shown in Figure 3.22. Several capacitance values for C_c and C_g were tested with the prototype to find the maximum channel loss with proper operation. The measured maximum channel loss is −14 dB with a 500 fF capacitor for both C_c and C_g, which is equivalent to 12 μm separation between chips, assuming no additional capacitive loading at the input to the receiver. Since there is parasitic capacitance from the PCB traces and package, the back-calculated C_g including parasitic capacitance is about 2.5 pF.

Table 3.2 Performance summary of the 1st prototype chip.

Technology	0.13 μm CMOS	
Area	Transmitter	1328 μm^2
	Receiver	5041 μm^2
Power dissipation (900 Mbps @ 1.8V)	Transmitter	2.11 mW
	Receiver	5.18 mW
Maximum data rate	900 Mbps @ 1.8 V, 27 ºC	
BER	Feed-forward on	$<10^{-13}$
	Feed-forward off	0.8×10^{-9}
RX V_{DD} tolerance	±10% of 1.9 V (BER $<10^{-12}$)	

The eye-diagrams for the transmitter and receiver outputs are shown in Figure 3.23. A $(2^{18}-1)$-bit pseudo-random binary sequence (PRBS) is generated on-chip through an 18-bit LFSR. The outputs are measured by a Tektronix BSA85C and GB1400 BER tester. The PWM symbols are shown in the eye-diagram of the transmitter output. The measured BER is less than 10^{-13} at a data rate of 900 Mbps. The overall power consumption for the transmitter and receiver is measured as 2.11 mW and 5.18 mW, respectively. Due to the closed-loop regulation of the DLL, the receiver shows a good tolerance of supply voltage variation. It performs with BER below 10^{-12} for ±10% change in supply voltage.

The feed-forward clock selector successfully enhances BER performance. It can overcome a maximum of 150 ps pulse-width change. If we turn off the clock selector, the measured BER is 0.8×10^{-9}. If the selector is on, BER drops to less than 10^{-13}. The major measurement results are summarized and compared with recently published work in Table 3.2.

3.5 Summary

A single-channel capacitive I/O link intended for wireless IC testing has been designed and implemented in a 0.13 μm CMOS process. It uses I/O bond pads as antennas for wireless IC testing to minimize silicon area. To further reduce the area consumed by the antennas, the prototype utilizes PWM signaling, which allows transmission of both a clock and data through a single capacitive channel. A DLL-based receiver with a 1-cycle PD and feed-forward clock selector is proposed to minimize active circuit area and achieve robust communication. The prototype chip demonstrates up to 900 Mbps synchronous communication with BER less than 10^{-13}.

Chapter IV

Non-Contact I/O Pad for Wafer-Level Testing

This chapter presents a non-contact I/O pad for wireless testing. The proposed pad can wirelessly transfer both clock and data signals during testing. Since the pad is also equipped with a digital buffer and ESD protection circuits, it can be used as a normal bond pad after testing. The measured data from die-level experiments are presented and shown to validate the proposed capacitive channel model.

4.1 Introduction

Recently capacitive coupling has been actively researched for wireless testing because bond pads in standard I/O circuits can be reused as antennas, which dramatically reduces the area for additional testing circuits [12][30][31][34][35][69]. We have proposed a single channel capacitive I/O link for wireless IC testing in Chapter 3, which simultaneously delivers both a clock and data with PWM signals. This prototype successfully demonstrated the feasibility of wireless IC testing, but also has a few limitations.

First, antennas need to be loaded by ESD protection circuits in order to be used as normal bond pads after testing. The ESD circuits significantly decrease the signal

strength at the receiver. There exists a trade-off between the received signal strength and the level of ESD protection. More ESD protection results in less signal strength in the receiver. The effect of ESD capacitive loading was underestimated in our previous work. To form a capacitive channel, we used 50 times larger capacitors than the die-level coupling capacitance. Although the effective gain is the same as we simulated, the effect of ESD circuits in the PCB-level emulation is significantly reduced. To be more realistic, the effective channel gain must be very small.

Second, the prototype in Chapter 3 has little flexibility in the selection of data rate and symbols. A relatively simple CDR was implemented with PWM signals, but they are DC-unbalanced and suffer from DC-level fluctuations when they are passed through capacitive links. To mitigate the DC-level fluctuations, we proposed a dynamic feed-forward clock selection scheme. This technique improves BER performance with initially designed PWM symbols, but requires a careful estimation of the maximum pulse width variations. The variations highly depend on the symbol duty-cycle factor and the bandwidth of the channel. Therefore, the feed-forward clock selector is only effective for fixed symbols and channels, and therefore it provides low flexibility in choosing data rate and symbol duty cycle.

Third, capacitive coupling is created on a PCB, not with coupled bond pads, due to difficulties in fine chip-level alignment. Since the signal strength of near-field coupling is very sensitive to misalignment, especially to varied separation distances, precise alignment methods are necessary to implement capacitive coupling on a chip scale.

We next propose a method of wireless IC testing via capacitive coupling, which utilizes adjustable transmitter power, pulse position modulation (PPM), and electrical

alignment measurement circuits in an effort to make the wireless I/O link more robust. Due to changing transmitter power, channel gain degradation from misalignment and ESD protection can be compensated for by raising the transmitter power. Then, we can trade off transmitter power for higher ESD protection. The simulated channel gain with ESD protection for the second prototype is −33.6 dB with the identical pad size and 10 μm separation. This is −19.6 dB lower than that of the previous prototype, mainly because of its relatively larger ESD protection circuits. However, the impact of additional power consumption is not significant if we use a wired power connection between the ATE and DUTs.

PPM with return-to-zero (RZ) signaling enables a more flexible data rate and results in received signals free from DC-level fluctuations. With proper termination resistance, the capacitive channel attenuates signal quickly and generates positive/negative pulses depending on rising/falling edges of the input NRZ signals. This technique has been used in capacitive communication due to its lack of DC fluctuation [17][21][31][41][42]. Since the resulting pulses remain the same with different data rates, the receiver can support more flexible data rates.

We also propose electrical alignment measurement circuits that help to achieve proper alignment in the *x*- and *y*-directions, and to correct angular misalignment between the die. They consist of simple positive and negative bar-shaped capacitive sensors. Thank to these new features, we successfully demonstrated chip-level capacitive wireless communication with a data rate of 1 Gbps and BER less than 10^{-11}.

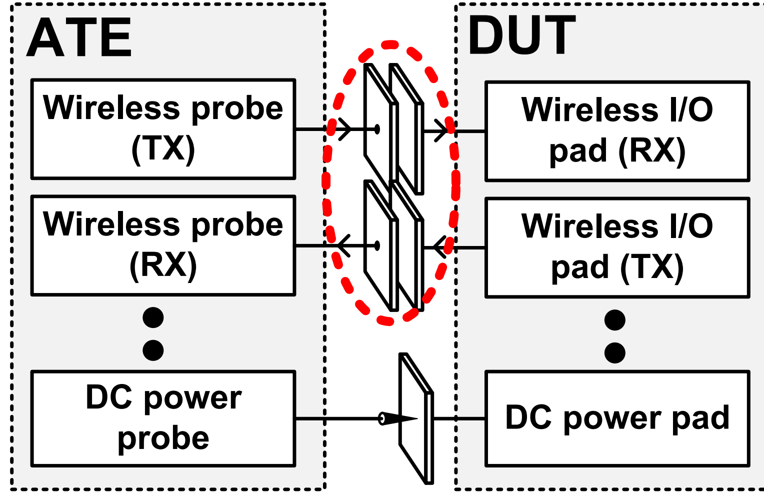


Figure 4.1 Capacitively-coupled wireless testing system.

4.2 Channel Model for RZ Signaling

The proposed system for wireless IC testing is depicted in Figure 4.1. The communication channels between the ATE and DUTs are capacitively coupled through two 117 µm × 65 µm bond pads formed with a top aluminum metal layer. As we have shown in Chapter 2, the capacitive channel can be modeled as follows when the parasitic inductance is sufficiently small.

$$\frac{V_{Rx}}{V_{Tx}} = \frac{C_c}{C_c + C_g} \tag{4.1}$$

Its overall gain is roughly $C_c / (C_c + C_g)$, where C_c is the coupling capacitance and C_g is parasitic capacitance to ground, including ESD loading. EM simulations with HFSS v11 were conducted to extract these values. The simulated channel gain without the termination resistor is about –26.6 dB with a C_c of 7 fF and a C_g of 122 fF. A pad separation of 10 µm is assumed, or about twice the passivation thickness. In this system, the power connection is assumed to be wired.

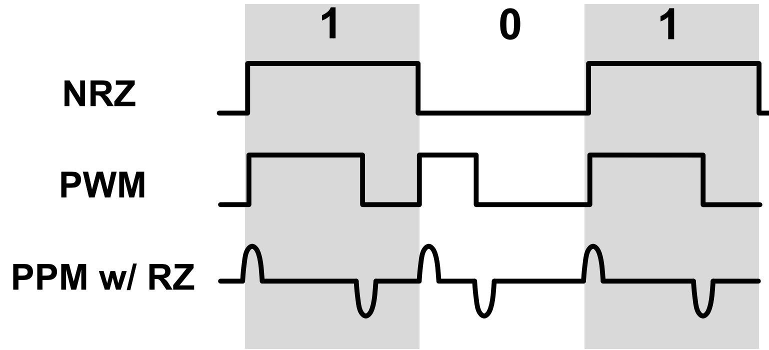


Figure 4.2 PPM with RZ signaling.

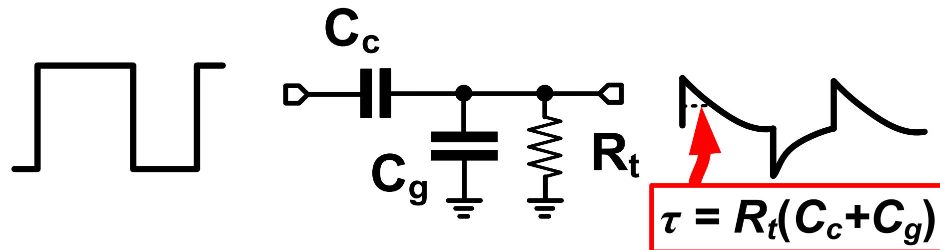


Figure 4.3 Capacitive channel model with the termination resistor R_t.

We use PPM with RZ signaling to embed clock information into the data stream. Positive pulses contain the timing information and negative pulses are used for encoding data. PPM signaling represents the '0' and '1' symbols by the relative locations of positive and negative pulses, as illustrated in Figure 4.2. These PPM signals do not switch in opposite directions at the same time, and thus there is no worst-case Miller coupling. Pulses for PPM can be easily generated with a capacitively-coupled channel terminated with the proper resistance as illustrated in Figure 4.3. The resulting pulses do not suffer from DC-level fluctuation with proper termination resistance R_t.

In Figure 4.4, the channel gain and DC fluctuation factor based on (3.5) are plotted with various R_t values. The region A was used to maintain pulse width information for PWM signals. The received signal swing is also maximized

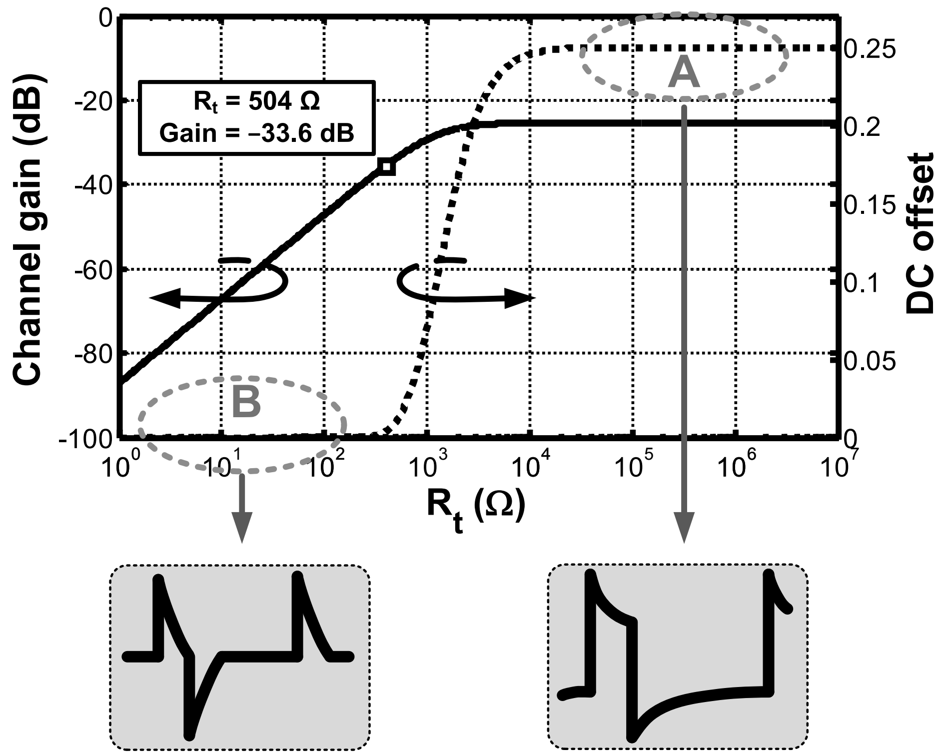


Figure 4.4 Channel gain and DC fluctuation factor with various R_t values at 1 GHz.

with relatively large R_t in the region A. In contrast, we use the region B where the received signals attenuate quickly with a small time constant. In this region, the signals become sharp pulses after passed through the capacitive channel. The signals are highly band-limited in this case, and do not suffer from DC-level fluctuation. An R_t value of 504 ohm is selected, which maximizes the received swings while keeping DC-level fluctuation negligibly small. To generate self-clocked PPM signals, the modulator first converts incoming NRZ data to PWM signals. These are then converted to RZ pulse signals, with termination resistance R_t, at the receiver. By combining PWM and RZ signaling, we can generate self-clocked PPM signals. The overall simulated waveforms are presented in Figure 4.5. Generated PPM RZ signals with termination resistance R_t have an amplitude of 80 mV and pulse width of 130 ps.

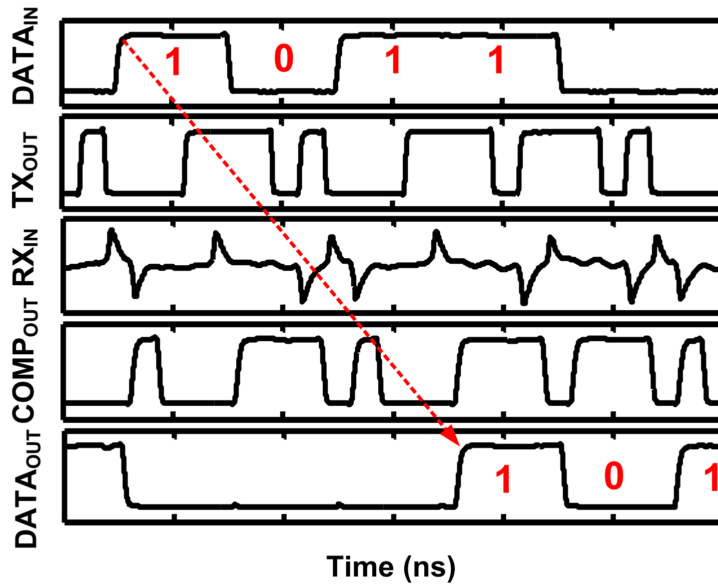


Figure 4.5 Simulated waveforms. PPM signals with RZ signaling are generated from PWM signals with a terminated capacitive channel.

4.3 Overall Architecture

A block diagram of the proposed capacitively-coupled transmitter and receiver is shown in Figure 4.6. The schematic and circuit implementation of the transmitter and receiver are presented.

4.3.1 Transmitter with Adjustable Power

The transmitter uses the same PWM modulator as the previous prototype. The modulator in Figure 4.7(a) consists of a voltage-controlled delay line (VCDL), and an XOR-based edge combiner. The VCDL generates fixed delays t and $2t$ where t is the pulse width for symbol ‘0’. The VCDL has a wider range of t values to support more flexible pulse width in PWM symbols compared to the previous version. Edges are

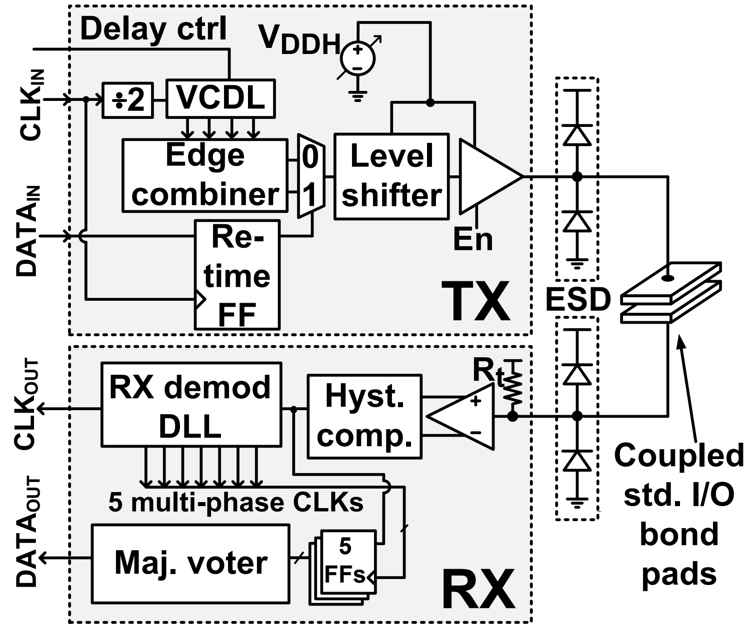
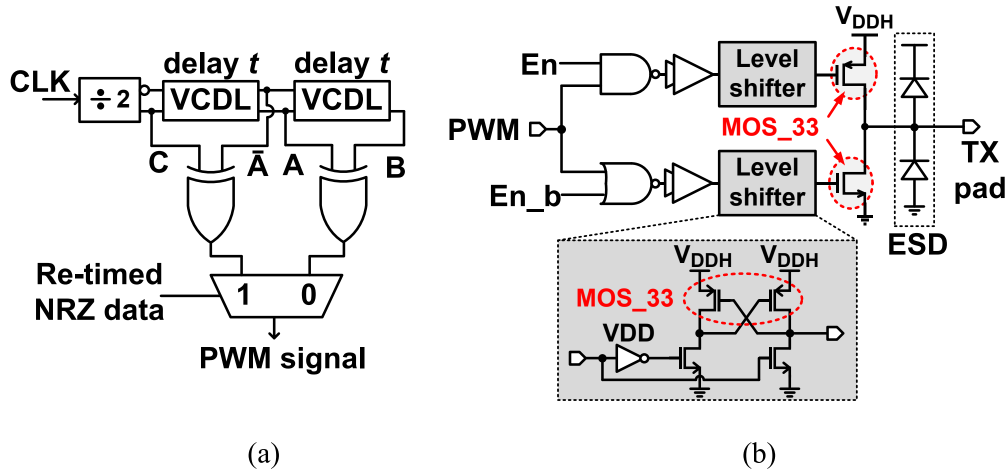


Figure 4.6 Block diagram of TX and RX.



(a) (b)

Figure 4.7 (a) Schematic of the PWM modulator, (b) TX tri-state driver with thick-oxide devices MOS_33.

then selected by the XOR-based edge combiner to form PWM symbols. To support adjustable transmitter power, the PWM outputs are level-shifted to a V_{DDH} voltage tunable from off-chip, which is usually higher than the nominal supply voltage, and then

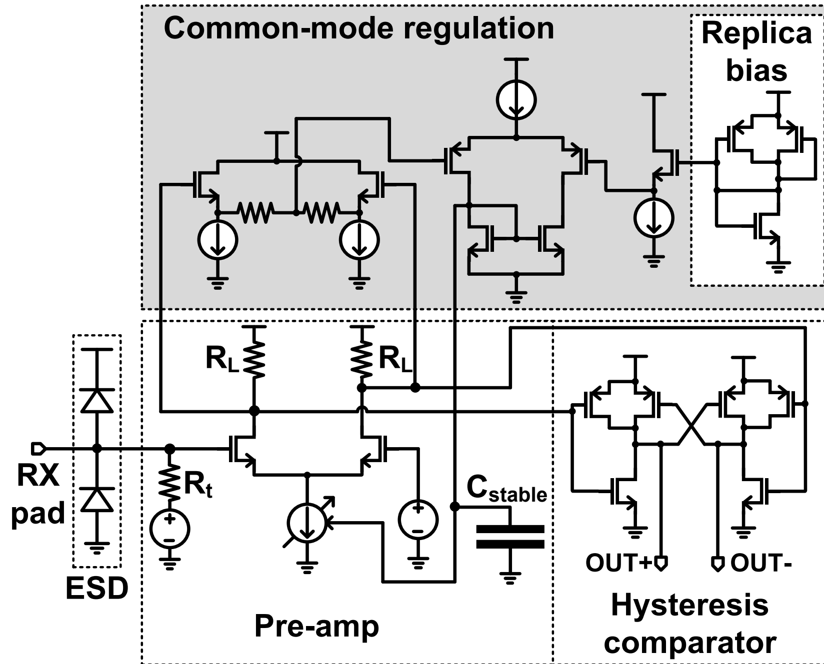


Figure 4.8 Schematic of the RX amplifier with a hysteresis comparator.

driven by a tri-state output driver formed with thick-oxide transistors, as shown in Figure 4.7 (b). The driving strength can be tuned by adjusting V_{DDH}.

4.3.2 Receiver Pre-Amplifier and Hysteresis Comparator

The receiver consists of a pre-amplifier, a hysteresis comparator, and a demodulator with a delay-locked loop (DLL). As noted previously, input to the receiver is terminated with resistance R_t to generate RZ signals by limiting the channel bandwidth, as shown in Figure 4.8. The pre-amplifier converts single-ended inputs to differential outputs. It is a differential common-source amplifier with resistive loads and pseudo differential inputs. One of the inputs is directly connected to the receiver pad and ESD protection circuits, the other is connected to a DC voltage source generated on-chip. Its gain is about 14.2 dB, and its 3-dB cutoff frequency is about 1.43 GHz.

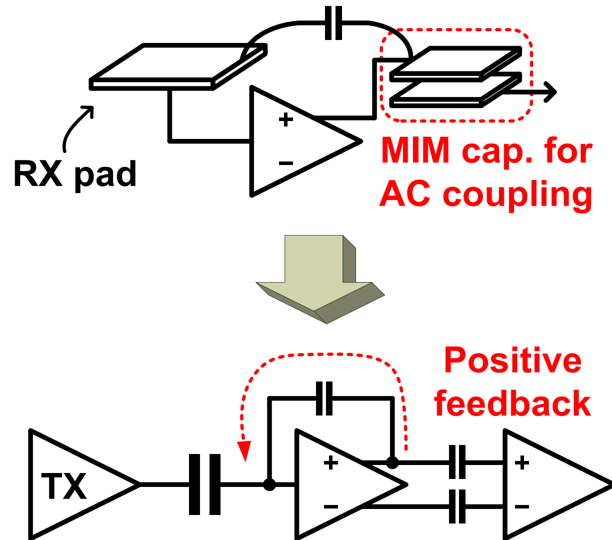


Figure 4.9 Potential positive feedback from unwanted coupling between the RX pad and AC-coupling capacitor.

AC coupling with a capacitor is a widely using technique to interface an amplifier to the following stage. However, this can cause unwanted positive feedback to the receiver pad in capactively-coupled communication. The potential positive feedback is illustrated in Figure 4.9. Here, if the top plate of the AC-coupling capacitor is connected to the non-inverting output, the coupling between receiver pad and the top plate of the capacitor forms a positive feedback loop. If the capacitance in the feedback path is large enough, the entire system becomes unstable. To resolve this, we can place the capacitor away from the input receiver pad to reduce the feedback gain, but this solution is limited by area constraints.

Instead, common-mode regulation with replica bias circuits was used to set the output at the proper DC level for the next stage in Figure 4.8. The common-mode regulation is also beneficial in that it reduces the effect of variations on the resistive load. The DC-level changes with different R_L values without the common-mode regulation.

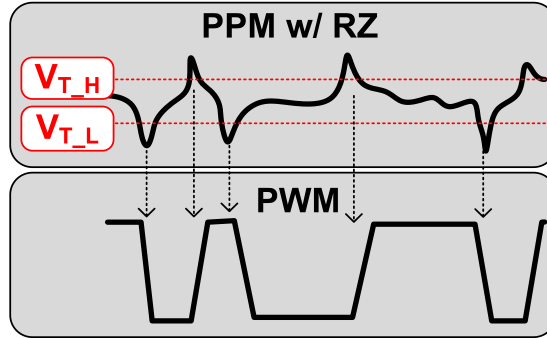


Figure 4.10 PWM signals regenerated from PPM RZ signals with the hysteresis comparator.

However, the proper DC-level of the output is regulated by turning on the feedback circuitry. In this case, the output remains at the same voltage level although the value of load resistance changes. The additional capacitor of 2.4 pF is used to ensure the loop stability.

After converting single-ended signals to differential signals, a hysteresis comparator regenerates PWM signals from PPM RZ signals as shown in Figure 4.10. The hysteresis comparator dynamically changes its threshold voltage between V_{T_H} and V_{T_L} based on the previously received bit. It consists of the amplification transistors and a cross-coupled pMOS pair for latching. The threshold voltage of the comparator is carefully set by sizing the cross-coupled transistors so that it properly detects incoming pulses while rejecting the noise. The input voltage level is set by the replica bias circuits to reduce the impact of process variation. The bias circuits are sized identically to the hysteresis comparator, and the circuit layout is placed very close to the comparator. The overall operation of both the pre-amplifier and the hysteresis comparator is shown in Figure 4.5. The input PPM RZ signals are correctly converted to PWM NRZ signals.

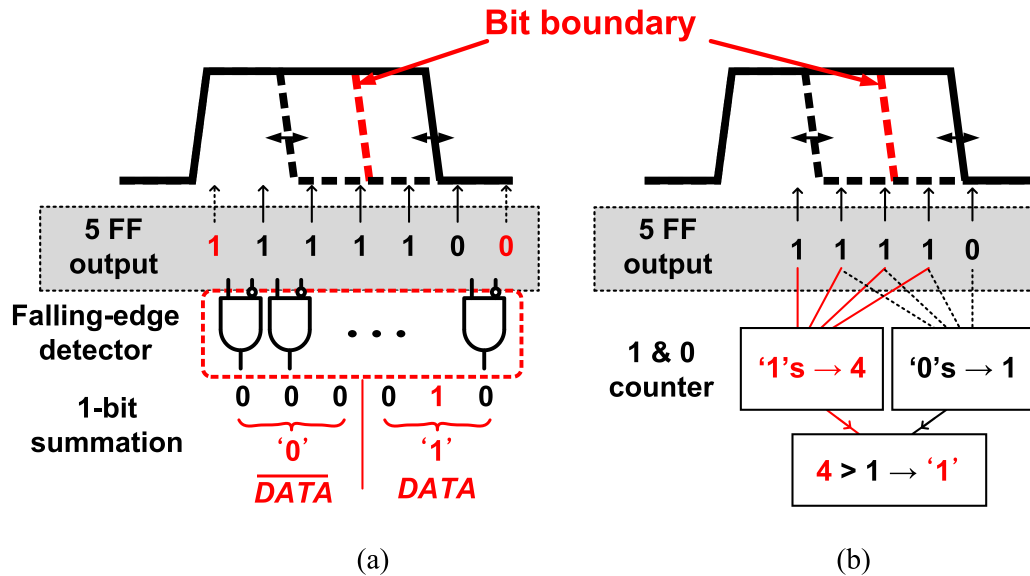


Figure 4.11 Two bit-decision schemes with symbol '1': (a) falling edge detection, and (b) counter-based detector.

4.3.3 Receiver Demodulator

The PWM signals are demodulated with a DLL-based sampler and bit-decision circuits. The DLL consists of a VCDL and a 1-cycle phase detector similar to the previous design described in Chapter 3. After 1-cycle locking, the VCDL generates five different phase clocks. Five positive edge-sensitive flip-flops then over-sample the input PWM signals with these multi-phase clocks. The bit-decision circuits utilize these over-sampled data to decide which symbol is sent. Since PPM RZ signals do not suffer from DC-level fluctuation, the feed-forward clock selector is removed. Instead, two types of bit-decision circuits are designed and evaluated: one is based on falling-edge detection circuits, and the other is a counter-based majority voter. Both the bit-decision makers support flexible data rates and PWM symbols. As illustrated in Figure 4.11, the over-sampled bits are thermometer-coded, which means that there is a run of '1' bits and then a run of '0' follows it. The length of the run of '1' bits represents the pulse width of

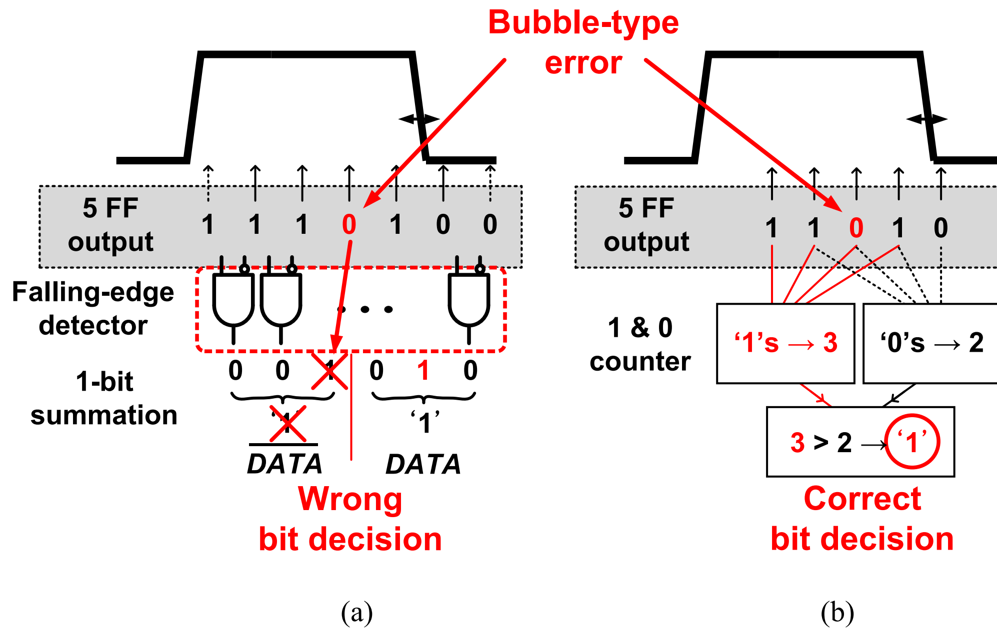


Figure 4.12 Two bit-decision schemes with a bubble-type error: (a) falling edge detection makes wrong bit decision, but (b) counter-based detector suppresses the error.

the signals. The easiest way to demodulate incoming signals is to find where this transition occurs. Two-input AND gates with one inverted input can detect the transition. If it is located in the first half of the bit-decision range, the signal is the '0' symbol. Otherwise it becomes the '1' symbol. This technique is relatively simple and can be implemented with a few digital logic gates. In addition, it can be used with PWM signals having different duty cycles, as long as the pulse width is distinguishable by the minimum quantized step of the over-sampler. PWM signals with a duty cycle lower than 50% can be detected as the '0' symbol; a higher duty cycle means the '1' symbol. Therefore, we can choose any duty-cycle factor of PWM symbols in the transmitter, and the receiver can tolerate high jitter.

However, this technique is prone to bubble-type errors. For example in Figure 4.12, if one flip-flop generates an erroneous output bit, the falling edge detection cannot make a proper bit-decision. To suppress bubble errors, counter-based bit-decision circuits

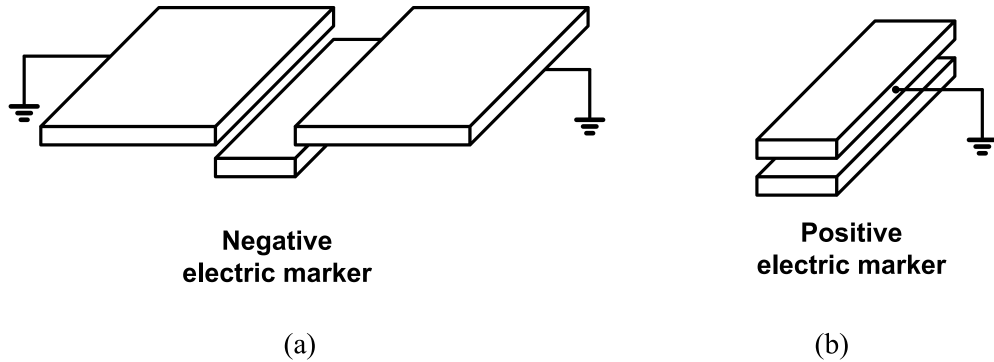


Figure 4.13 Two types of electrical alignment markers: (a) negative marker, and (b) positive marker.

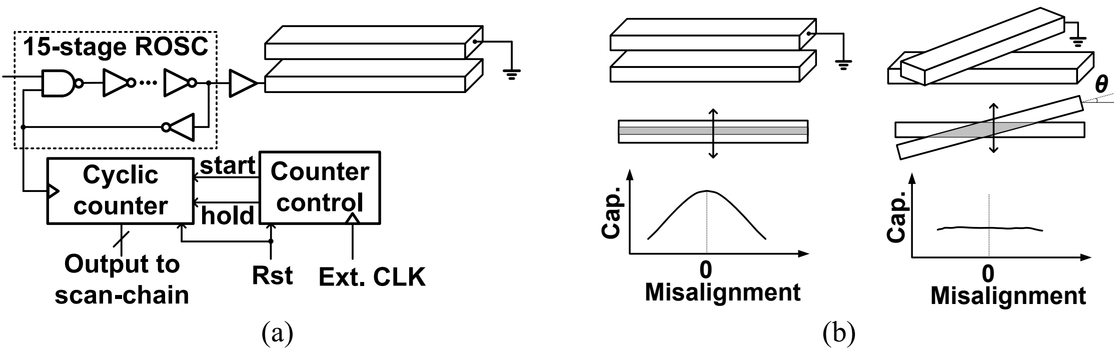


Figure 4.14 (a) Schematic of capacitance measurement circuits, and (b) alignment mechanism.

are also implemented. These circuits count the numbers of ‘0’ and ‘1’ bits among the resulting over-sampled outputs. If there are more ‘1’ bits than ‘0’, the PWM signal represents the ‘1’ symbol. In other cases, the bit decision is ‘0’. Since the counter sums the over-sampled data bits, a bubble-type error is successfully corrected. The counter-based bit decision supports flexible duty cycles for the PWM signals as well. A simple illustration for the bit-decision operation is given in Figure 4.12.

The jitter noise, which is usually caused by noise coupled through supply connections, can be successfully suppressed with both demodulators. A bubble-type error usually occurs when one of the over-sampling flip-flops malfunctions due to

metastability, cross-talk, or soft error. It can be only corrected with the counter-based majority voter.

4.4 Electrical Alignment Markers

For die-level evaluation of the prototype test chips, the electrical alignment markers shown in Figure 4.13 are used. We expect that at the wafer-level in an ATE environment, alignment markers will not be required. Together the two markers cover *x*- and *y*-axis misalignment. The *x*-axis marker is a negative marker consisting of a long plate on the ATE side, and a vacant area surrounded by ground plates on the DUT side. The *y*-axis marker comprises two identical long metal plates on both ATE and DUT sides. We designed different types of markers in order to compare their performance. For both markers, a large ground plate is required, which provides good current return paths for accurate capacitance measurements.

Alignment is measured using the capacitance measurement circuits in Figure 4.14(a) consisting of a 15-stage ring oscillator, a 10-bit cyclic counter, and a controller. The counter measures frequency by counting positive edges of the ring oscillator over a fixed period of time. Its frequency depends on the RC time constant of the output node connected to the markers, so frequency is directly proportional to the markers' coupling capacitance, which can be maximized or minimized, accordingly. We can achieve very high resolution of the measured capacitance by increasing the counting period [39]. The resulting 10-bit output values are read off-chip through the scan-chain, and represent a relative change in capacitance.

Table 4.1 Simulated coupling capacitance and oscillation frequency

	Marker type	Coupling cap.	Frequency
x-direction marker	Negative	4.7 fF	747 MHz
y-direction marker	Positive	10.4 fF	731 MHz

.

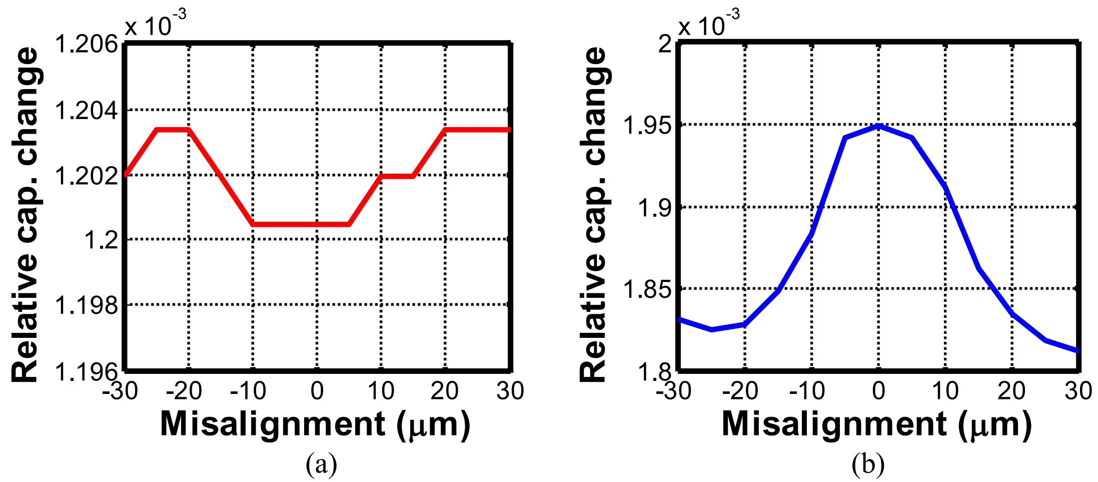


Figure 4.15 Measured relative capacitance change without rotation misalignment from (a) negative *x*-marker, and (b) positive *y*-marker.

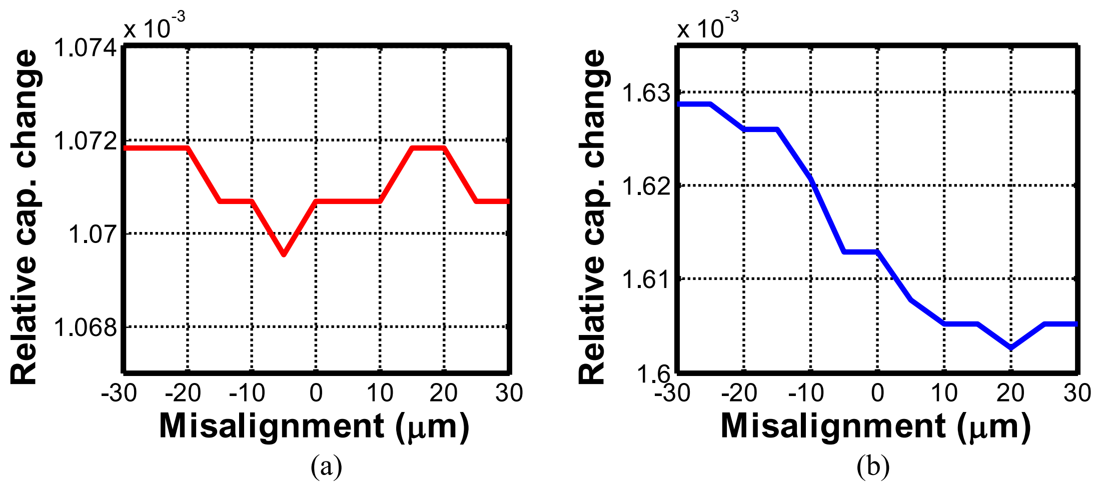


Figure 4.16 Measured relative capacitance change with rotation misalignment from (a) negative *x*-marker, and (b) positive *y*-marker.

Proper alignment can be achieved by measuring the relative coupling capacitance with varying misalignment. If we vary the alignment in the *x*-direction, the coupling

capacitance of the overlap of *x*-marker is minimized when the marker is perfectly aligned. Similarly, for *y*-direction alignment, the coupling capacitance is maximized with proper alignment. The measured relative capacitance values with misalignments are illustrated in Figure 4.14(b). They are both symmetric and centered around the zero-misalignment point. The *x*-marker is 20 µm × 115 µm, and the y-marker is 20 µm × 345 µm. Since the negative *x*-marker is shorter in length than the positive *y*-marker, the change in relative capacitance is also smaller with the fixed counting period 4.8 µs, which was selected with HFSS EM simulations. The simulated frequency of the ring oscillator and coupling capacitance values for perfect alignment are shown in Table 4.1. The simulated frequencies of the ring oscillators are not identical since their coupling capacitance values are slightly different when perfectly aligned.

The capacitance measurement data with two face-to-face stacked chips are plotted in Figures 4.15 and 4.16. Although the counting period is increased to 7.2 µs for the *x*-marker, there is no significant improvement in resolution of relative capacitance. This is mainly due to smaller coupling capacitance than the *y*-marker and more fringing capacitance from the complex structure of the negative marker. These markers also allow rotation misalignment to be measured. As we expected, their overlap becomes less alignment-dependent due to their long shape when rotated. The capacitance change is flatter in this case than that with proper alignment. The *y*-marker was used to measure the rotation because of its higher resolution. In Figure 4.16, the relative capacitance values with rotation are present. A proper rotation alignment can be achieved by finding the sharpest peak at zero-misalignment with *y*-marker. Since the *x*-marker has low resolution, the *x*-marker is used for coarse alignment, and then fine alignment in the *x*-direction was

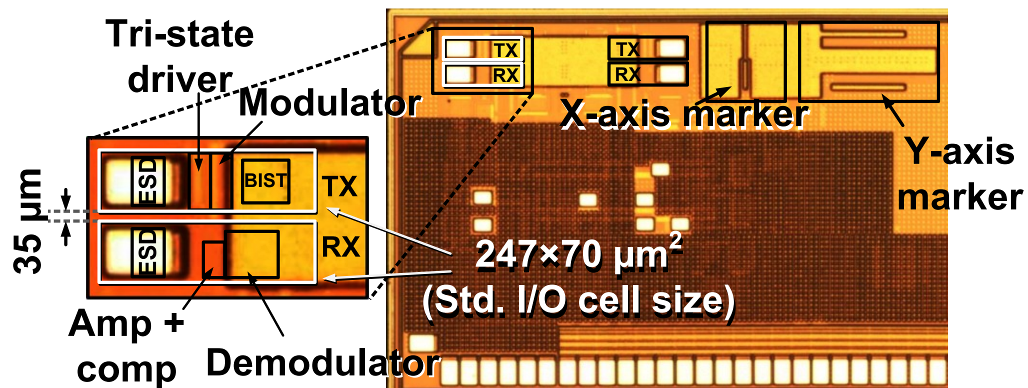


Figure 4.17 Die photomicrograph of the prototype chip.

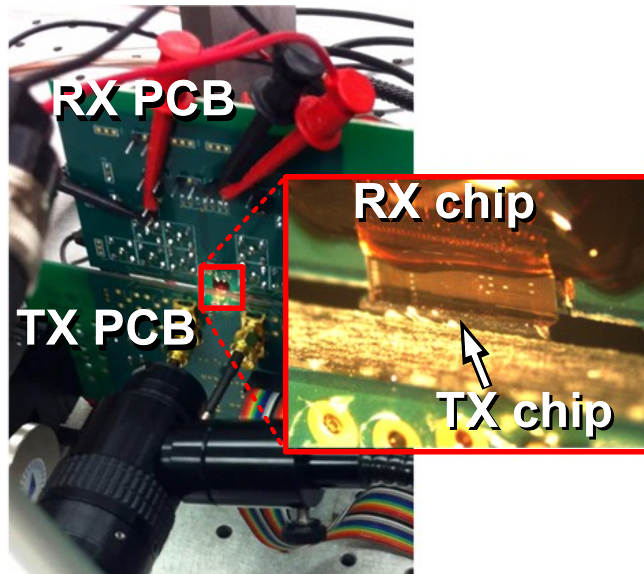


Figure 4.18 Test setup with a micro-manipulator.

mainly performed with a microscope by observing and adjusting two side edges of the chip.

4.5 Communication Link Measurement Results

A prototype chip was fabricated in 0.13 μm CMOS. Its die photo is shown in Figure 4.17. The chip was tested using a PCB mounted with a micro manipulator that

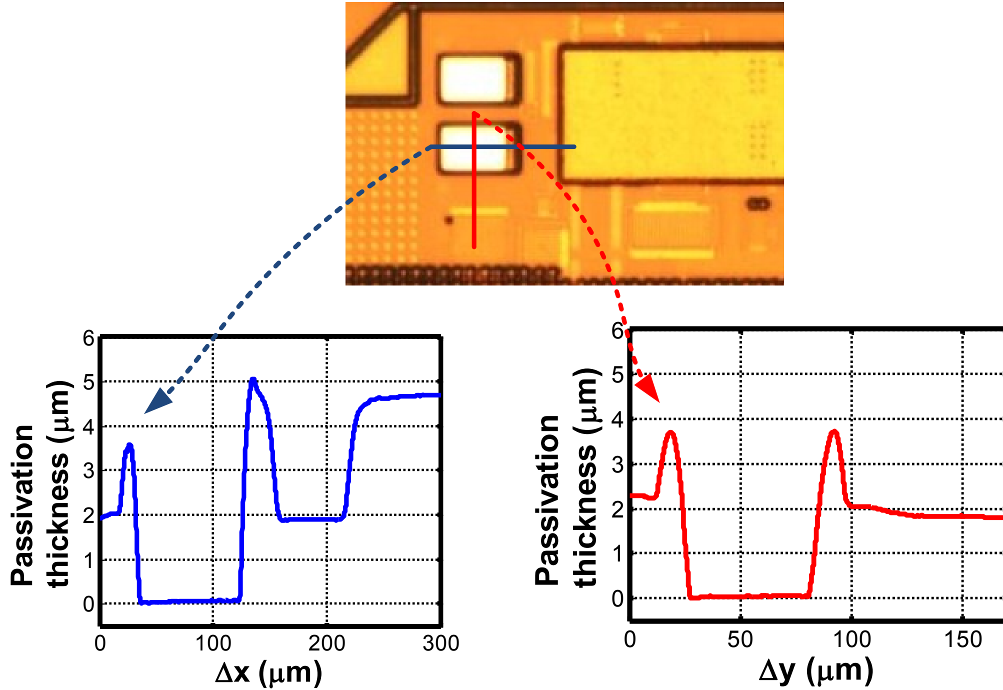


Figure 4.19 Test chip surface profile measured by a Dektak 6M surface profiler.

supports 3D positioning with sub-micron precision, as shown in Figure 4.18. Since the channel gain is very sensitive to the chip separation, the passivation thickness of the prototype was measured using Veeco's Dektak 6M surface profiler. The surface profile near the wireless pads is measured and plotted in Figure 4.19. The surface profile looks quiet uniform, but the maximum thickness is measured as 5 μm which is slightly higher than the nominal 4 μm thickness of this process. Although the 5 μm thickness is only for a small and limited area, we assume the chip separation as 10 μm, which is twice of the thickness with sufficient margins.

The prototype supports two different modulation methods, NRZ and PPM. They can be selected using a multiplexer in the modulator circuitry. A $(2^{15} - 1)$-bit PRBS generated on-chip provides input test patterns to the transmitter. The response of the receiver was measured by a Tektronix GB 1400 BER tester. For the NRZ mode, the

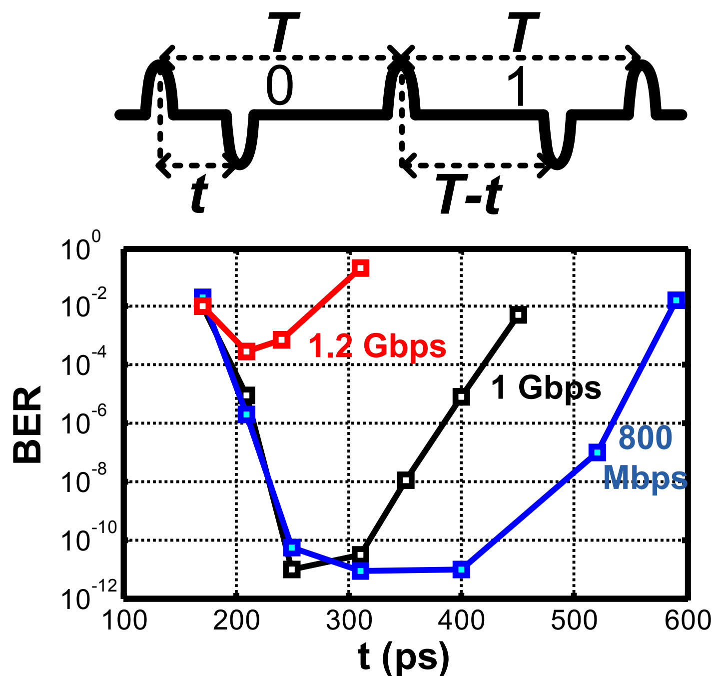


Figure 4.20 Measured BER vs. minimum pulse distance *t* (*T* = 1ns).

prototype achieves BER less than 10^{-12} with a 1.4-Gbps data rate and a V_{DDH} of 2.7 V in the transmitter. However, the 1.4-Gbps data rate is limited by the GB1400 BER tester which supports only up to 1.4-Gbps data rate. Based on the measured minimum pulse distance of PPM in Figure 4.20, we can estimate that the actual maximum data rate is up to 4 Gbps. With PPM, the measured BER was less than 10^{-11} with a 1-Gbps data rate using the same V_{DDH}. We transmit both clock and data signals at the same time by sacrificing the data rate. This is advantageous since it does not require an additional clock channel. The BER of less than 10^{-11} was achieved with the counter-based bit decision. The BER values with falling-edge detection falls below 10^{-9} due to bubble-type errors. The rest of the BER measurement was conducted with the counter-based bit-decision. The measured BER versus minimum pulse distance *t* for PPM is shown in Figure

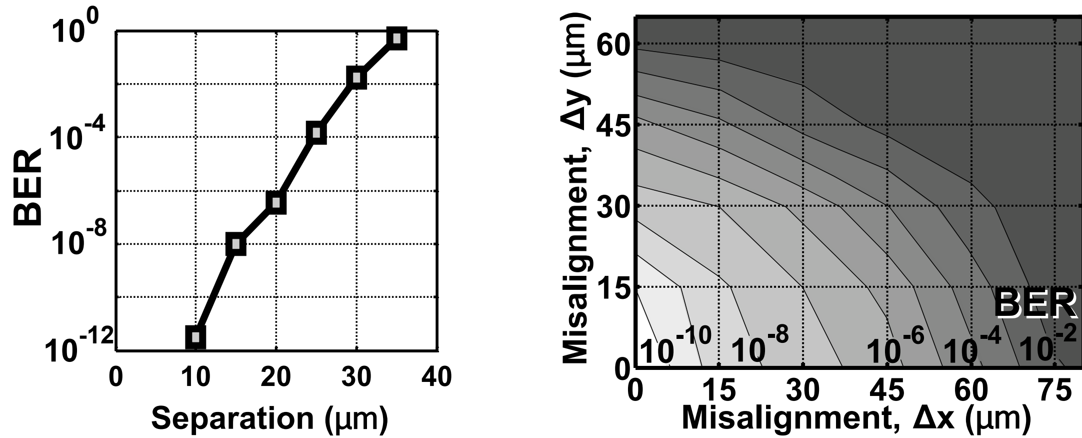


Figure 4.21 Measured BER vs. (a) pad separation, and (b) *x*- and *y*-misalignment.

4.20. Here, t is identical to the pulse width in PWM. The left side of the bathtub curve represents the performance limitation by the pre-amplifier and hysteresis comparator while reconstructing PWM signals from PPM. If t is less than 250 ps, the positive and negative pulses are too close to each other, and reduce the effective amplitude. Then, such small pulses cannot be regenerated by the hysteresis comparator. The right side of the bathtub curve shows the BER performance limited by the DLL-based demodulator. If t comes close to a half of the symbol duration T, reconstructed PWM signals cannot be distinguishable. As we expected, the counting bit-decision circuits successfully support flexible duty-cycle factors. In contrast to our previous work, t can vary from 250 ps to 310 ps when the data rate is 1 Gbps, and is usually fixed at 250 ps with feed-forward clock selection. We can select wider range of t if a lower data rate is used.

BER values corresponding to different separation and misalignment values appear in Figure 4.21. BER performance is more sensitive to the chip separation. Misalignment in the *x*- and *y*- directions affects the BER performance as well, but not as significantly as the chip separation. The cross-talk effect is also measured by turning on the adjacent transmitter site. It was found to have an imperceptible impact on the BER.

Table 4.2 Performance summary of the 2nd prototype chip.

Technology	0.13 μm CMOS	
Area	Transmitter	3307 μm^2
	Receiver	7315 μm^2
Power dissipation (1 Gbps @ 1.3V)	Transmitter	4.1 mW
	Receiver	6.3 mW
Maximum data rate	PPM with RZ	1 Gbps
	NRZ	1.4 Gbps *
Channel gain	−33.6 dB	
BER	0.3×10^{-11}	

* This is limited by the performance of the measuring equipment.

Both the transmitter and receiver have less area than a standard 247 μm × 70 μm I/O pad, including ESD protection circuits and standard digital I/O buffers intended for use as I/O pads after testing. Key performance details are given in Table 4.2.

4.6 Summary

We have demonstrated a prototype IC for wireless testing that successfully employs capacitive non-contact I/Os, and PPM with RZ signaling for clock embedding. The performance of NRZ and PPM was compared, and the two different bit-decision methods were evaluated. The counter-based bit-decision shows better BER performance than the falling-edge detection method. The fabricated prototype supports a flexible minimum-pulse distance and adjustable transmitter power. The chip surface is sufficiently uniform and maximum passivation thickness is 5 μm. Due to fringing capacitance, the proposed capacitive links show good tolerance of *x*- and *y*-misalignment. The prototype chip demonstrates up to 1 Gbps self-clocked communication with BER less than 10^{-11}.

Chapter V

On-Chip Wireless Voltage Measurement

In the previous two chapters, we mainly focused on wireless testing of digital ICs, which requires delivering digital signals between the ATE and the DUTs. This chapter looks into several wireless methods for testing analog ICs and process characterization. Voltage measurement results from the prototype chip with both wired and wireless setups are compared and discussed.

5.1 Introduction

Generally speaking, testing of analog ICs is more complicated than that of digital ICs. Since most I/O data are digital, only digital data communication links are needed for IC testing when wired power connections are present. However, many different parameters need to be collected for analog testing, including voltage, current, timing, and frequency information. In general, complex and power-consuming interfaces are required to collect such analog outputs without significant distortion. Analog and mixed-signal testing with on-chip test interfaces has been an active research area for many years [60][64][65][82]. This research mainly focuses on how to input signals to DUTs and how to collect the corresponding output signals using on-chip circuitry. In most cases, the circuits for analog testing convert the original signals to certain forms which are more

easily collected and compared at the ATE. For example, in [64] analog output signals are digitized to improve compatibility with conventional ATE. The converted signals usually differ from the original signals, and require additional signal processing to remove discrepancies such as quantization noise or harmonic distortion. It is critical to minimize such discrepancies if accurate analog IC testing is desired. Process characterization is another form of analog testing. Measurement of data from sacrificial test circuits, so-called "process characterization", is necessary to predict the functionality and performance of an IC [4]. Various analog parameters which can be expressed in terms of current or voltage change are required to measure process variation, including leakage current and process mismatch. These are similar to what needs to be measured in analog IC testing.

Process characterization is an important way to reduce manufacturing cost by the prediction of yield. Due to limited accessibility from off-chip test equipment to the DUT, on-chip circuits are widely used for characterization, and can achieve measurement resolution comparable to off-chip equipment [13][28][29][32]. However, the accessibility of on-chip characterization circuits is still limited since measured parameters must be digitized, or extra probe pads must be added for analog measurements. In both cases, the area overhead due to additional analog-to-digital conversion circuits (ADCs) and probe pads is substantial. Also, on-chip characterization circuits need to be spread over the entire die or wafer to estimate site-to-site or wafer-to-wafer variation [57].

We propose two methods for wireless analog testing which can be used for both analog IC testing and process characterization. They replace probes with wireless circuits and channels, and therefore mitigate the effect of physically-contacting probe tips. In

addition, wireless communication can greatly improve the accessibility of the testing and on-chip characterization circuits if it supports a wide communication range. If this range is sufficiently broad, the added circuits can also be used after packaging. For deep sub-micron technology, there has been a strong demand for on-line test and measurement circuits to detect aging effects and gate leakage current, not only at the fabrication stage, but also over a chip's entire lifetime [13][29].

On-chip wireless analog testing and on-chip characterization circuits not only improve accessibility, they also can provide significantly smaller area using off-chip equipment with high accuracy. It is also expected that measurement accuracy can be improved with wireless communication due to the off-chip measuring equipment. As discussed above, most on-chip characterization circuits include analog-to-digital conversion of the data being measured. Generally more area is required to achieve higher ADC resolution, but the area of on-chip characterization circuits is usually limited. For example, in [13] a 13-bit ADC is used to extract the I-V characteristics of FETs in a DUT, but the ADC is too large to be placed in each individual characterization circuit. As a result, one high-resolution ADC is shared by every characterization circuit. Sharing one ADC may affect the accuracy because complex interconnections and switches are required. However, with wireless testing techniques, the ADC can be removed from the DUTs and placed on the tester. Since accuracy and post-processing power on the tester side can be a lot better than that on-chip, it is expected that the area of test circuits on the DUTs can be significantly reduced while improving measurement accuracy as long as the distortion from wireless channels can be compensated for.

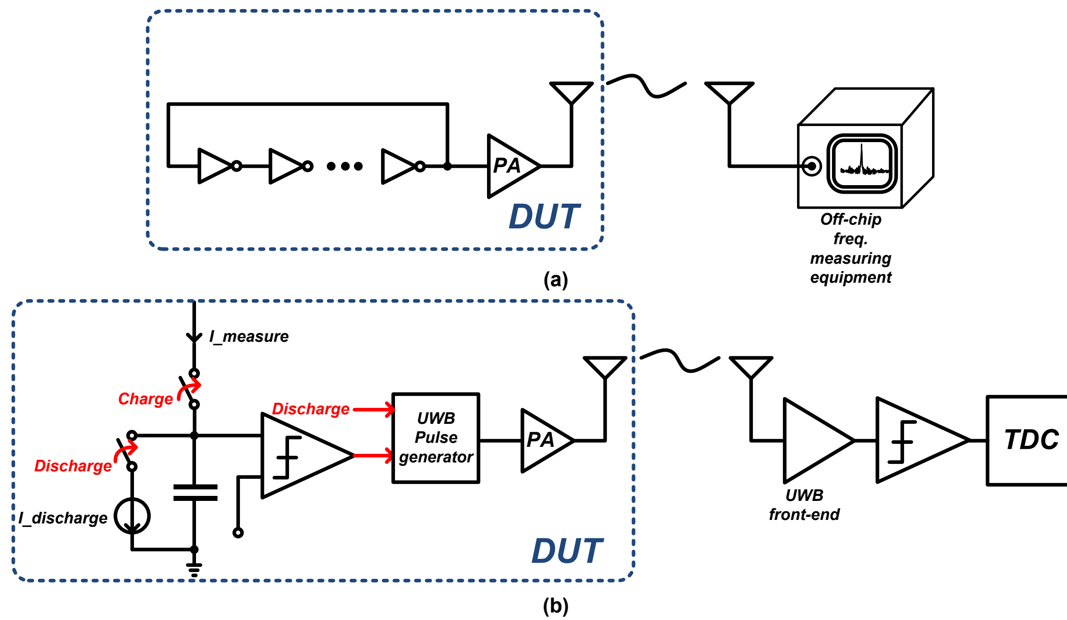


Figure 5.1 Possible implementations of analog IC testing.

Two possible implementations of a wireless analog IC tester and characterization circuit are shown in Figure 5.1. An inverter-based ring oscillator is widely used for on-chip characterization. Any process variation is reflected as a change in threshold voltage, which is strongly correlated to the frequency of oscillation of a ring oscillator. A digital counter or time-to-digital conversion (TDC) circuit is conventionally used for frequency digitization. In Figure 5.1(a), a ring oscillator is connected to an antenna of sufficient driving strength, and then off-chip ADC or frequency-measuring equipment is used to measure the frequency of the ring oscillator. Because most off-chip measuring equipment provides much higher accuracy than on-chip circuitry, we can expect better measurements from it. Another possible implementation of wireless current measuring circuits is depicted in Figure 5.1(b). Slope ADC current measurement circuits for device characterization can be assisted by an ultra-wide band (UWB) pulse generator and

receiver combined with a TDC. By moving the complexity of the TDC from the DUT to the tester, we can minimize area consumption and achieve high accuracy.

We present a prototype wireless voltage measurement circuit which consists of a dual-slope integrator and an UWB pulse generator in Figure 5.1(b). It utilizes a capacitively-coupled channel between on-chip pads and RF probe tips. The high-speed oscilloscope is used as a tester instead of the TDC to check the feasibility of the proposed architecture. The prototype successfully conveys voltage information through the capacitive channel. The impact of the wireless channel on the performance of the prototype and the feasibility of wireless analog testing will be discussed later.

5.2 Integrating ADC

An integrating ADC circuit converts analog input voltage to a digital code by measuring the time to charge or discharge an capacitor up to a certain voltage level V_{ref}. A schematic of a single-slope ADC is shown in Figure 5.2, which is the simplest integrating ADC. It accumulates charges to an integrating capacitor with a slope of $-V_{in} / RC$. The slope is proportional to the input voltage V_{in}, and thus the charging time represents the input voltage value. A TDC is usually used to convert time information to a digital code. Assuming an ideal and linear integrator, the minimum time unit T_b that can be resolved represents one bit of information. This is related to a minimum voltage unit V_b as follows.

$$(V_b \times T_b) \propto R \cdot C \tag{5.1}$$

Based on (5.1), we can see that the TDC's minimum resolution is related to the R and C values of the integrator for fixed ADC resolution. In most cases, relatively large R

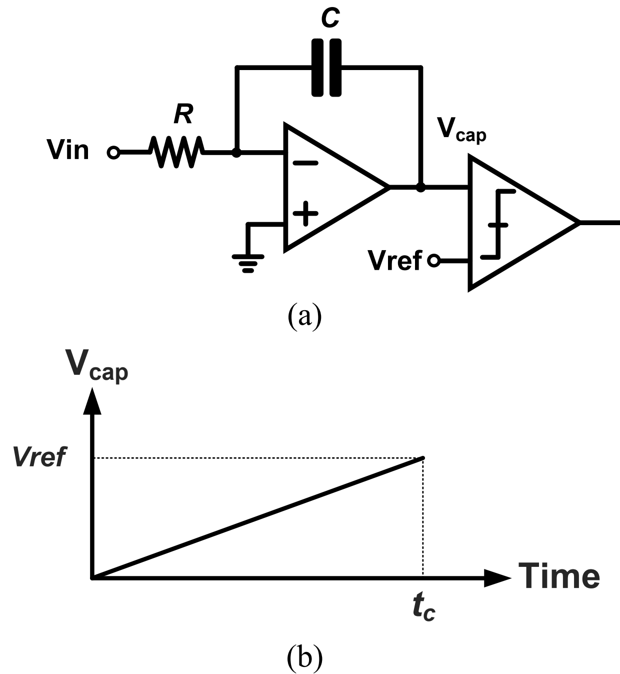


Figure 5.2 (a) Schematic of a single-slope ADC, and (b) its timing diagram.

and *C* values can be selected to produce a TDC with decent performance. In other words, there exists a trade-off between the size of *R* and *C* and the accuracy of the TDC. Since the size of on-chip *R* and *C* is usually limited, resolution of the TDC needs to be sufficiently high. The major drawback of the single-slope ADC is that the measured time information depends on the *R* and *C* values in the integrator. On-chip *R* and *C* may suffer from process variations. To avoid this dependency, a dual-slope architecture is widely used.

A dual-slope ADC integrates input voltage over a fixed amount of time. Then, it discharges the capacitor with a fixed rate and measures the time until the output voltage becomes AC ground. Since the ratio of the time for charge and discharge is independent on the *R* and *C* values for the integrator, V_{in} and V_{ref} are linear and independent of *R* and *C* as long as they are time-invariant.

$$V_{in} \times t_{charge} = -V_{ref} \times t_{discharge} \qquad (5.2)$$

where t_{charge} is charging time and $t_{discharge}$ is discharging time. The equation (5.2) depicts the relationship between V_{in} and V_{ref}. Although the dual-slope ADC is independent on *R* and *C* values, there still exist the same trade-offs between *R* and *C* and TDC resolution.

5.3 Wireless Voltage Measurement Architecture

We implemented the wireless voltage measurement circuits in Figure 5.1(b) based on the dual-slope ADC architecture. As mentioned, it is robust over wide variations of *R* and *C* values. The goal is to replace the TDC with a wireless transmitter and test equipment. If we assume timing measuring equipment has high accuracy, the performance limitations of the TDC can be traded for the distortion and non-linearity of the wireless transmitter and channels. In addition, the *R* and *C* values of the integrator can be chosen to be relatively small if we use off-chip timing measuring equipment with high resolution.

A UWB transmitter is used to convey timing information wirelessly. Since it generates very sharp pulses, timing information can be easily transmitted. In addition, it has low power consumption because it can be designed with static CMOS circuits. The most power consumption occurs when it generates UWB pulses.

There are many sources of non-linearity and distortion in the proposed architecture even though we assume an ideal off-chip TDC. For example, the integrator may suffer from non-linearity if its gain is insufficient. Also, clock feed-through and

charge injection can affect the voltage output of the integrator when we switch the input voltage from V_{in} to V_{ref}. Careful design is required to minimize these non-linearity effects.

For the prototype design, we focus more on the distortion and non-linearity added by the UWB pulse generator and wireless channels, not the non-ideality of the integrator and comparator. Therefore, the integrator is made of a simple one-stage operational amplifier with a low unity gain frequency and decent gain. The input voltage is assumed to have very low frequency as well. The prototype supports both wired and wireless pulse generators with output pads. The performance difference between wired and wireless setups is measured and compared to evaluate the impact of the added wireless communication.

5.4 Prototype Implementation

The schematic of the prototype is shown in Figure 5.3. It consists of an integrator, a continuous comparator, a UWB pulse generator, and a digital controller. An on-chip resistor of 60 kΩ and capacitor of 5 pF are used in the integrator. V_{ref} is set to 400 mV based on the input range needed by the operational amplifier in the integrator. The integrator covers the input voltages from 600 mV to 855 mV. It discharges the capacitor first, and then charges until the output becomes the AC-ground voltage 600 mV. Discharge time t_{dis} is defined by an off-chip clock frequency applied to the digital controller. With a 30 MHz clock frequency, t_{dis} is set to 0.04 μs.

A static comparator in Figure 5.4 detects zero-crossing points and generates digital output. Since the output voltage slope is fixed at constant V_{ref}, the input to the comparator is always the same. However, the output of the comparators can also contribute to the non-linearity by adding a time-varying latency to the output signals. An

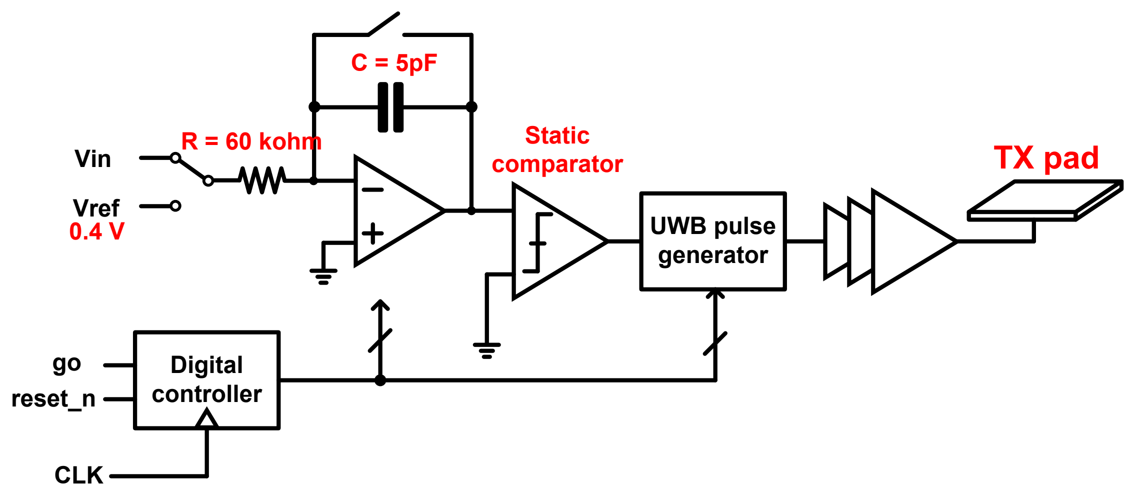


Figure 5.3 Schematic of the prototype voltage measurement circuits.

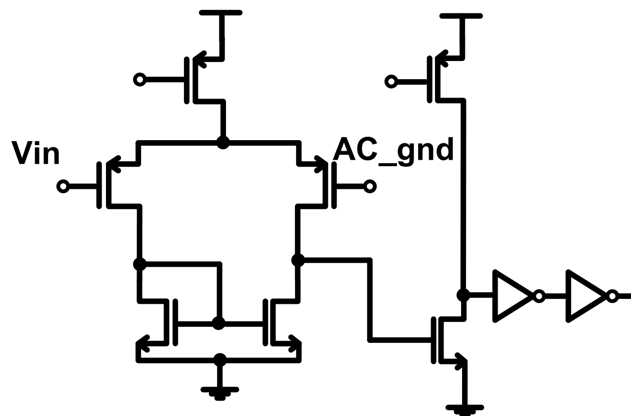


Figure 5.4 Schematic of the static comparator.

additional digital buffer stage is placed after the comparator to ensure a full-swing digital output.

The UWB pulse generator is based on a pulse generator with an NAND gate and a delayed input as shown in Figure 5.5. We are interested in the timing information during the discharge phase. A UWB pulse is generated when charge starts (*start* in Figure 5.6) and when the output of the integrator crosses AC ground (*done* in Figure 5.6). First, these

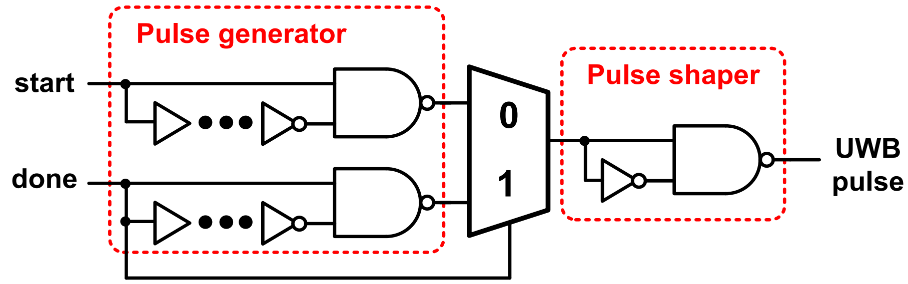


Figure 5.5 Schematic of UWB pulse generator.

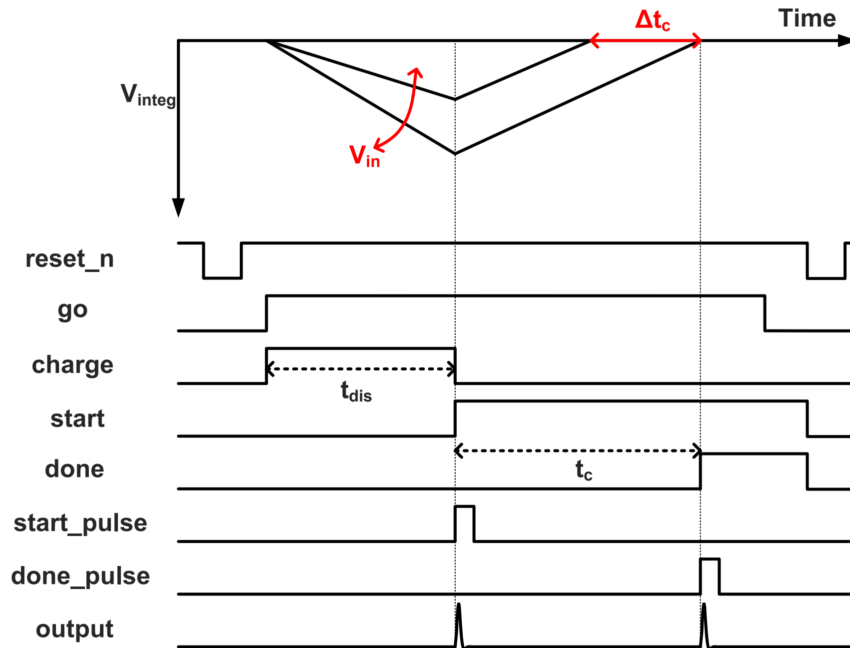


Figure 5.6 Timing diagram of the prototype architecture.

signals *start* and *done* are converted to pulses of relatively long width. Then, the *done* signal selects a multiplexer output between those two pulses. In order not to corrupt timing information from the *done* signal, the control signal to the multiplexer needs to arrive earlier than *done_pulse*. Simulations with process, supply voltage, and temperature variations were conducted to ensure this. To minimize discrepancy between two pulses corresponding to *start* and *done* signals, they must be generated by a single pulse generator. The UWB pulse shaper makes these pulses more sharp with the narrow pulse

widths after the multiplexer. The multi-stage digital buffers drive the output pads. Since the UWB pulse is generated from digital CMOS circuits, its amplitude and pulse width are prone to supply voltage and process variations as well. However, the effect of process variation cannot have significant impact on the time information since the same UWB pulse generator is used. Also, supply noise can be mitigated by averaging the measured data over multiple measurements.

The digital controller utilizes an off-chip clock so that the charging time can be adjusted. It generates proper control signals for the various switches in the integrator. The overall timing diagram of the proposed architecture is presented in Figure 5.6. Voltage measurement is performed when the off-chip *go* signal is asserted after reset. By measuring the time interval between two pulses, the ratio of V_{in} to V_{ref} can be calculated with (5.2).

5.5 Prototype Measurement Results

A prototype chip containing the foregoing wireless voltage measurement circuits was fabricated in a 0.13 μm CMOS process. The chip photomicrograph is shown in Figure 5.7. A resistor and capacitor for the integrator are implemented on-chip with a poly resistor and a MIM capacitor. Input voltage V_{in} and reference voltage V_{ref} are given off-chip, and a clock is required for the digital controller to generate switch control signals. The controller is made from a digital standard cell library. We expect that for the complete wireless analog testing system V_{ref} will be generated on-chip, and a clock and control signals will be sent wirelessly from the ATE. The output of the pulse generator is connected to a digital driver which drives wireless probe pads. Ground-signal-ground

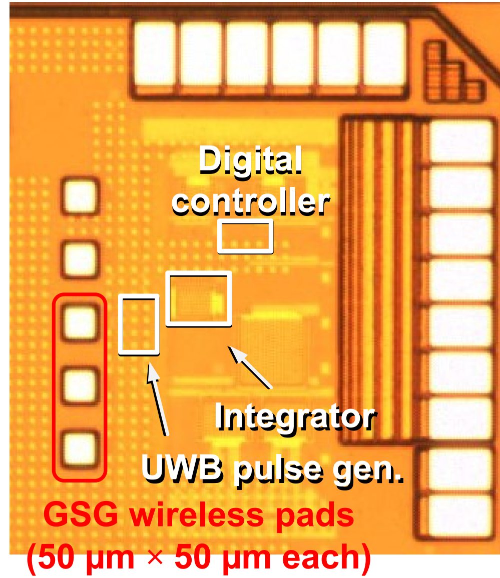


Figure 5.7 Die photomicrograph of the prototype.

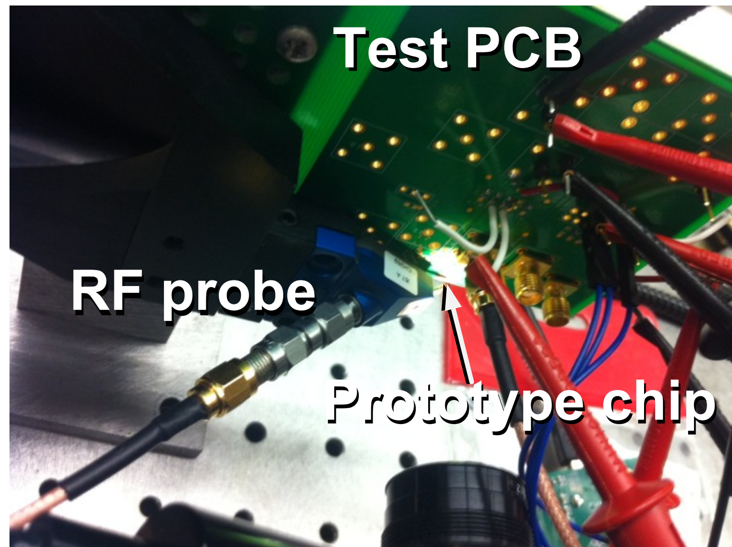
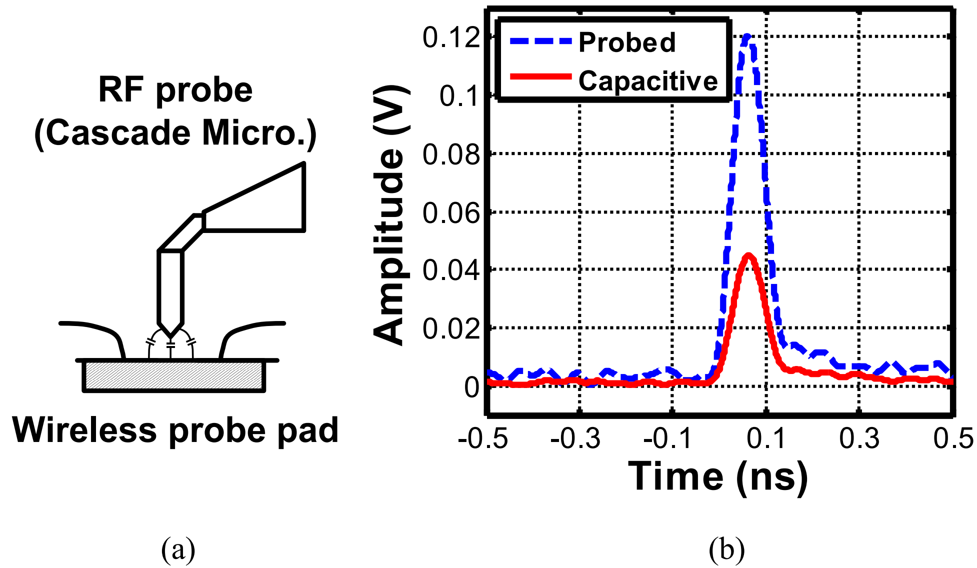


Figure 5.8 Test setup.

(GSG) probe pads of size 50 µm × 50 µm are placed to form capacitive coupling to the RF probe tips. The overall active area of the prototype is 13089 µm^2, excluding pads. The prototype consumes 3.5 mW with supply voltage of 1.2 V. The test setup is shown in Figure 5.8.



(a) (b)

Figure 5.9 (a) Capacitive coupling between a wireless probe pad and an RF probe, and (b) measured UWB pulses.

For a wired test setup, the output pads are probed by a GSG-type RF probe, from Cascade Microtech, and directly to a high-speed Tektronix TDS6124C oscilloscope which supports a 12-GHz bandwidth and a 40GS/s sampling rate. The oscilloscope can detect 19 ps rise time. Based on initial measurement, we assume that the prototype supports 8-bit resolution. To check the output linearity, input voltage V_{in} is varied from 600 mV to 855 mV with 1 mV steps. This step size is enough so that the performance measurement is not limited by the resolution of the oscilloscope, which supports 0.5 ps timing resolution.

For the wireless test setup, capacitive coupling is used between the RF GSG probe and probe pads on-chip. The probe tip is lightly touched down to the pads, and then is lifted up by about 3 μm by a probe positioner, as illustrated in Figure 5.9(a). A laterally-mounted microscope is used to make sure that the probe tip does not touch the pads. The UWB pulse amplitude is measured with the wired and wireless setup in Figure 5.9(b).

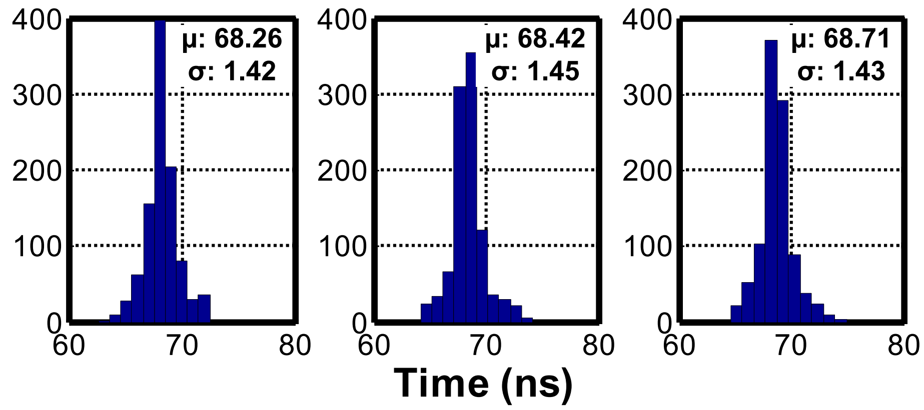


Figure 5.10 Histograms of three different wireless measurements with V_{in} = 600mV.

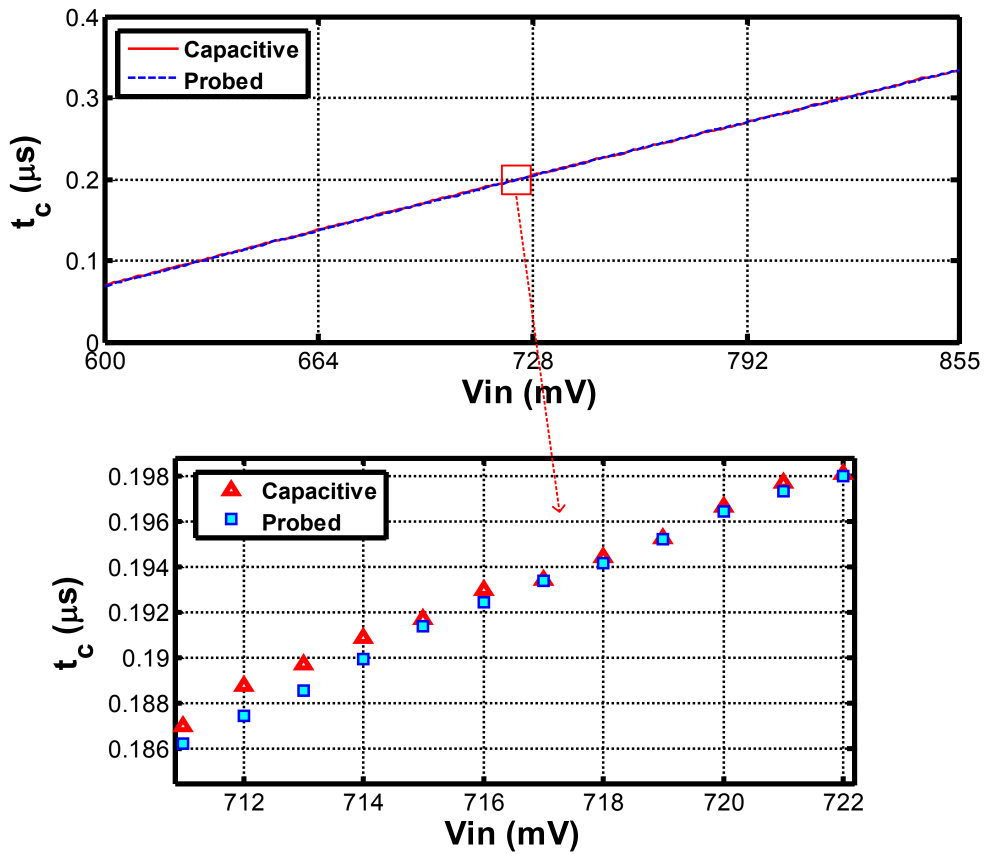


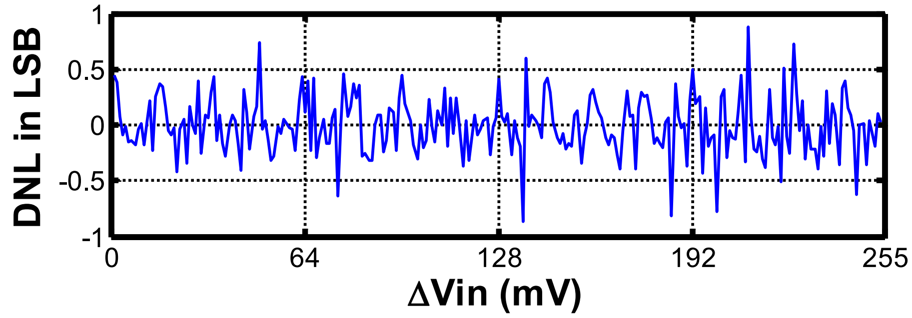
Figure 5.11 Measured t_c with V_{in} from 600 mV to 855 mV with 1 mV step.

Based on this, the capacitive channel gain is about −8.48 dB. The pulse width is 82 ps for wired testing and 89 ps for the wireless setup. To check the repeatability of the measurements, testing with the wireless setup were conducted multiple times with a fixed V_{in}. Figure 5.10 shows the histograms of three different wireless setups with V_{in} of 600 mV. For each measurement, a thousand samples were taken. Assuming a target resolution of 8 bits for the LSB, we can conclude that the variation is within the acceptable range.

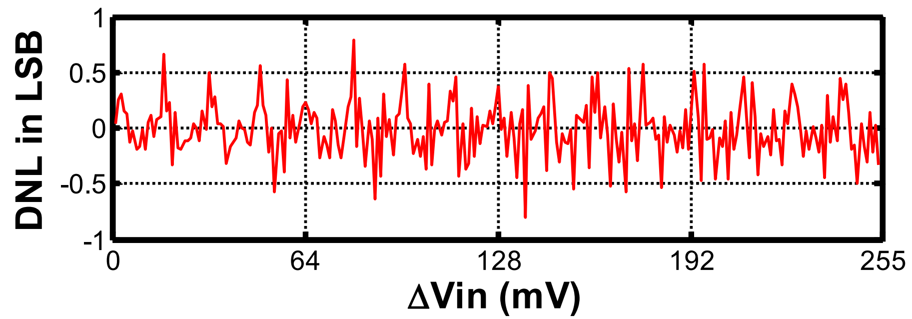
Since the operational amplifier, comparator, and switches are non-ideal, they all contribute to the non-linearity of the voltage-to-time conversion. In addition, the comparator adds a different delay to the UWB pulses. The *start* signal is directly given by the digital controller, but the *done* signal is generated by the comparator with a fixed latency after the zero-crossing. The buffer stage is intended to match different delays. Process and temperature variation also exist.

The time data measured with varying input voltage V_{in} is plotted in Figure 5.11. More than 1000 points are measured per input voltage step and averaged to remove jitter noise. In order to calculate an ideal LSB width, ideal linearity is assumed with a straight line between an initial discharging time with V_{in} of 600 mV and the final voltage 855 mV. The ideal LSB size is 1.035 ns in the time scale for both the wired and wireless setup. In each case, the time t_c increases monotonically with input voltage.

To check non-linearity, both differential non-linearity (DNL) and integral non-linearity (INL) are measured in Figures 5.12 and Figure 5.13. The maximum DNL is 0.88 of the LSB for the wired setup, and 0.80 of the LSB for the wireless setup. In both cases, there is no missing code. Since both have good monotonicity over the input voltage range,

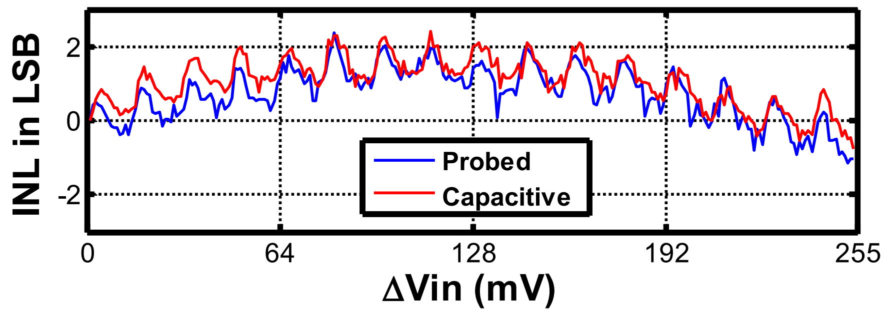


(a)

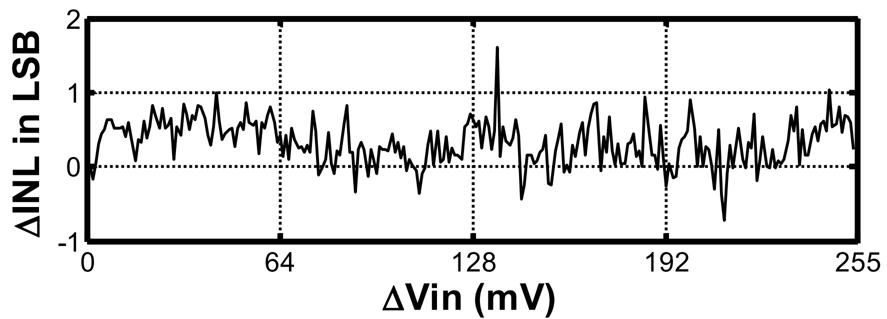


(b)

Figure 5.12 Measured DNL for (a) wired setup and (b) wireless setup.



(a)



(b)

Figure 5.13 (a) Measured INL and (b) INL added by the wireless channel.

the prototype can be used for voltage measurements. The INL measurement in Figure 5.13 shows that the prototype is quite non-linear. This is mainly because the gain of the operational amplifier is not sufficient, and the pulse generator and non-ideal MOS switches contribute non-leariry. The difference from the wired measurements is also presented in Figure 5.12(b). Based on the measurement data, we can conclude that the wireless setup provides performance comparable to that of the wired setup. Due to the small pulse amplitude, the output pulses are more prone to noise and jitter in the wireless setup. However, these random effects are greatly reduced by averaging values from a sufficiently large number of measurements. Also, the measurements were conducted multiple times, and the results are consistent. In every measurement, the outputs are monotonic with no missing codes. Good monotonicity produces a one-to-one match between the input voltage V_{in} and the measured time t_c changes. This prototype chip can measure DC voltage with 1 mV voltage resolution. Since the state-of-the-art on-chip bandgap voltage reference circuits can only achieve resolution of 3 mV without post tuning or trimming, the wireless voltage measurement circuits do not limit the measurement accuracy when the prototype is equipped with an on-chip reference generator [25].

5.6 Summary

A prototype design of wireless voltage measurement circuits has been implemented in a 0.13 μm CMOS process. It can convert DC input voltage in the range 600 mV to 855 mV to timing information, and deliver the result wirelessly to a tester. The prototype achieved 1 mV resolution for voltage measurement. The non-linearity of a

capacitive channel was also evaluated. The degradation of the channel seems relatively small compared to other design factors such as the linearity of the integrator, non-ideal switching, and the latency of the comparator. In addition, since it utilizes a capacitively-coupled channel with the smaller pads and compact on-chip circuitry, it can be placed easily where voltage measurement is needed. The effects of cross-talk and interference from adjacent channels are negligible in capacitive coupling [34]. We can conclude that the proposed architecture for wireless voltage measurement is feasible for wireless analog IC testing and wireless characterization.

Chapter VI

Contributions and Future Work

In this chapter, the contributions of this dissertation are summarized. Ideas for future work are suggested as well.

6.1 Thesis Contributions

This dissertation addresses the design and implementation of circuits to support wireless testing of ICs. The circuit technology for wireless IC testing requires a short communication distance, small area consumption, and robust communication. Two prototype ICs incorporating wireless testing systems were fabricated and tested with the proposed methods of testing digital circuits. Both successfully demonstrated gigahertz communication speeds with a bit-error rate less than 10^{-11}. A third prototype IC containing analog voltage measurement circuits was implemented to determine the feasibility of wirelessly testing analog circuits. The fabricated prototype achieved satisfactory voltage measurement with 1 mV resolution.

The main contributions of the dissertation are summarized as follows:

- A new channel model of capacitve coupling in the context of bond pads that can be used for both wireless and wirebond connections was proposed. This

provides more accurate frequency response, and includes the effects of cross-talk, DC-level shift, and misalignment.

- A compact CDR architecture was proposed and demonstrated to avoid a dedicated clock channel. This design employs feed-forward clock selection and counter-based majority voting which can be easily implemented with scalable digital circuits.

- We successfully fabricated and tested two prototype implementations for wireless testing via capacitive coupling to validate the proposed channel model and CDR architecture.

- Wireless voltage measurement circuits were designed and implemented in a test chip to check feasibility of wireless analog IC testing. This is one of the first voltage measurement prototypes for wireless IC testing.

Channel Model: Prior channel models of capacitive coupling do not consider separate ground nodes for ATE and the DUT, which may contribute to parasitic inductance from long current return paths. We proposed a new model with separate ground effects to provide a more intuitive way to design antennas and circuits for efficient and robust communication. To improve accuracy, the effects of misalignment, DC-level shift, and cross-talk were analytically modeled and evaluated. The BER experiments with prototype chips proved the correctness of the model and our earlier simulation results.

CDR Architecture: The implemented prototype chip with the proposed CDR architecture is one of the first I/O links intended for wireless testing, which delivers clock and data

signals together. We proposed PWM and PPM with RZ signaling schemes to embed the clock into the data steam. A new 1-cycle PD was presented to achieve a compact DLL design. The proposed feed-forward clock selector greatly improves BER performance for PWM symbols. A counter-based bit-decision scheme was also used for the near-optimum detection of PPM RZ signals. These circuits were built with digital circuits which are compact and scalable.

Prototype Chips for Digital IC Testing: Two prototype test chips were fabricated and tested to validate the proposed channel model and architecture. The first chip achieves a data rate of 900 Mbps with BER less than 10^{-13}. It consumes 7.29 mW with a communication distance of 14 μm when no ESD loading is assumed. The second chip achieves 1-Gbps communication speed with BER below 10^{-11}. Wireless communication with chip separation of 10 μm was demonstrated with ESD protection circuits. The power consumption is measured as 10.4 mW.

Wireless Analog IC Testing: The feasibility of wireless testing for analog ICs via capacitive coupling was also demonstrated with a prototype chip. The non-linearity and distortion added by the wireless channel was measured and compared to a wired case. This wireless prototype leverages the advantages of capacitive coupling such as robustness against cross-talk from adjacent channel and good misalignment tolerance.

6.2 Suggestions for Future Work

We have successfully validated our models and design for wireless testing with three prototype CMOS chips employing near-field capacitive communication. The following three directions can be pursued in the future to make wireless testing more realistic.

We focused on wireless signal transfer between the ATE and the DUTs, and assumed that power connections remain wired. Although reducing the number of signal probes mitigates many problems arising from conventional probes, electric power needs to be delivered wirelessly for complete wireless testing. There has been active research on wireless power transfer through either capacitive or inductive coupling for various applications [3][11][33][61][79][88]. Die-level feasibility was also studied for 3D ICs and contactless assembly to PCBs. Still the power density per area and the efficiency of power transfer is insufficient for use in wafer-level testing. Therefore, wireless power transfer for partial circuits under test or wirelessly powered on-chip characterization circuits are more practical.

For wafer-level wireless testing, the number of input and output ports makes it difficult to use wireless testing for very large and complex designs due to excessive testing time, insufficient bandwidth, and the number of channels. To reduce the number of input/output pads while keeping good controllability and observability in testing, built-in self-test (BIST) circuits have been widely used for large and complex DUTs. On-chip BIST circuits reduce the amount of data to be transferred between a DUT and a tester. The saved bandwidth can be used to increase the number of test points on the DUTs. This

can be regarded as a trade-off between the bandwidth per DUT and the number of DUTs. BIST employs a test pattern generator for local or entire blocks of a DUT, and can compare output responses from the DUT to predetermined signatures for verification. A DUT with BIST requires much less input and output test data. Due to this, we may achieve massively parallel testing for single or multiple dice with BIST. Wireless BIST circuits may be implemented with a base station on the tester and multiple self-contained test stations on the DUT. Such an unbalanced communication system is widely used in low-power communication system such as radio-frequency identification tags and readers in [61].

Automatic gain control (AGC) and automatic switching between wireless and wired modes can be studied in the future as well. Although we utilized adjustable transmitter power for the second prototype, it can be adjusted off-chip. AGC is a widely-used technique to control the transmit power with a feedback loop to maintain good BER performance. With AGC, the BER performance can be reliably maintained at a certain level even with misalignment or process variations. Automatic switching between wireless and wired mode is also beneficial. For example, wireless or wired mode can be automatically set by measuring impedance at the ground pad. For the wireless setup, the ground pads have relatively high impedance at low frequency, but they become very low impedance nodes with wire bonding to ground. Then, the wireless testing system does not need to configure wireless pads independently with extra control circuitry, and the system complexity can be greatly alleviated.

This dissertation has demonstrated the feasibility of wireless IC testing by providing analytical channel models and architectures for robust communication. It is

hoped that the results will prove useful in designing efficient and cost-effective wireless communication systems for testing of ICs.

APPENDICES

Appendix A

Near-Field Basics

RF is used in most forms of wireless communication systems. Recently, relatively short range communication, such as body area network (BAN) and personal area network (PAN), is attracting research interest. Near-field communication has become a strong candidate because of its high efficiency and low power consumption [36][75][78][89]. Here, we present background theory for near-field communication.

An electromagnetic field is completely described by Maxwell's equations.

$$\nabla \times E = -\frac{\partial B}{\partial t},$$

$$\nabla \times H = J_s + \frac{\partial D}{\partial t},$$

$$\nabla \cdot D = \rho_s,$$

$$\nabla \cdot B = 0. \qquad \text{(A.1)}$$

Near-field and far-field characteristics of the field can be understood by solutions in terms of the distance R from the radiation source.

The electric and magnetic field cannot be analyzed independently because the time-dependent magnetic field is necessarily coupled with the electric field. However, sometimes we can solve field problems in which we can neglect displacement currents to simplify the relevant Maxwell's equations. This is called a quasi-static electromagnetic field assumption. ($\partial D/\partial t = 0$) Once the quasi-static condition has been met, the field solution becomes one of circuit theory rather than the propagating wave solution. Quasi-static equations have a form equivalent to the heat diffusion equations, which means the

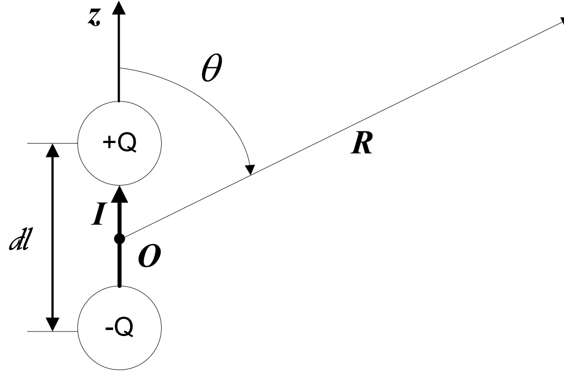


Fig. A.1. Elemental electric dipole.

mechanism of energy transfer is diffusion rather than a propagating wave [18].

The elemental electric dipole is the simplest type of radiating system. We examine both near-field and far-field assumptions and how they are related to a propagating electromagnetic wave and quasi-static field.

For the region sufficiently near to the dipole, $\beta R = 2\pi R/\lambda \ll 1$, and if we solve Maxwell's equations (A.1), E becomes

$$E_R = \frac{p}{4\pi\varepsilon_0 R^3} 2\cos\theta,$$
$$E_\theta = \frac{p}{4\pi\varepsilon_0 R^3} \sin\theta, \qquad \text{(A.2)}$$
$$E_\phi = 0$$

where $p = \hat{a}Qdl = \hat{a}\left(\pm\frac{I}{j\omega}\right)dl, c = 1/\sqrt{\mu_0\varepsilon_0}$. p is an electric dipole moment. μ_0 and ε_0 are permeability and permittivity of free space respectively. The resulting solution is identical to that of the electric field intensity from the static electric field theory. This implies that the near-field of a dipole can be approximated as quasi-static. The region $\beta R = 2\pi R/\lambda \gg 1$ is the far-field zone. This condition results in

$$E_\theta = j\frac{Id\ell}{4\pi}(\frac{e^{-j\beta R}}{R})\eta_0\beta\sin\theta \tag{A.3}$$

where $\eta_0 = \sqrt{\mu_0 / \varepsilon_0}$. The electromagnetic solutions in the far-field zone have the same properties as those of a plane wave. We can derive the solutions for the elemental magnetic dipole by a similar approach.

With no approximation, the general solutions of the elemental electric or magnetic dipole have the terms, $1/R$, $1/R^2$ and $1/R^3$, which correspond with the radiation, induction and quasi-static terms [18]. The dominant term is decided according to the distance and frequency. For the near-field case, the quasi-static term dominates, and the radiation term is dominant for the far-field solutions. The boundary that divides the near and far fields is called the far-field or Fresnel zone condition.

Once the near-field magnetic condition is satisfied, we can calculate the mutual inductance between coupled inductors or the capacitance of coupled capacitors. The equations for inductance are derived from Ampere's law and are the same as what is used in circuit theory. Using two coupled magnetic dipoles placed parallel to each other in the near field, we can derive mutual inductance M and the coupling coefficient k.

$$k = \frac{M}{\sqrt{L_1L_2}} = \frac{\mu\pi r_1^2 r_2^2 N_1N_2}{2R^3\sqrt{L_1L_2}}. \tag{A.4}$$

Here, r denotes the radius of the magnetic dipole, and N is the number of turns. The self-inductance of coupled coils is given by L, and R is the distance between the coils. In most practical cases, there exist flux leakage and misalignment issues. The mutual inductance should be calculated with compensation for the leakage and variation of geometry.

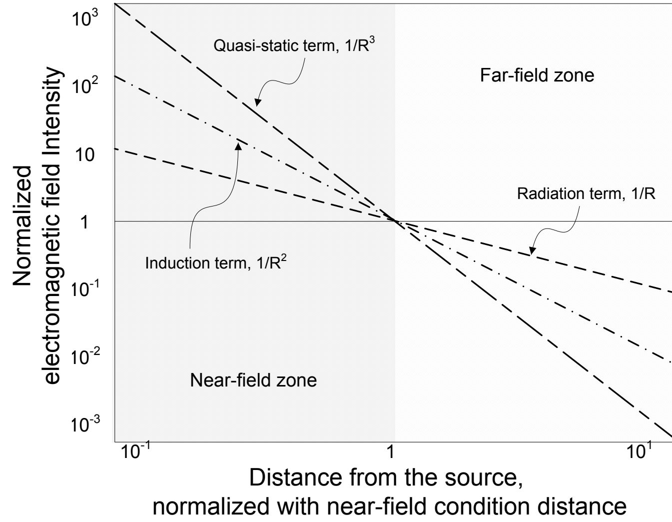


Fig. A.2. Near-field and far-field boundary based on [18].

Capacitance can be represented as follows.

$$C = \varepsilon \frac{A}{R} \tag{A.5}$$

Here ε is the permittivity of the medium, A denotes the overlap area, and R is the separation between the two plates. This equation is valid when the dimension of the plates is much larger than R. If not, the fringing effect of plate edges becomes significant, and the capacitance may differ from the above expression.

Appendix B

Clock Data Recovery with PWM Signals

For both very high-speed wired communication and wireless communication, synchronization is of the utmost importance since demodulation highly depends on clock timing [66][80][83]. A communication channel usually distorts both the phase and amplitude of transmitted signals. Phase changes in the received signal make the reconstruction of data even more difficult. We can send a reference clock through the extra channel independent of the data channel, but in most cases such an additional channel is unavailable or wasteful. For our design, since we use a bond pad as an electrode, we use only one channel. Thus, we must embed clock information along with data transmission. For example, Manchester coding in the Ethernet specifications has the clock information encoded as rising or falling edge for symbols. Because every bit contains a rising or falling transition, a simple analog filter can extract clock information from Manchester-coded data.

mB/nB encoding is a well-known baseband encoding method for clock embedding in CDR; mB/nB means that there exists at least one rising transition in an n-bit binary data packet, and integer m is less than integer n [83]. In simpler terms, the encoded signals contain m-bit data in an n-bit data packet. The transition is called the master transition and does not contain any information except clock synchronization information. Either a DLL or PLL with a $1/n$ divider can synchronize a clock to the master transition regardless of data bits. A DLL or PLL compares phase between the master transition and each nth rising edge of the clock to maintain the synchronization. It ignores any transition other than the master transition due to the $1/n$ divider. For example,

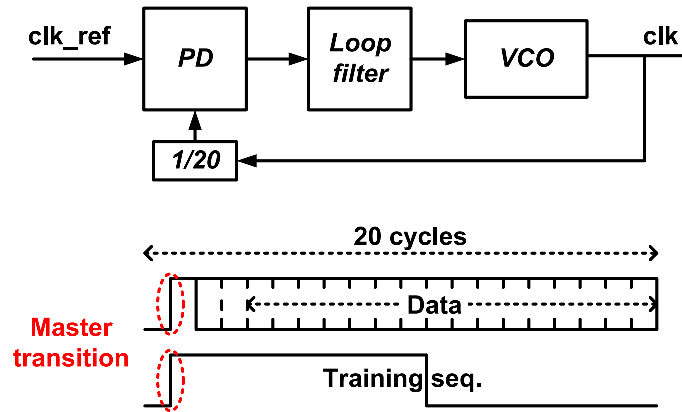


Fig. B.1. Illustration of 16B/20B encoding and CDR by a PLL [83].

Figure 11 shows the bit configuration of 16B/20B encoding. Because master transitions occur in each 20-bit data sequence, we can adjust the phase of a locally generated clock to synchronize to the master transition using a PLL with a 1/20 divider. To make sure to match the packet boundary, we use a training sequence at the beginning of synchronization, which is sometimes called a preamble. The training sequence doesn't have any rising edges in the packet, and therefore a DLL or PLL can successfully lock the clock to the training sequence. Once a receiver clock locks to the reference, we can send random data with mB/nB encoding.

For simplicity and efficiency, we use 1B/2B encoding with non-return-to-zero (NRZ) signaling. This is also known as PWM; it modulates a signal based on the location of the falling edge. To avoid confusion, we will use the term "PWM" for this dissertation. Since data are modulated at falling edges of the clock in the time domain, we lose 50% of the signals for clock synchronization. However, this modulation simplifies the receiver design by removing the requirement for a PLL because the modulated signals contain embedded clock information. For 1 Gbps baseband modulation, the width of a narrow pulse for the symbol '0' is designed to be 250 ps, and the pulse width for '1' is 750 ps.

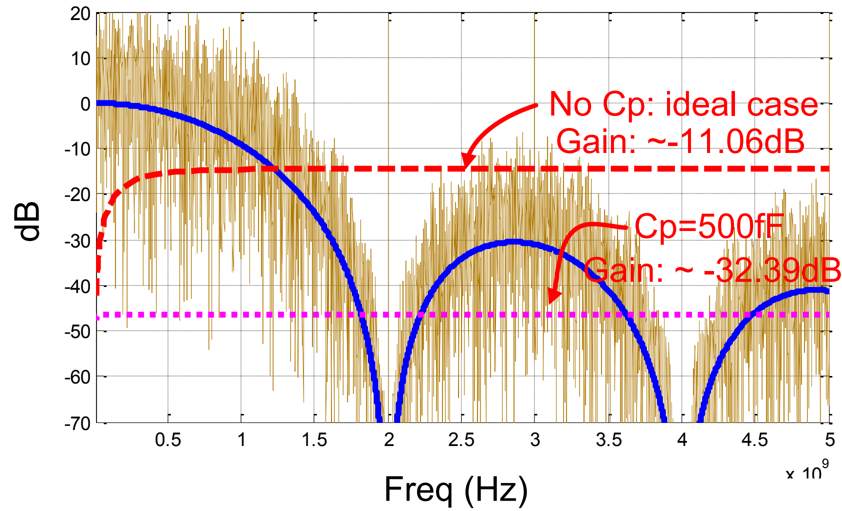


Fig. B.2. Power spectral density of 1 Gbps random PWM signals. Red dotted line is the channel characteristic with parasitic capacitance C_p.

The power spectral density and symbol shapes for 1Gbps baseband signals are shown in Figure B.2. These contain power at DC due to the NRZ encoding. Although our channel model has high-pass characteristics with a cut-off frequency at 100 kHz, we do not lose that much power as long as we use a high enough frequency. For our design, we aim for 1Gbps, and Figure B.2 reveals that the portion of loss from a high-pass channel is negligible. Since PWM signals are not DC-balanced, its DC level fluctuates with the data pattern.

There are three major clock synchronization methods for CDR: a PLL, a DLL, and an injection-locked oscillator [63]. Among these, an injection-locked oscillator is well known for its simple implementation and low power consumption. But it requires passive elements, which are too large to be placed in the I/O pad-sized receiver. Instead of an injection-locked oscillator, PLLs and DLLs are widely used for clock synchronization. An essential difference between these two is the use of a voltage-controlled oscillator (VCO), which is able to adjust not only the phase but also the

frequency of a regenerated clock. For this reason, a PLL is commonly used for CDR circuits when the reference clock has a lot of jitter. However, a DLL also has advantages over a PLL in terms of ease of implementation and stability. We used PWM and a DLL-based demodulator for our design.

Since we use PWM, we reconstruct both clock and data using a DLL. If a phase detector is only sensitive to rising edges, we can synchronize one-cycle-delayed signals to incoming signals regardless of NRZ data since they are modulated in locations of falling edges. A DLL generates multi-phase clocks synchronized with the incoming signals. If we choose one clock edge which is placed in the middle of NRZ data, rising edge flip-flops can reconstruct the proper data. A DLL-based receiver has another advantage over a PLL in terms of jitter immunity and stability. Since a clock is sent with data through the same channel, and jitter noise at every positive clock edge moves NRZ data at the same time, we can reconstruct the transmitted data using a DLL as long as the delayed clock edge is within the NRZ boundary. Since a DLL is a one-pole system, it is unconditionally stable; in contrast, design of a stable PLL requires intensive analysis of a second-order control system. As long as we can linearize a dynamic model of a DLL, a loop can be stabilized. A DLL loop dynamic model can be written as follows.

$$H(s) = \frac{1}{1 + s/\omega_N}, \qquad \omega_N = \frac{K_{PD} I_{CP} K_{DL} F_{REF}}{C_{LF}} \tag{B.1}$$

Here, K_{PD} is the gain of a phase detector, and I_{CP} means the amount of charge pump current, C_{LF} is capacitance of the loop filter, K_{DL} is delay line gain, and F_{REF} is a reference frequency. A general rule of thumb for a DLL is to design it with loop bandwidth ω_N at least 1/10 lower than F_{REF} [63]. With this design criterion, we assume

the DLL is stable, and the dynamic linear model holds against nominal supply voltage noise.

BIBLIOGRAPHY

[1] *Advantest ATE NEWS*, https://www.advantest.com. [Online]. Available: http://www.advantest.com

[2] D. Appello, P. Bernardi, M. Grosso, and M. S. Reorda, "System-in-Package Testing: Problems and Solutions," *IEEE Design & Test of Computers,* vol. 23, pp. 203-211, Jun. 2006.

[3] M. W. Baker and R. Sarpeshkar, "Feedback Analysis and Design of RF Power Links for Low-Power Bionic Systems," *IEEE Trans. on Biomedical Circuits and Systems*, vol. 1, pp. 28-38, Mar. 2007.

[4] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Springer, 2000.

[5] R. Canegallo, M. Mirandola, A. Fazzi, L. Magagni, R. Guerrieri, and K. Kaschlun, "Electrical Measurement of Alignment for 3D Stacked Chips," in *Proc. ESSCIRC*, pp. 347-350, Sep. 2005.

[6] K. Chakrabarty and E. J. Marinissen, "Test Challenges and Solutions in TSV-Based 3D Stacked ICs," in *Proc*. *IEEE European Test Symposium*, May 2009.

[7] K. Chandrasekar, J. Wilson, E. Erickson, Z. Feng, J. Xu, S. Mick, and P. Franzon, "Inductively Coupled Connectors and Sockets for Multi-Gb/s Pulse Signaling," *IEEE Trans. on Advanced Packaging*, vol. 31, pp. 749-758, Nov. 2008.

[8] D. K. Cheng, *Field and Wave Electromagnetics*, *Second Edition*, Addison-Wesley, 1989.

[9] W.-J. Choe, B.-J. Lee, J. Kim, D.-K. Jeong, and G. Kim, "A Single-Pair Serial Link for Mobile Displays with Clock Edge Modulation Scheme," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2012-2020, Sep. 2007.

[10] W. S. Coates, R. J. Bosnyak, and I. E. Sutherland, "Method and Apparatus for Probing an Integrated Circuit through Capacitive Coupling," *US Patent 6,600,325*, July 2003.

[11] E. Culurciello and A. G. Andreou, “Capacitive Inter-Chip Data and Power Transfer for 3-D VLSI,” *IEEE Trans. on Circuits and Systems Part 2 Express Briefs*, vol. 53, pp. 1348, Dec. 2006.

[12] M. Daito, Y. Nakata, H, Gomyo, H. Kusamitsu, Y. Komoto, K. Iizuka, K. Ikeuchi, G. S. Kim, M. Takamiya, and T. Sakurai, “Capacitively Coupled Non-Contact Probing Circuits for Membrane-Based Wafer-Level Simultaneous Testing,” *IEEE J. Solid-State Circuits*, vol. 46, pp. 2386-2395, Sep. 2011.

[13] N. Drego, A. Chandrakasan, and D. Boning, “A Test-Structure to Efficiently Study Threshold-Voltage Variation in Large MOSFET Arrays,” in *Proc. IEEE Int’l Symp. on Quality Electronic Design,* pp. 281-286, Mar. 2007.

[14] A. Fazzi, L. Magagni, M. Mirandola, B. Charlet, L. Di Cioccio, E. Jung, and R. Canegallo, “3-D Capacitive Interconnections for Wafer-Level and Die-Level Assembly,” *IEEE J. Solid-State Circuits*, vol. 42, pp. 2270-2282, Oct. 2007.

[15] A. Fazzi, R. Canegallo, L. Ciccarelli, L. Magagni, F. Natali, E. Jung, P. L. Rolandi, and R. Guerrieri, “3-D Capacitive Interconnections with Mono- and Bi-Directional Capabilities,” *IEEE J. Solid-State Circuits,* vol. 43, pp. 275-284, Jan. 2008.

[16] B. Floyd, K. Kim, and K. K. O, “Wireless Interconnection in a CMOS IC with Integrated Antennas,” in *ISSCC Dig. Tech. Papers,* pp. 238-239, Feb. 2000.

[17] Q. Gu, Z. Xu, J. Ko, and M.-C. F. Chang “Two 10 Gb/s/pin Low-Power Interconnect Methods for 3D ICs,” in *ISSCC Dig. Tech. Papers,* pp. 448-449, Feb. 2007.

[18] Z. Haznadar et al., *Electromagnetic Fields, Waves and Numerical Methods*, IOS Press, 2000.

[19] R. Ho, T. Ono, R. D. Hopkins, A. Chow, J. Schauer, F. Y. Liu, and R. Drost, “High Speed and Low Energy Capacitively Driven On-Chip Wires,” *IEEE J. Solid-State Circuits*, vol. 43, pp. 52-60, Jan. 2008.

[20] D. Hopkins, A. Chow, R. Bosnyak, B. Coates, J. Ebergen, S. Fairbanks, J. Gainsley, R. Ho, J. Lexau, F. Liu, T. Ono, J. Schauer, I. Sutherland, and R. Drost, "Circuit Techniques to Enable 430Gb/s/mm2 Proximity Communication," in *ISSCC Dig. Tech. Papers*, pp. 368-369, Feb. 2007.

[21] M. Hossain and A. C. Carusone, "5-10 Gb/s 70 mW Burst Mode AC Coupled Receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 524-537, Mar. 2010.

[22] Y.-T. Hsing, L.-M. Denq, C.-H. Chen, and C.-W. Wu, "Economic Analysis of the HOY Wireless Test Methodology," *IEEE Design & Test*, vol. 27, pp. 20-30, May 2010.

[23] H. Ishikuro, T. Sugahara, and T. Kuroda, "An Attachable Wireless Chip Access Interface for Arbitrary Data Rate Using Pulse-Based Inductive-Coupling through LSI Package," in *ISSCC Dig. Tech. Papers*, pp. 360-363. 2007.

[24] T. Itoh, S. Kawamura, T. Suga, and K. Kataoka, "Development of an Electrostatically Actuated MEMS Switching Probe Card," in *Proc. Int'l Conf. on Electrical Contacts*, pp. 226-230, Sep. 2004.

[25] V. Ivanov, R. Brederlow, and J. Gerber, "An Ultra Low Power Bandgap Operational at Supply from 0.75V," *IEEE J. Solid State Circuits*, vol. 47, pp. 1-9, July 2012

[26] J. J. Johansson, *Near-Field and Far-Field Theory*, http://www.sm.luth.se. [Online]. Available: http://www.sm.luth.se/~urban/master/Theory/3.html

[27] A. Jussila and J. Takaneva, "Contactless Interconnection Methods – Capacitively Coupled Interconnection in Mobile Devices," in *Proc. Workshop on Signal Propagation on Interconnects*, pp. 1-4, May 2008.

[28] E. Karl, P. Singh, D. Blaauw, and D. Sylvester, "Compact In-Situ Sensors for Monitoring Negative-Bias-Temperature-Instability Effect and Oxide Degradation," in *ISSCC Dig. Tech. Papers*, pp. 410-411, Feb. 2006.

[29] C. H. Kim, K. Roy, R. K. Krishnamurthy, and S. Borkar, “An On-Die CMOS Leakage Current Sensor for Measuring Process Variation in Sub-90nm Generations”, in *Symp. on VLSI Circuits Dig. Tech. Papers*, pp. 250-251, Jun. 2004.

[30] G.-S. Kim, M. Takamiya, and T. Sakurai, “A 25-mV-Sensitivity 2-Gb/s Optimum-Logic-Threshold Capacitve-Coupling Receiver for Wireless Wafer Probing Systems,” *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 56, pp. 709-713, Sep. 2009.

[31] G.-S. Kim, K. Ikeuchi, M. Daito, M. Takamiya, and T. Sakurai, “A High-Speed, Low-Power Capacitive-Coupling Transceiver for Wireless Wafer-Level Testing Systems,” in *Proc. IEEE Int'l 3D System Integration Conf.*, Nov. 2010.

[32] T.-H. Kim, R. Persaud, and C. H. Kim, “Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits,” *IEEE J. Solid-State Circuits*, vol.43, pp.874-880, Apr. 2008.

[33] A. Kurs, A. Jaralis, R. Moffatt, J. D. Joannopoulos, P, Fisher, and M. Soljacic, “Wireless Power Transfer via Strongly Coupled Magnetic Resonances,” *Science*, vol. 317, pp. 83-86, Jul. 2007.

[34] D. Y. Lee, D. D. Wentzloff, and J. P. Hayes, “Wireless Wafer-Level Testing of Integrated Circuits via Capacitively-Coupled Channels,” in *Proc. IEEE DDECS*, pp. 99-104, Apr. 2011.

[35] D. Y. Lee, D. D. Wentzloff, and J. P. Hayes, “A 900 Mbps Single-Channel Capacitive I/O Link for Wireless Wafer-Level Testing of Integrated Circuits,” in *A-SSCC Dig. Tech. Papers*, pp.153–156, Nov. 2011.

[36] S. Lee, K. Song, J. Yoo, and H.-J. Yoo, “A Low-Energy Inductive Coupling Transceiver with Cm-Range 50-Mbps Data Communication in Mobile Device Applications,” *IEEE J. Solid-State Circuits*, vol. 45, pp. 2366-2374, Nov. 2010.

[37] S.-K. Lee, Y.-S. Kim, H. Ha, Y. Seo, H.-J. Park, and J.-Y. Shim, "A 650Mb/s-to-8Gb/s Referenceless CDR Circuit with Automatic Acquisition of Data Rate," in *ISSCC Dig. Tech. Paper,* pp. 184-185, Feb. 2009.

[38] J.-J. Lin, L. Gao, A. Sugavanam, X. Guo, R. Li, J. E. Brewer, and K. K. O, "Integrated Antennas on Silicon Substrates for Communication over Free Space," *IEEE Electron Device Letter*, vol. 25, pp. 196–198, Apr. 2004.

[39] Y.-S. Lin, D. Sylvester, and D. Blaauw, "Alignment-Independent Chip-to-Chip Communication for Sensor Applications Using Passive Capacitve Signaling," *IEEE J. Solid-State Circuits*, vol. 44, pp. 1156-1166, Apr. 2009.

[40] S. Luan, A. Eftekhar, O. H. Murphy, and T. G. Constandinou, "Towards an Inductively Coupled Power/Data Link for Bondpad-less Silicon Chips," in *Proc. Int'l Symp. on Circuits and Systems*, pp. 2597-2600, May 2011.

[41] L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, and P. Franzon, "3 Gb/s AC Coupled Chip-to-Chip Communication Using a Low Swing Pulse Receiver," *IEEE J. Solid-State Circuits,* vol. 41, pp. 287-296, Jan. 2006.

[42] L. Luo, J. Wilson, S. Mick, L. Zhang, E. Erickson, and P. Franzon, "A 36Gb/s ACCI Multi-Channel Bus Using a Fully Differential Pulse Receiver," in *Proc. Custom Integrated Circuits Conference*, pp. 773-776, Sep. 2006.

[43] A. Majumdar, J. E. Cunningham, and A. V. Krishnamoorthy, "Alignment and Performance Considerations for Capacitive, Inductive, and Optical Proximity Communication," *IEEE Trans. on Advanced Packaging*, vol. 33, pp. 690-701, Aug. 2010.

[44] W. R. Mann, F. L. Taber, P. W. Seitzer, and J. J. Broz, "The Leading Edge of Production Wafer Probe Test Technology," in *Proc. Int'l Test Conf.,* pp. 1168-1195, Oct. 2004.

[45] E. J. Marinissen, D. Y. Lee, J. P. Hayes, C. Sellathamby, B. Moore, S. Slupsky, and L. Pujol, "Contactless Testing: Possibility or Pipe-Dream?," in *Proc. Design, Automation, and Test in Europe (DATE*), pp. 676–678, Apr. 2009.

[46] E. J. Marinissen and T. Zorian, "Testing 3D Chips Containing Through-Silicon Vias," in *Proc. IEEE International Test Conf.*, pp. 1-11, Nov. 2009.

[47] N. van der Meijs and J. T. Fokemma, "VLSI Circuit Reconstruction from Mask Topology," *Integration*, vol.2, pp. 85-119, 1984.

[48] P. P. Mercier and A. P. Chandrakasan, "A Supply-Rail-Coupled eTexiles Transceiver for Body-Area Networks," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1284-1295, June 2011.

[49] D. A. B. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," *Proc. IEEE*, vol. 88, pp. 728-749, Jun. 2000.

[50] N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Analysis and Design of Inductive Coupling and Transceiver Circuit for Inductive Inter-Chip Wireless Superconnect," *IEEE J. Solid-State Circuits*, vol. 40, pp.829-837 Apr. 2005.

[51] N. Miura, D. Mizoguchi, M. Inoue, K. Niitsu, T. Nakagawa, M. Tago, M. Fukaishi, T. Sakurai, and T. Kuroda, "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," in *ISSCC Dig. Tech. Papers*, pp. 1676-1677, Feb. 2006.

[52] N. Miura, H. Ishikuro, T. Sakurai, and T. Kuroda, "A 0.14 pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping," in *ISSCC Dig. Tech. Papers*, pp. 358-359, Feb. 2007.

[53] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, and T. Kuroda, "An 11Gb/s Inductive-Coupling Link with Burst Transmission," in *ISSCC Dig. Tech. Papers*, pp. 298-299, Feb. 2008.

[54] N. Miura, Y. Yuan, S. Kawai, K. Takatsu, Y. Asano, and T. Kuroda, "A 0.55 V 10 fJ/bit Inductive-Coupling Data Link and 0.7 V 135 fJ/Cycle Clock Link with Dual-Coil Transmission Scheme," *IEEE J. Solid-State Circuits*, vol. 46, pp. 965-973, Apr. 2011.

[55] B. Moore, M. Margala, and C, Backhouse, "Design of Wireless On-Wafer Submicron Characterization System," *IEEE Trans. on VLSI*, vol. 13, pp. 169-180, Feb. 2005.

[56] B. Moore, M. Mangrum, C. Sellathamby, M. Reja, T. Weng, B. Bai, E. Reid, I. Filanovsky, and S. Slupsky, "Non-Contact Testing for SoC and RCP (SIPs) at Advanced Nodes," in *Proc. Int'l Test Conf.*, pp. 1-10, Oct. 2008.

[57] S. Mukhopadhyay, K. Kim, K. A. Jenkins, C.-T. Chuang, and K. Roy, "Statistical Characterization and On-Chip Measurement Methods For Local Random Variability of a Process Using Sense-Amplifier Based Test Structure," in *ISSCC Dig. Tech. Papers,* pp. 400-401, Feb. 2007.

[58] Pacific Asian Systems Supply Ltd., *Product Introduction*, [Online]. Available: http://pass.emenda.net.

[59] P. Park, L. Chen, L. Wang, S. Long, H. K. Yu, and C. P. Yue, "On-Wafer Wireless Testing and Mismatch Monitoring Using RF Transmitters with Integrated Antennas," in *Proc. IEEE RFIC Symp*., pp. 505-508, Jun. 2009.

[60] B. Provost and E. Sanchez-Sinencio, "On-Chip Ramp Generators for Mixed-Signal BIST and ADC Self-Test," *IEEE J. Solid-State Circuits*, vol. 38, pp. 263-273, Feb. 2003.

[61] K. Ramakrishnan, "Performance Benchmarks for Passive UHF RFID Tags," M.S. dissertation, the University of Kansas, 2005.

[62] B. Razabi, "CMOS Technology Characterization for Analog and RF Design," *IEEE J. Solid-State Circuits*, vol. 34, pp. 268-276, Mar. 1999.

[63] B. Razavi, *Phase-Locking in High-Performance Systems*, IEEE Press, Wiley-Interscience, 2003.

[64] G. W. Roberts, "Metrics, Techniques and Recent Developments in Mixed-Signal Testing," in *Proc. IEEE/ACM Int'l Conf. on Computer Aided Design*, pp. 514-521, Nov. 1996.

[65] G. W. Roberts, "Improving the Testability of Mixed-Signal Integrated Circuits," in *Proc. Custom Integrated Circuits Conference*, pp. 214-221, May 1997.

[66] L. Rodoni, G. von Büren, A. Huber, M. Schmatz, and H. Jäckel, "A 5.75 to 44Gb/s Quarter Rate CDR with Data Rate Selection in 90nm Bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 44, pp. 1927-1941, Jul. 2009

[67] D. Salzman and T. Knight, "Capacitive Coupling solves the Known Good Die Problem," in *Proc. IEEE Multi-Chip Module Conference*, pp. 95-99, Mar. 1994.

[68] Samsung Electronics, *1Gb D-die DDR3 SDRAM Specification, Rev. 1.1*, Aug. 2008.

[69] M. Scandiuzzo, S. Cani, L. Perugini, S, Spolzino, R. Canegallo, L. Perilli, R. Cardu, E. Franchi, and C. Gozzi, and F. Maggioni, "Input/Output Pad for Direct Contact and Contactless Testing," in *Proc. IEEE European Test Symp.*, May 2011.

[70] E. F. Scarselli, A. Gnudi, F. Natali, M. Scandiuzzo, R. Canegallo, and R. Guerrieri, "Automatic Compensation of the Voltage Attenuation in 3-D Interconnection Based on Capacitive Coupling," *IEEE J. Solid-State Circuits*, vol. 46, pp. 498-506, Feb. 2011.

[71] C. V. Sellathamby, M. Reja, L. Fu, B. Bai, E. Reid, S. H. Slupsky, I. M. Filanovsky, and K. Iniewski, "Non-Contact Wafer Probe Using Wireless Probe Cards," in *Proc. Int'l Test Conf.,* 6 pp. -452, Nov. 2005.

[72] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors 2009 Edition*, 2009.

[73] Semiconductor Industry Association (SIA), *SIA Roadmap 2003,* 2003.

[74] J. Seo, R. Ho, J. Lexau, M. Dayringer, D. Sylvester, and D. Blaauw, "High-Bandwidth and Low-Energy On-Chip Signaling with Adaptive Pre-emphasis in 90nm CMOS," in *ISSCC Dig. Tech. Papers*, pp. 182-183, Feb. 2010.

[75] M. Shinagawa, M. Fukumoto, K. Ochiai, and J. Kyuragi, "A Near-Field Sensing Transceiver for Intrabody Communication Based on the Electrooptic Effect," in *Proc. IEEE Trans. Instrum. Meas.,* vol. 53, pp. 1533-1538, Dec. 2004.

[76] K. Shingo, K. Katoka, T. Itoh, and T. Suga, "Design and Fabrication of an Electrostatically Actuated MEMS Probe Card," in *Proc. Int'l Conf. on Transducers, Solid State Sensors, Actuators and Microsystems*, vol. 2, pp. 1522-1525, Jun. 2003.

[77] K. Smith, "RF Membrane Probe Cards," *Southwest Test Workshop Technical Program*, Jun. 1998.

[78] S.-J. Song, N. Cho, and H.-J. Yoo, "A 0.2-mW 2-Mb/s Digital Transceiver Based on Wideband Signaling for Human Body," *IEEE J. Solid-State Circuits,* vol. 42, pp. 2021-2033, Sep. 2007.

[79] J. Tompson, A. Dolin, and P. Kinget, "2.6GHz RF Inductive Power Delivery for Contactless On-Wafer Characterization," in *Proc. Int'l Conf. on Microelectronic Test Structures*, pp. 175-179, Mar. 2008.

[80] O. Tyshchenko, A. Sheikholeslami, H. Tamura, M. Kibune, H. Yamaguchi, and J. Ogawa, "A 5-Gb/s ADC-Based Feed-Forward CDR in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1091-1098, Jun. 2010.

[81] *Understanding Integrating ADCs*, Maxim Integrated Product, Inc., [Online] Available: http://www.maxim-ic.com/app-notes/index.mvp/id/1041

[82] A. Valdes-Garcia, F. A.-L. Hussien, J. Silva-Martinez, and E. Sanchez-Sinencio, "An Integrated Frequency Response Characterization System with a Digital

Interface for Analog Testing," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2301-2313, Oct. 2006.

[83] R. Walker, "Clock and Data Recovery for Serial Digital Communication," *ISSCC Short Course*, Feb. 2002.

[84] Y. Wang, A. M. Niknejad, V. Gaudet, and K. Iniewski, "A CMOS IR-UWB Transceiver Design for Contact-Less Chip Testing Applications," *IEEE Trans. on Circuits and Systems-II*, vol. 55, pp. 334-338, Apr. 2008.

[85] Y. Yoshida, K. Nose, Y. Nakagawa, K. Noguchi, Y. Morita, M. Tago, and T. Kuroda, and M. Mizuno, "Wireless DC Voltage Transmission Using Inductive-Coupling Channel for Highly-Parallel Wafer-Level Testing," in *ISSCC Dig. Tech. Papers*, pp. 470-471, Feb. 2009.

[86] I. Young, J. K. Greason, and K. L. Wong, "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1599-1607, Nov. 1992.

[87] C. P. Yuan and T. N. Trick, "A Simple Formula for the Estimation of the Capacitance of Two-Dimensional Interconnects in VLSI Circuits," *IEEE Electron Device Letters*, vol. EDL-3, pp. 391-393, 1982.

[88] Y. Yuxiang, N. Miura, S. Imai, H. Ochi, and T. Kuroda, "Digital Rosetta Stone: A Sealed Permanent Memory with Inductive-Coupling Power and Data Link," in *Symp*. on *VLSI Circuits Dig. Tech. Papers*, pp. 26-27, Jun. 2009.

[89] T. G. Zimmermann, "Personal Area Networks: Near-Field Intrabody Communication," *IBM System Journal,* vol. 35, pp. 609-617, 1996.