Energy-Efficient Wireless Circuits and Systems for Internet of Things

by

Jaeho Im

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical and Computer Engineering)
in the University of Michigan
2020

Doctoral Committee:

Associate Professor David D. Wentzloff, Chair
Associate Professor Prabal Dutta, University of California - Berkeley
Professor Anna Gilbert
Assistant Professor Hun-Seok Kim

Jaeho Im

jaeim@umich.edu

ORCID iD: 0000-0002-0223-3751

To God, my family, and all lovely people around me in my life

Table of Contents

List of Tables

List of Figures

Abstract

As the demand of ultra-low power (ULP) systems for internet of thing (IoT) applications has been increasing, large efforts on evolving a new computing class is actively ongoing. The evolution of the new computing class, however, faced challenges due to hard constraints on the RF systems. Significant efforts on reducing power of power-hungry wireless radios have been done. The ULP radios, however, are mostly not standard compliant which poses a challenge to wide spread adoption. Being compliant with the WiFi network protocol can maximize an ULP radio's potential of utilization, however, this standard demands excessive power consumption of over 10mW, that is hardly compatible with in ULP systems even with heavy duty-cycling. Also, lots of efforts to minimize off-chip components in ULP IoT device have been done, however, still not enough for practical usage without a clean external reference, therefore, this limits scaling on cost and form-factor of the new computer class of IoT applications.

This research is motivated by those challenges on the RF systems, and each work focuses on radio designs for IoT applications in various aspects. First, the research covers several endeavors for relieving energy constraints on RF systems by utilizing existing network protocols that eventually meets both low-active power, and widespread adoption. This includes novel approaches on 802.11 communication with articulate iterations on low-power RF systems. The research presents three prototypes as power-efficient WiFi wake-up receivers, which bridges the gap between industry standard radios and ULP IoT radios. The proposed WiFi wake-up receivers operate with low power consumption and remain compatible with the WiFi protocol by using back-channel communication. Back-channel communication embeds a signal into a WiFi

compliant transmission changing the firmware in the access point, or more specifically just the data in the payload of the WiFi packet. With a specific sequence of data in the packet, the transmitter can output a signal that mimics a modulation that is more conducive for ULP receivers, such as OOK and FSK. In this work, low power mixer-first receivers, and the first fully integrated ultra-low voltage receiver are presented, that are compatible with WiFi through back-channel communication. Another main contribution of this work is in relieving the integration challenge of IoT devices by removing the need for external, or off-chip crystals and antennas. This enables a small form-factor on the order of mm^3-scale, useful for medical research and ubiquitous sensing applications. A crystal-less small form factor fully integrated 60GHz transceiver with on-chip 12-channel frequency reference, and good peak gain dual-mode on-chip antenna is presented.

Chapter 1 Introduction

1.1 The Advent of a New Computing Class and the Internet-of-Things (IoTs)

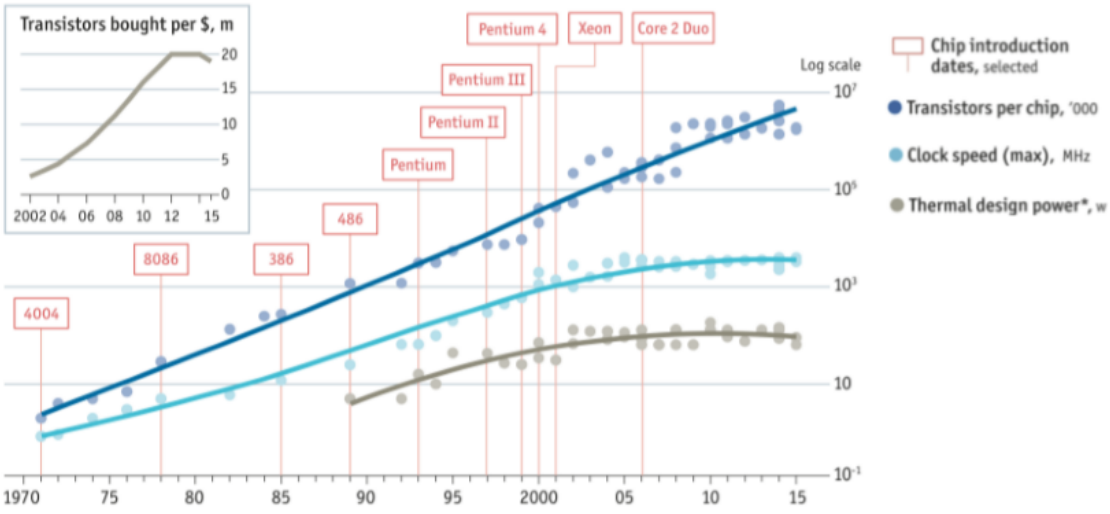


Figure 1.1 Stuttering of transistors per chip, clock speed and thermal design power [2].

Computing devices have improved, and changed modern lives for over 50 years as integrated circuit (IC) semiconductor manufacturing has continuously evolved. The evolution of the density of the number of transistors per single IC, following Moore's law, has doubled the number of transistors on a single IC every 18-24 months [1]. This improvement led computing devices to achieve low cost and high data rate, while shrinking its form-factor.

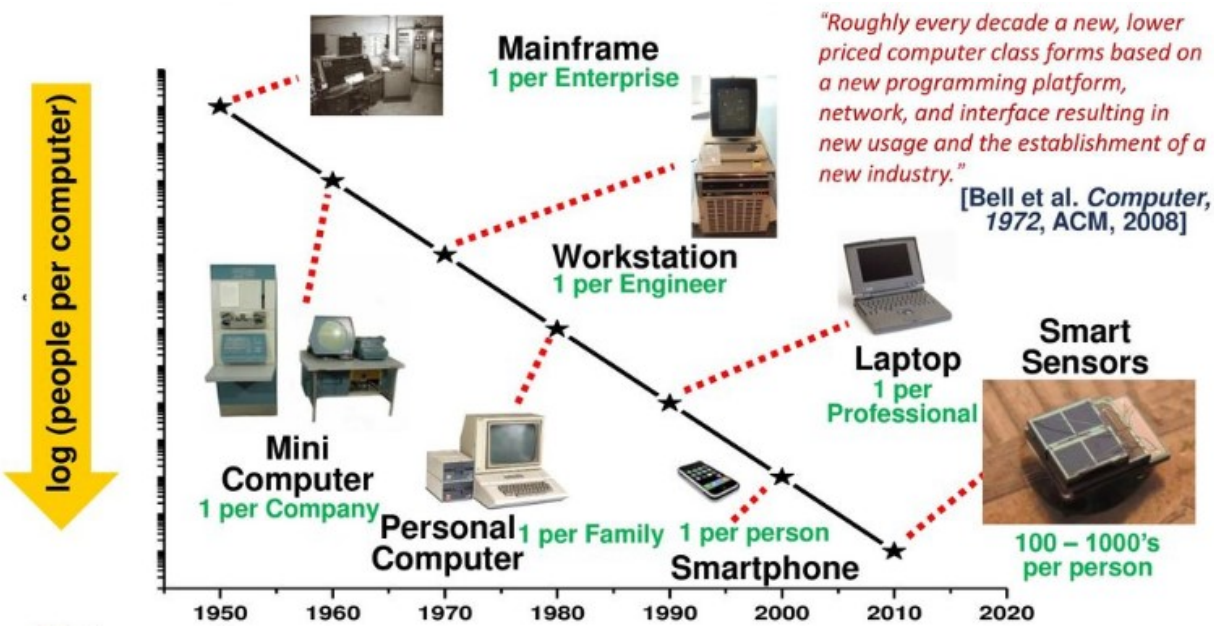


Figure 1.2 Long-Term scaling trend of computing devices over years [3].

Recently, the improvement on scaling of IC manufacturing, however, seems to be slowing down. Smaller transistors are becoming more difficult to fabricate, and the considerable effort for continuing Moore's law accompanies a lot more cost than it used to. As shown in Figure 1.1, however, the value of transistors has saturated, and decreased since 2015 [2]. The maximum tolerable power density in ICs is another issue that limits the speed of clock and amount of computing actions per second. For processors, as the density of the transistor and clock speed increases, the energy dissipated per unit area also increases, which is ultimately restricted by the maximum safe power limit. In addition, the scaling of transistors has no longer been making them more energy-efficient, especially in the analog domain such as power management, clock generation, and RF transceivers. The slowing of fundamental scaling, and its limited improvement seems to be hopeless. However, this has presented an opportunity to improve performance of ICs by expecting significant change and more diverse options in the circuit architectures, systems, and applications software level approaches.

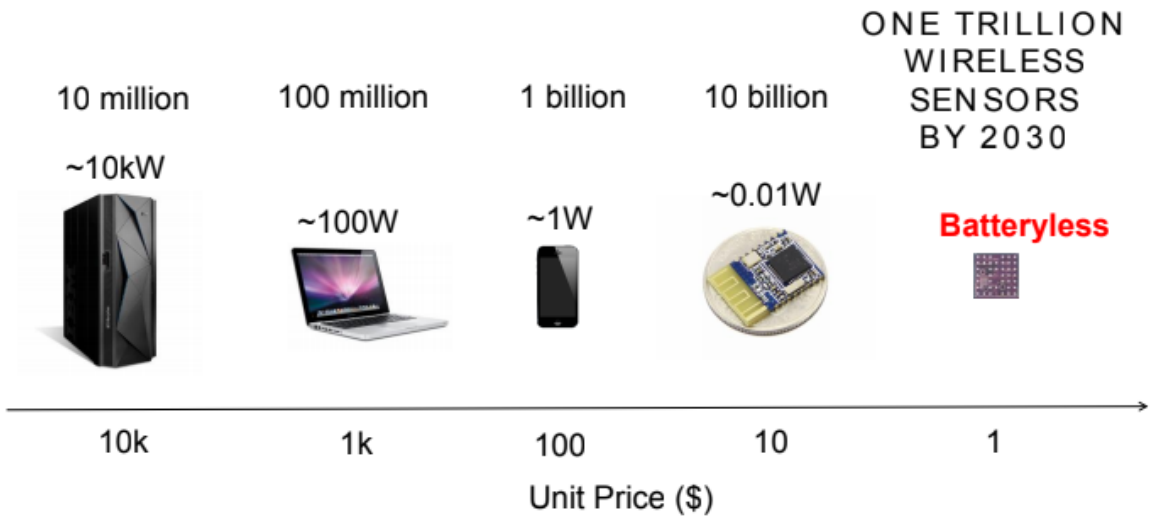


Figure 1.3 Power budgets, and quantities for each type of computing class [4].

According to Bell's Law [1], a new computer class has appeared every decade as a new "minimal" computer by either using lower cost components or a fractional part of the state-of-the-art chips that results in a new platform for a new computing environment. A class may be the consequence and combination of a new platform with a new programming environment, a new network, or new interface with people and/or other information processing systems, where each successive class has had a 100x reduction in physical volume [1], [3], [4]. In Figure 1.2, following the advent of personal computers in 1980s and wireless portable devices such as laptops and smartphones in 1990s and 2000s, wireless sensor networks (WSNs) take center stage as the next trend of computing devices toward more compact, lower cost, more ubiquitous computing [3]. Ubiquitous sensing was projected to reach volumes of 100 sensors per person by 2017, and is currently on a path to reach 10s of Billions of devices in the early 2020s.

Combining the platform, wireless network, and interface into one to integrate with other systems is clearly a new class that are offering wireless deployments, and hence reduced cost for existing applications, such as process, building, home automation, and control. The new class of

WSNs could record the state of a person or object (things such as scales, appliances, switches, thermometers, and thermostats) including its location and physical characteristics using the existing wireless infrastructure for reporting. The successive advent of a new wirelessly connected computing class has been defined as “the Internet of Things (IoT)” in 1999, which is the representative candidate of this new class of computing device [5]. The IoT is an interrelating system of computing devices that involves internet connectivity for each devices ranging from desktop, laptops to non-internet enabled physical devices and everyday objects that are associated with embedded technology. By converging multiple technologies into the system such as sensors, data analysis, and machine learning, the environment is interacting, automatically controlled, or efficiently managed by a control base over the internet. Hence, wireless communication is one of the most crucial factors in IoT devices in order to provide ubiquity. Connected devices are part of a scenario in which every device talks to other related devices in an environment to automate home and industry tasks, and to communicate usable sensor data to users, businesses and other interested parties.

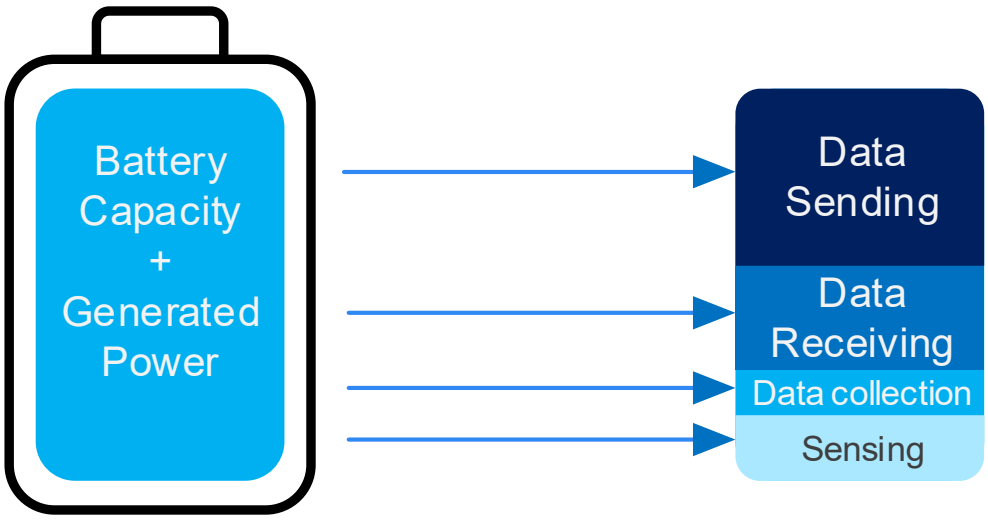


Figure 1.4 Typical energy consumption a low-power IoT device.

As the IoT devices are gradually demanding, and evolving over time, several specification requirements of IoT devices are evolving to enhance its ubiquity. The device has to be low power to sustain its battery life to reduce the concern of battery replacement of each IoT device, especially those in difficult-to-reach locations. The other challenge is integration, or small form factor that reduces the cost of IoT devices by reducing its dependency on external components. State-of-the-art IoT devices require off-chip components, including components that support the power-hungry RF system which typically dominates the form-factor and cost of the IoT device. For sufficient communication range, the radio in the IoT device requires an antenna typically in the range of centimeters. A bulky crystal oscillator for a stable frequency reference is another off-chip component commonly used that dominates the volume of the IoT device. Lastly, the battery typically is the largest portion of the volume of the device.

For the widespread adoption of IoT devices, they have to be compatible with commercial wireless communication protocols such as LPWAN, Zigbee, Bluetooth Low Energy, Cellular, satellite, Wi-Fi, etc [6]. The radio that supports those wireless communication protocols, however, consumes power well beyond 1mW due to the challenging requirements on the circuit performance, which limits the battery life of IoT device. As shown in Figure 1.4, data transmission and reception draws most of the energy from battery than other functions of the low-power IoT device.

IoT radio developers have realized these challenges, and many contributions, and studies have been made to attempt to solve these challenges. The following sections cover the background of state-of-art energy efficient RF systems that addressed, and contributed to solve those challenges.

1.2 Low active power for IoT radios

With the coming of age of the Internet of Things (IoT), demand on ultra-low power (ULP) radios will continue to boost tremendously. Innovations in both the system architecture and circuits implementation are essential for the design of truly ubiquitous receivers for IoT applications. There are several design challenge in radios for IoT applications, including 1) minimize the power consumption with an adequate sensitivity level, 2) operate in a congested frequency spectrum using highly integrated solutions, and 3) maintain compliance with an adopted communication standard [7, 8]. Significant efforts, and studies to minimize active power of radios have been done by several research groups, which has gradually improved the radio performance in a lot of perspectives, especially ranging performance (sensitivity). A survey of ULP radios published in top tier circuits journals and conferences is done to identify the research directions in their design and its limitations

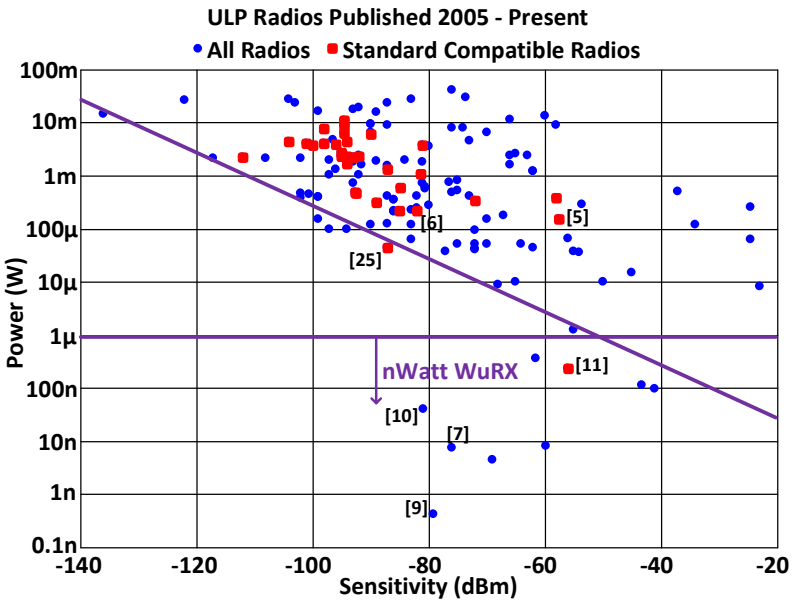


Figure 1.5 Ultra-low power radio survey: sensitivity vs. power for coherent and non-coherent modulation.

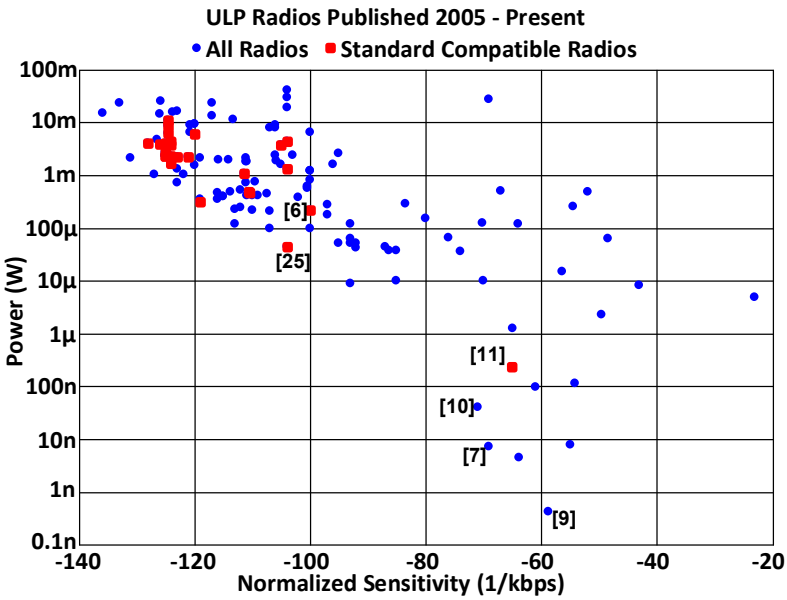


Figure 1.6 Ultra-low power radio survey: normalized sensitivity vs. power.

[9]. Figure 1.5 shows the power vs sensitivity (range) trade-off for the recent 179 published ULP receivers. With the exception of nanowatt wake-up radios, an empirical line with a slope of ½ bounds the performance. This implies the power will increase by a factor of 10 for a 10x increase in the receiver range (assuming a path-loss coefficient of 2). When the sensitivity is normalized to the data rate (Figure 1.6), however, the power vs sensitivity trade-off becomes more settled since nanowatt radios have relatively low data rates. In both figures, standard compliant radios clearly tend to be higher power. This is expected since most standards nowadays have stringent requirements on sensitivity, interference rejection and frequency accuracy. To achieve these specifications, high power receiver blocks might become required such as LNAs, active filters with sharp frequency response, and phase locked loops (PLLs) with accurate crystal frequency references.

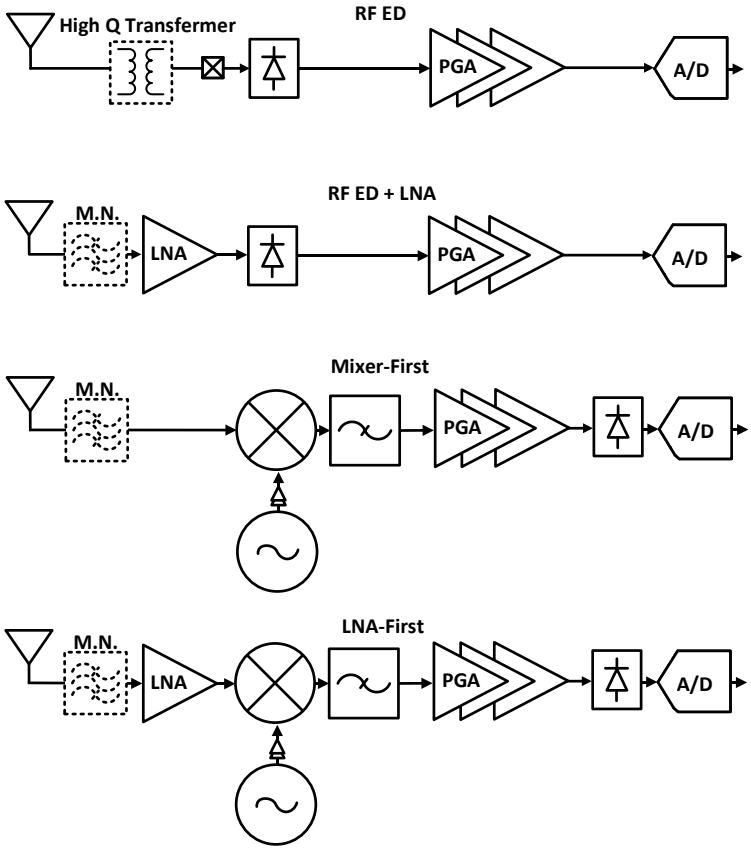


Figure 1.7 Low power radio architectures.

The modulation scheme plays an important role in the specifications of the radio and hence its power consumption [10]. Unlike non-coherent modulation such as OOK, FSK modulation, coherent communication requires significantly higher power to demodulate because the carrier phase is needed for coherent detection which necessitates using a PLL in the receiver.

The following sections are related to low power design trends that are observed in recent publications.

1.2.1 Nanowatt wake-up radios:

By utilizing an all passive RF front-end, the RX power can be reduced significantly to the nanowatt level. This is achieved using an RF envelope detector to convert the incoming signal to DC (Figure 1.7). However, an RF envelope detector has a large bandwidth which limits the sensitivity of such architecture to typically less than -60 dBm [11] due to the high noise bandwidth. The sensitivity can be further improved by ~ 20dB by using a high Q transformer at the front-end which provides passive gain and filtering [12, 13] (Figure 1.7). The Q factor of the off-chip matching network can be also limited as the center frequency of the system goes above the sub-GHz range. With this architecture, the integrated interference mitigation techniques used are mostly limited to continuous wave interferes (CW) which can be characterized as an additional DC offset for the comparator [14]. This assumption is not valid for all wireless channels since they experience some level of signal fading which makes these techniques less effective in a real environment. Another limitation of this architecture is it does not support high frequencies due to the large shunt capacitance in RF detectors. Figure 1.8 shows that

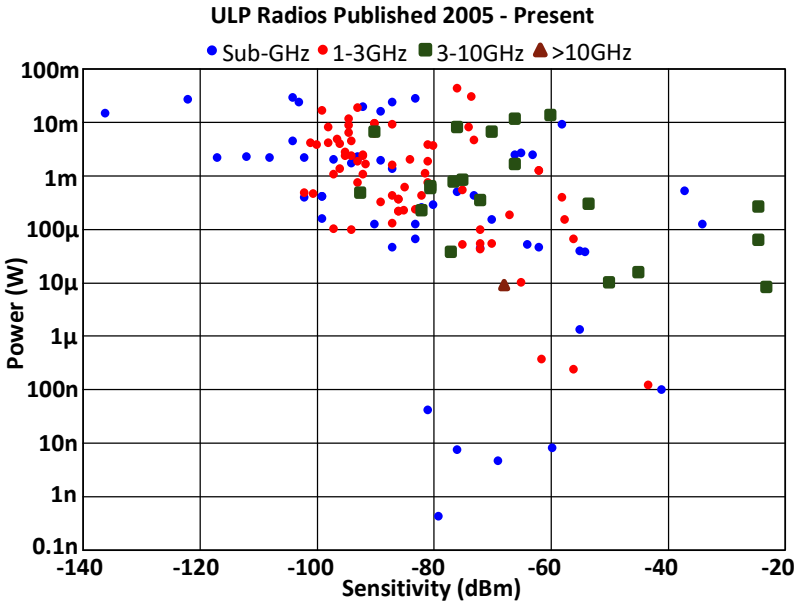


Figure 1.8 Low power radio survey: sensitivity vs. power at different frequency regimes.

all radios consuming less than 10 μW operate at a frequency lower than 3 GHz. Sub-threshold analog and digital logic are common to achieve sub 1-μW power levels [11]. For very low data rates, a bit level duty cycled have been reported [14]. This allows for improved sensitivity levels with low average power using duty cycling.

1.2.2 Mixer-first radios for selectivity:

Another design trend to save power is to avoid using active RF gain (LNA) while using a mixer as a first stage instead [15, 16, 17] (Figure 1.7). Since the first RX stage dominates its noise performance, mixer-first radios suffer from higher noise figure (NF), when optimized for low power consumption, which degrades their sensitivity (range). Nevertheless, this architecture can still achieve decent selectivity levels with a sub-mW power budget [18]. In so-called mixer-first receivers, the dominant block in terms of power consumption is the local oscillator and its buffers. In order to reduce the LO power, the conventional LC oscillator can be replaced with a ring oscillator (RO) especially in more advanced CMOS nodes [19]. However, ROs have worse frequency stability making it harder to design the radio without a significant performance degradation in its sensitivity and/or selectivity [20]. Alternatively, an LC oscillator can have its inductor off-chip to overcome the limited quality factor for on-chip inductors resulting in a significant power reduction by up to 75% compared with fully on-chip LC oscillators [21]. Although these off-chip inductors can be found in very small form factors, it is not a fully integrated solution, which might not suit some IoT applications.

1.2.3 LNA-first radios for long range:

Long range applications require sensitivity levels beyond -100dBm. To achieve this, a LNA-first topology is usually used. Similar to RF ED based wake-up radios; bit-level duty cycling was applied also in LNA first radios [22] to reduce the average power. In addition, lower supply voltages have been used to improve the power efficiency of LNAs [23]. In [24], a low voltage quadrature LNA was adopted in a current-reuse topology resulting in a power consumption of 600μW for the RF front-end, transimpedance amplifier and baseband filter.

1.3 Widely Adoptable RF Wireless Systems for IoT

1.3.1 Ubiquitous wireless communication protocols for IoT devices

Given the clear power and performance trade-off discussed in the previous section, one of the challenges in ULP design is to still be able to communicate through an existing adopted standard. Several types of approach have been done that helps low-power IoT devices communicate with existing standards that maximizes the widespread adoption. The most common network protocols adopted by IoT devices will be covered briefly in next several paragraphs, such as BLE, WiFi, NB-IoT, LTE-M, and LPWAN.

Bluetooth Low Energy (BLE) is one of the most promising low power consumption wireless technologies for IoT applications. Everything from physical design to use models is designed to keep power consumption at a minimum. But to further reduce power consumption, a BLE device can be kept in sleep mode most of the time, but when an event occurs, the device will wake up and a short message will be transferred to a gateway, PC or smartphone. Ultimately, the active power consumption

	Frequency Band	Data Rate (kbps)	Range	Latency	Power
WiFi	2400,5000	54000,450000	Short	Fast	High
BLE, BT 5.0	2400	1000,2000	Short	Medium	Low
NB-IoT/LTE-M	700,850,1700	200	Long	Slow	High
LPWAN	915	50	Long	Slow	Medium

Table 1.1 Specifications of wireless network protocols for IoT applications.

is reduced to a tenth of the energy consumption of classic Bluetooth. In low duty cycle applications, a button cell battery could provide up to a year of power.

WiFi (IEEE 802.11) is one of a most ubiquitous wireless network protocols for users due to its high data-rate, and large deployment of WiFi routers (access points). Simplicity of the network compared to cellular networks is another benefit that attracts many IoT applications. The WiFi radios, however, limits potential of adoption in ULP applications due to its excessive power due to strict requirements of the system. For this limitation, a new version of the 802.11 protocol is in development from the 802.11ba task group (TG) that can save energy while the WiFi device is asleep [25].

NB-IoT and LTE-M are new cellular network protocols for IoT applications that in some aspects reuses technical components from LTE to facilitate operation within an LTE carrier [26]. The entirety of those protocols is operable in a narrow spectrum, providing unprecedented deployment flexibility because of the minimal spectrum requirements. Those network protocols have benefits on widespread adoption because it is operable within the LTE network protocol which was introduced in 2008 and is now pervasive. The NB-IoT compliant radios are used to send and receive messages over long distances (> 10km maximum), extending the target link budget of 164dB by using data repetition. The NB-IoT network is focused on very low data rates that is ideal for simpler static sensor applications. The LTE-M is very similar to NB-IoT because it also branched out from the LTE standard.

The LTE-M network has wider bandwidth, thus, higher data rate is supported compared to NB-IoT devices. The power consumption of those network protocols, however, are excessive compared to LPWAN, or BLE, again due to its network complexity.

A low-power wide-area network (LPWAN) is a wireless network protocol for very long range communications at low data-rate that is utilized in IoT applications [27]. The radio has less power consumption than cellular IoT radios with hardware simplicity that leads to a low power, low cost system. The network protocol, however, has higher latency and less frequent data transfer than cellular IoT network protocols. These networks are relatively new, and therefore not widely deployed as of today, which limits the widespread adoption.

The surge of connected devices clearly points out that any system which computes, senses, and/or interacts will eventually have connectivity. Although this can be easily achieved in today's technology due to the advancements in the integrated radios, seamless connectivity still remains a big problem in various low-power applications. Always ON, always connected operation is not feasible in almost all battery constrained systems even when low-power protocols such as Bluetooth low energy (BLE) or ZigBee are utilized. This issue becomes drastically challenging, especially for applications in which sparse data traffic is observed over an unscheduled protocol (such as WiFi). Event-driven radios such as ultra-low power (ULP) wake-up receivers (WRXs) have been playing an essential role as a solution to seamless connectivity in the aforementioned applications by providing low latency and low power operation simultaneously.

1.3.2 High specification requirements (sensitivity, interference rejection)

RF interference will increase since the limited bandwidth is shared with a rapidly growing number of IoT devices using multiple heterogeneous wireless communication standards. Integrated

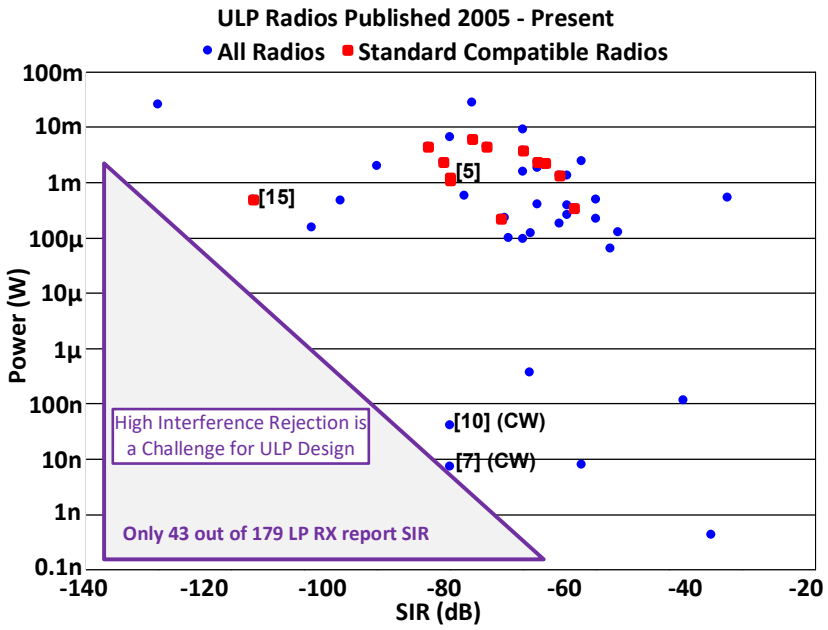


Figure 1.9 Ultra-low power radio survey: SIR vs. power.

solutions for interference rejection pose a real challenge in ULP radio design since they typically require high power and will increase the receiver total power significantly, especially with narrowband channels [28, 10]. The signal to interference rejection (SIR) performance of ULP receivers is shown in Figure 1.9. The trade-off can be clearly observed where only a few standard complaint ULP radios report their selectivity performance, and they consume at least 100s of µWatts. This can be attributed to the active filtering requiring high power to synthesize a high Q filter response, which is done traditionally by cascading multiple active filter stages. On the other hand, off chip passive filtering is possible but leads to lower system integration, therefore, increases cost. For example in [29, 14], off-chip RF MEMS are used to enhance the selectivity performance of the radio.

One possible solution for power reduction with less dependence on off-chip components is a companion radio that is used to listen for wake-up messages, and enables the main radio when it receives a packet from the desired channel. There are unwanted cases that the companion radio triggers

a false alarm. The channel for wake-up is often in an unlicensed ISM band, and usually surrounded by incumbent radios. Without sufficient channel rejection, those interferers can saturate the companion radio system and impact its operation.

1.4 Fully Integrated RF Systems

1.4.1 Minimizing off-chip components

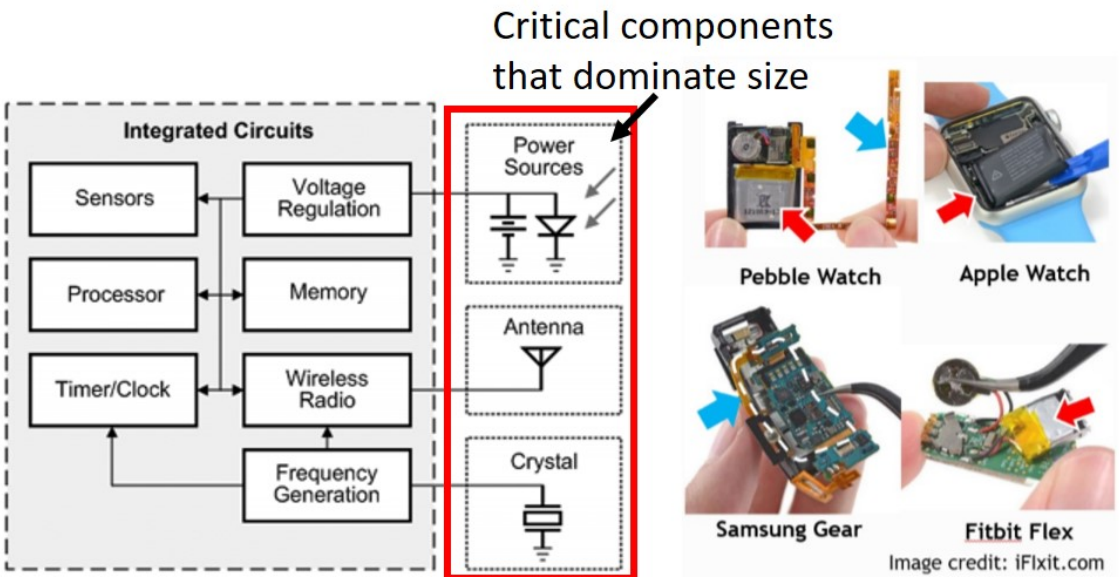


Figure 1.10 Block diagram of a typical WSN node [68].

In recent years the efficient design of a wireless sensor network has become a leading area of research. A wireless sensor network can be defined as a network of devices that can communicate the information gathered from a monitored field through wireless links. The data is forwarded through multiple nodes, and with a gateway, the data is connected to other networks like the internet [30]. A wireless sensor network consists of base stations and a number of wireless sensor nodes (WSNs). These networks are used to monitor physical or environmental conditions like sound, pressure, temperature

and co-operatively pass data through the network to a main location. Today's wireless sensors are composed of multiple components such as a microcontroller, power management, sensor, transceiver, timer/clock, battery, and antenna. These components tend to be commercial off-the-shelf (COTS) components, which could be bought individually then put together on a printed circuit board in Figure 1.10. It has a great advantage that it can afford a designer flexibility, but doesn't look like the new class of computers in future sensor nodes. In most of these applications, the bulky battery takes up a significant fraction of the total volume and the antenna for the radio sticks out several centimeters. The result is this system increases up to centimeters or tens of centimeters in at least one dimension. Due to these problems, the integration of the battery and antenna are two major issues for realizing the integrated cubic mm-scale wireless sensor nodes.

1.4.2 Antenna-on-Chip (AoC)

At low RF frequency (<10GHz), a several-cm antenna is required for good radiation efficiency, which is difficult to integrate on-chip. At high frequencies around 60 GHz, however, the electrical wavelength is on the mm-scale which allows the integration of the antenna on the chip. Recently, the wireless communications community has become increasingly interested in the unlicensed 60-GHz band where there is 9GHz of unlicensed spectrum available. The IEEE 802.15.3c Wireless personal area networks (WPANs) standard, which requires high data-rate and low-cost chipsets for wireless short-range communications, has been advancing technologies in this frequency band since 2003 [31]. The scaling down of transistors pushes up the high-frequency capability of the active devices in a complementary metal oxide semiconductor (CMOS) technology, which has made supporting the 60-GHz band in CMOS possible. However, the implementation of Antenna-on-Chip (AoC) has been challenging because the antenna structure should be a reasonable size compared to the wavelength of

the RF field and can be integrated with the circuitry. Reducing the size below the natural resonant length could cause low efficiency. In addition, there are still many issues to consider in CMOS manufacturing such as routing, density rule, keep-out areas, coupling with the actives.

1.4.3 Reference-less, and on-chip reference

For general wireless systems, a timing device generates a reference signal that oscillates at a constant, stable frequency with low jitter. They mainly consist of a resonating element providing an oscillating output with a specific frequency, either electrically or mechanically. Their ability to maintain a determined frequency in a specified period of time is the most important parameter limiting their implementation [4, 32]. As a resonate device, a quartz-crystal and a ceramic are well-known as mechanical resonators. The mechanical resonator has higher stability of the oscillation frequency than the electric resonator because it is much less affected by external circuits or by perturbation of the supply. A drawback of the mechanical resonator is its incompatibility with CMOS processes so that the resonator has to be off-chip component of the system. As its dimension shrinks to the microscale, most mechanical resonators exhibit nonlinearities that considerably degrade the frequency stability of the oscillator. On the other hand, the electrical resonator can be used in monolithic integration in a CMOS process, but the RC and LC resonator in CMOS has relatively Low-Q, and vulnerable to

Oscillator Type	Frequency	Stability	Power	Area
Quartz-crystal Osc.	52 MHz	5 ppm	6 mW	5.0 mm^2
Ceramix Osc.	30-280 MHz	50 ppm	40 mW	35 mm^2
MEMS Osc.	1-150 MHz	50 ppm	9 mW	5.0 mm^2
Saw based Osc.	315-1000 MHz	150 ppm	66 mW	37.5 mm^2

Table 1.2 Comparison table of the state-of-the-art timing devices.

environment such as voltage supply and process variations that could lead to instability and frequency offset. For many wireless sensor network applications, maintaining accurate time information is crucial. This requires an accurate timing reference. For the wireless sensor nodes (~ cm-scale) in the un-licensed bands below 60-GHz, the mechanical resonators such as a quartz-crystal [33], ceramic [34], MEMS [35] or saw-filter [36] have been used widely as frequency references. However, when it comes to mm-scale wireless sensor nodes (WSNs), the dimension of the timing devices is no longer relatively small compared to the integrated antenna and micro-battery. The mechanical OSC also requires high power consumption and cannot be integrated in a standard CMOS technology. The performance comparison table of the state-of-the-art timing devices is shown in Table 1.2.

Wireless systems with no off-chip timing reference have the potential to reduce the overall form-factor and cost, which benefits various applications that are area limited, such as medical applications.

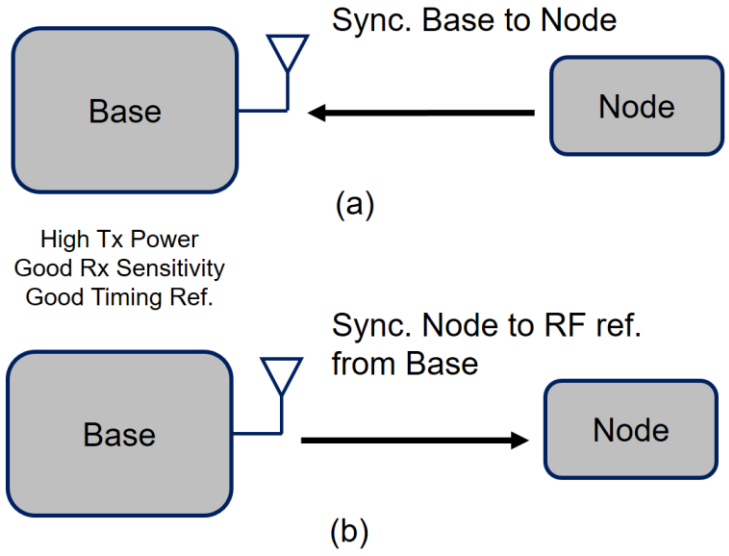


Figure 1.11 (a) Adaptive node-initiation synchronization communication [37]. (b) Adaptive base-initiation synchronization communication [38].

Recently, several reference-less RF radios were proposed that synchronize their carrier frequency to the reference on the air that is transmitted from a base station. Those radios can talk based on two different ways: 1) lock its frequency to the base station that takes the burden of clock accuracy, frequency reference [37]; 2) Transmit the signal from the node, and make the base station adapt frequency and timing based on received RF data [38]. This second approach can be beneficial for IoT devices because it doesn't need to rely on an off-chip crystal. However, the radio always has to talk with the base station that has a very accurate timing reference. Node-to-node communication without a reference clock is still a big challenge for IoT radios.

1.5 Dissertation Contribution and Organization

As explained in the previous section, the hard constraint on the evolution of the new class of IoT devices is closely related to RF systems, and radios in IoT devices. My research covers several endeavors for relieving energy constraints on RF systems by utilizing existing network protocols that eventually meets both low-active power, and widespread adoption. This includes novel approaches on 802.11 communication with articulate iterations on low-power RF systems. Also, my research contributes to relieve integration challenge by associating with small form-factor mm^3-scale WSN that doesn't rely on crystal reference, and external antenna. The detail contributions are described as follows:

1.5.1 A Sub-mW WiFi Back-Channel Receiver for Widespread Adoption on Ultra-Low Power IoT Radios

This work contributes to two different aspects to bridge the gap between ultra-low power custom radios, and standard compliant radios. The novel approach in Wi-Fi communication systems reduces the power budget significantly when no active Wi-Fi network connection is present, while always listening for the presence of a Wi-Fi router. A novel energy-efficient low-power down conversion RF front-end for back-channel communication reduces the active power of the proposed receiver further.

An ULP receiver for WiFi back-channel signals embedded in 5.8GHz IEEE 802.11a Wi-Fi OFDM packets has been demonstrated that enables extremely energy-efficient WiFi communication system without changing the firmware of the existing 802.11 routers. The back-channel receiver receives binary FSK modulated wideband signal from 802.11 transmitter that is been modulated by crafted data stream. The proposed back-channel receiver architecture employs a two-step down-conversion where the first mixing stage utilizes the 3rd harmonic of the LO for power efficiency. The radio uses an off-chip SAW filter, balun and a 250kHz reference crystal as external components. The receiver consumes 335µW with a sensitivity of -72dBm at a BER of 10^{-3} and data-rate of 31.25kb/s.

1.5.2 A Fully Integrated Energy-Efficient Ring-VCO Based 3rd-Harmonic Receiver for IEEE 802.11ba

This work demonstrates a Wi-Fi wake-up receiver with the best power vs. sensitivity trade-off designed for the new low-power 802.11ba standard. The power consumption of the RF front-end is optimized by removing active RF gain stages, and using a novel non-edge combining, 3rd harmonic passive mixer with a ring-based LO operating at 1/3 the RF frequency, while rejecting unwanted harmonics spurs by more than 37dB.

A 40 nm CMOS IEEE 802.11ba low-power wake-up receiver (LP-WUR) is presented. It receives 802.11ba messages generated by an 802.11 orthogonal frequency-division multiplexing (OFDM) transmitter operating at 5.8 GHz. The noise figure of the receiver is 14 dB, taking advantage of a 1:3 transformer that provides passive voltage gain in front of the high switch loss mixer-first RF front-end, and matching across 5.5-5.8 GHz with <-12 dB S11. The receiver achieves a sensitivity of -83 dBm and -20 dB adjacent channel signal-to-interference ratio (SIR) while consuming 220 μW at a bit-error-rate (BER) of 10-3 and data-rate of 62.5 kb/s, which shows the best sensitivity-power trade-off among >3 GHz receivers.

1.5.3 A Stand-Alone Ultra-Low Voltage, Low Power 802.11ba LP-WUR with Enhanced Ranging, and Interference Rejection for MELs Power Reduction SoC

A stand alone, fully integrated 0.2V 578μW ultra-low voltage (ULV) 2.4GHz 802.11ba WiFi wake-up receiver (WRX) is presented. This work contributes to energy-efficient, extremely low-voltage WRX system design without any external dependency except reference clock. The WRX includes a current-efficient ULV noise cancelling LNA with high turn step-up transformer, and Q-enhanced RF gain stages for low noise figure. For minimizing the current load on the micro-power manager, the 1/3 RF mixer, and ULV FLL are implemented. It achieves -91.5dBm sensitivity at 10-3 BER and data-rate of 62.5kbps, while rejecting 45dB of adjacent blocker with only 0.2V supply. From system integration measurement, the WRX includes an energy-efficient 5ms startup sequence which interfaces to an external node controller. The WRX eventually contributes to the ULP SoC for MELs energy reduction that saves energy loss from Watt-level to micro-Watt-level with availability of

wireless managing through WiFi network protocols, with enhanced channel-rejection, and ranging vs. power trade-off.

1.5.4 A Fully integrated 62-69GHz Reference-Less Multi-Channel Transceiver for Small Form-Factor System with Dual-Mode Slot Loop Antenna and On-Chip T-Line Reference based FLL

This work contributes to extremely small form factor, low-cost WSNs by using a physical characteristics of a T-line resonator on-chip, which removes the need for an external timing reference on the WSN. With recent advanced CMOS technology, and an articulated mixed signal structure, the on-chip frequency reference provides <0.5% chip-to-chip frequency accuracy, while providing multiple channel across a 60GHz wireless personal area network (WPAN) band.

A fully integrated 62-69GHz reference-less transceiver (TRx) is presented for low-cost, small form factor system that supports dense wireless environment without bulky external reference, and provide potential on wireless node-to-node communication. On-chip T-line resonator based frequency locked loop (FLL) helps the system lock to the desired frequency band with 4325ppm chip-to-chip variation, supports non-overlapping 12-channel on GSM band, with 580MHz spacing. The high efficient on-chip slot antenna supports transmission, and reception mode on same antenna with isolation of 38dB. The transceiver consumes 20mW standby power while supporting NF of 10dB, and sensitivity of -71dBm. The T-line resonator, and slot-loop antenna utilizes ground plane placed on top of the baseband circuitries that saves a large portion of active area. The whole TRx system is integrated in 2.5mm^2 CMOS die.

Chapter 2 A 335µW -72dBm Receiver for FSK Back-Channel Embedded in 5.8GHz Wi-Fi OFDM Packets

2.1 Introduction

WI-FI is the most ubiquitous wireless network protocol, however, its adoption into ultra-low power (ULP) internet-of-thing (IoT) devices has been limited because of the high active power consumption (>100 mW) of Wi-Fi radios. Even with heavy duty cycling of the 802.11 radio, the

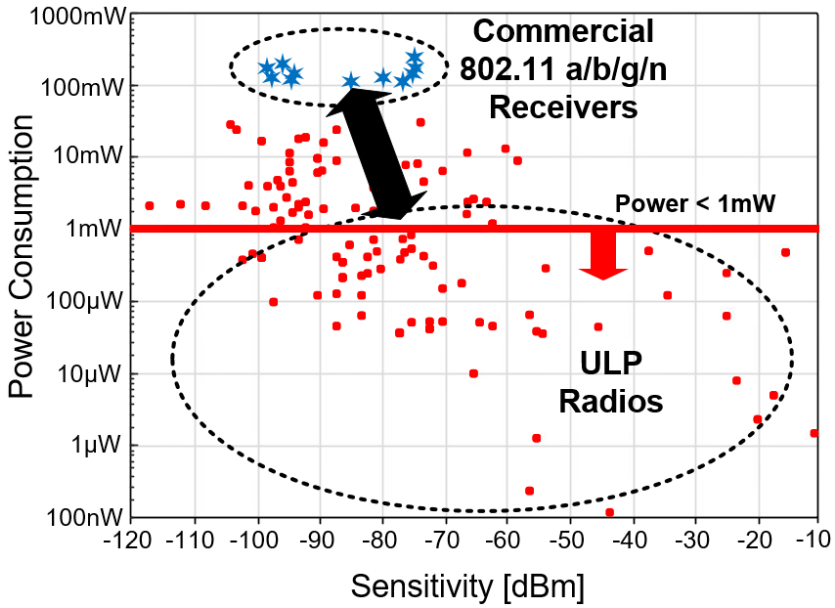


Figure 2.1 ULP radio survey from 2005 to present. Red data points of the radio survey are from top conferences (ISSCC, VLSI, RFIC, CICC) and commercial TRx chips. The blue stars are reported performance of commercial 802.11 a/b/g/n radios.

average power is still too high for most ULP IoT applications, and the startup energy often too great to make networking and latencies practical at ULP levels.

As shown in Figure 2.1, many custom ULP wake-up receivers have been proposed which operate well below 1 mW. In particular, ULP receivers that operate <100 μW, with sensitivities better than -80 dBm have been demonstrated [39, 40, 41]. Moreover, several local oscillator (LO)-less, sub-μW, <-60 dBm ULP receivers have been reported [42, 12]. While this last category of ULP receivers offers the best sensitivity-power tradeoff, one drawback of these LO-less receivers is they tend to suffer from poor channel selectivity, [39, 42, 12]. The common disadvantage shared by all of these ULP receivers is they are not compliant with any Wi-Fi standard, and therefore cannot take advantage of the ubiquity of Wi-Fi networks.

In this Chapter, we present a 335μW ULP receiver that demodulates wideband FSK back-channel messages that are embedded in standard-compliant 802.11a packets. On Wi-Fi transmitters, generating back-channel messages only requires control of the payload data without any hardware or firmware modification [43]. Therefore, back-channel message transmission is supported by any IEEE 802.11a or later legacy Wi-Fi devices that are already deployed. By using carefully crafted bit sequences in the payload of a Wi-Fi packet, we produce a wideband, binary FSK-modulated back-channel message via intentional unequal power allocation on the OFDM subcarriers. The ULP receiver then demodulates the FSK modulated back-channel message [43] by detecting power differences in two non-overlapping sets of OFDM subcarriers. Unlike conventional narrowband FSK schemes, the wideband property of the Wi-Fi back-channel FSK allows significantly relaxed specifications of the ULP receiver on phase distortion, order of the filter, and inter-modulation. This enables realizing ULP Wi-Fi back-channel receivers whose power consumption is significantly lower than that of a conventional FSK system.

Figure 2.2 shows an application of ULP Wi-Fi back-channel receiver that can be used as a Wi-Fi wake-up receiver. When the IoT device is out of network, only ULP back-channel receiver is active which tries receiving wake-up message from the Wi-Fi transmitter. As the receiver receive a back-channel wake-up message from 802.11 router, enable the main Wi-Fi radio, and turn-off the ULP back-channel receiver. By only enabling main Wi-Fi radio in the IoT device when the wake-up radio received wake-up message from Wi-Fi transmitter, active power consumption can be reduced substantially, while keeping low latency enabling Wi-Fi network.

Detail information of Wi-Fi back-channel FSK modulation, and its signal generation will be covered in Section II. 3rd harmonic mixing, which substantially reduces the overall power consumption, phase noise analysis for wideband demodulation, and detail circuit architecture of each demodulation steps will be covered in Section III. Finally, measured results will be covered in Section IV.

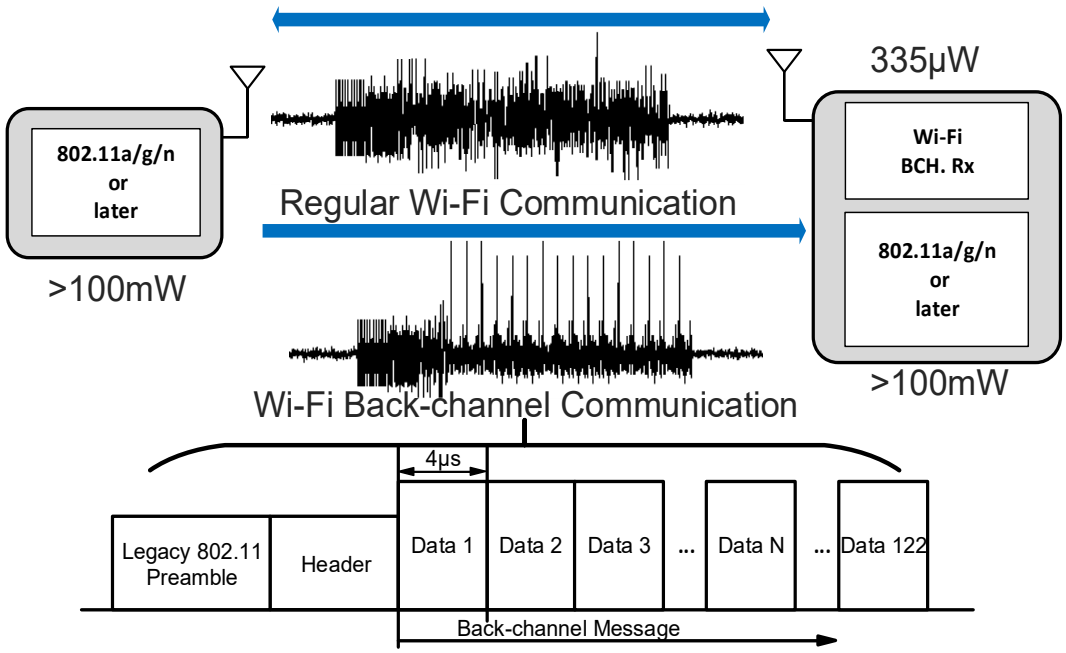


Figure 2.2 Application of ULP Wi-Fi back-channel radio.

2.2 Wi-Fi Back-Channel (De)Modulation

Since 802.11a in 1999, Wi-Fi standards have used OFDM because it has numerous advantages for high throughput devices. The power consumption of wideband OFDM mod/demod, however, is not suitable for ULP radios because it requires high-speed ADC/DAC, and significant baseband processing. Especially, OFDM receiver requires a high performance linear RF front-end to avoid intermodulation due to uncorrelated noisy like wideband signal that has high peak-to-average power ratio (PAPR). OFDM transmitters are basically capable of generating a wide range of RF signals, by taking a time-domain signals' FFT and mapping that to each of the OFDM sub-carriers.

By feeding carefully crafted bit sequences into the payload of a Wi-Fi packet, the Wi-Fi OFDM transmitter is made to produce a wideband back-channel FSK signal embedded in a 5.8GHz IEEE 802.11a compliant OFDM packet. Defining M subsets of subcarrier indices that is not overlapped to each subset, a back-channel M-ary wideband FSK signal can be generated by

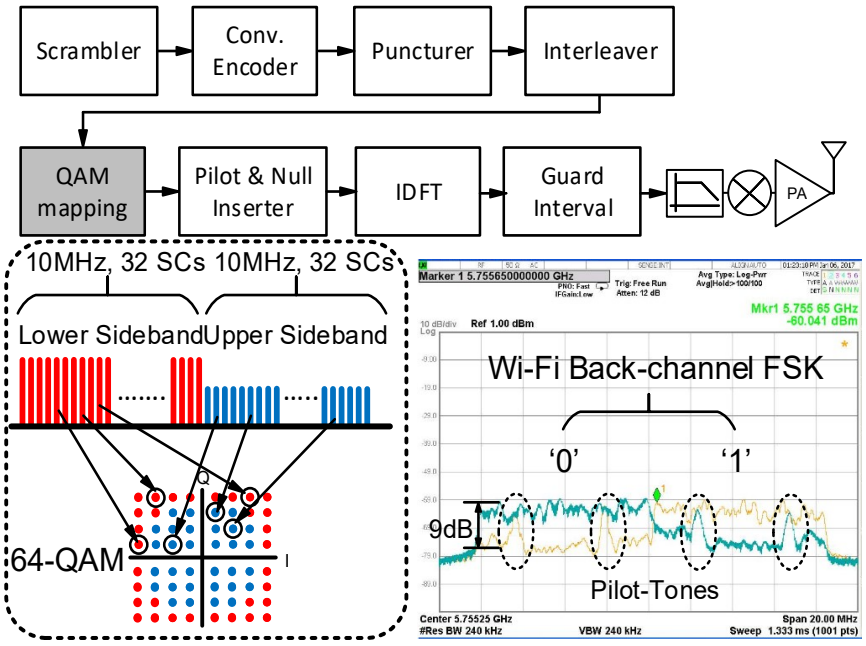


Figure 2.3 binary-FSK Wi-Fi back-channel modulation data-path.

allocating high power to one out of M subsets. The back-channel modulation, however, faces a challenge because it needs to comply strict constraint of the standard compliant packet structure, so that it requires an algorithm for FSK back-channel modulation scheme [43]. To relieve the complexity of the algorithm, and receiver design, binary-FSK scheme is chosen. The binary-FSK modulated back-channel occupies the same 20MHz bandwidth, and each binary back-channel message bit is conveyed by one OFDM symbol (4μs long). This is achieved by mapping only low-power constellation points the lower half of the channel, and high-power point to the upper half to encode a '0' (and vice versa for a '1') (Figure 2.3). Thus, the back-channel bit is demodulated by comparing the energy in the upper and lower halves of the Wi-Fi channel. As shown in Figure 2.3, the average power difference between each sideband introduced by FSK back-channel modulation is around 9dB, and each of the side band contains two-pilot tones, which is inserted in the Wi-Fi data-path. The max back-channel bit rate is identical to the Wi-Fi OFDM symbol rate, which is 250kHz (i.e., 4μs per back-channel bit). One can consider this as a spread spectrum scheme where 250kb/s binary FSK is spread over a 20MHz bandwidth. This simple non-coherent demodulation mechanism combined with a relatively low symbol rate allows an ULP implementation of a Wi-Fi back-channel receiver, as a companion wakeup radio to a fully compliant Wi-Fi radio. The wide bandwidth of the FSK back-channel symbols also makes the receiver relatively insensitive to phase noise and frequency offset in the LO, further reducing power.

2.3 Low Power RF Receiver Circuit Design

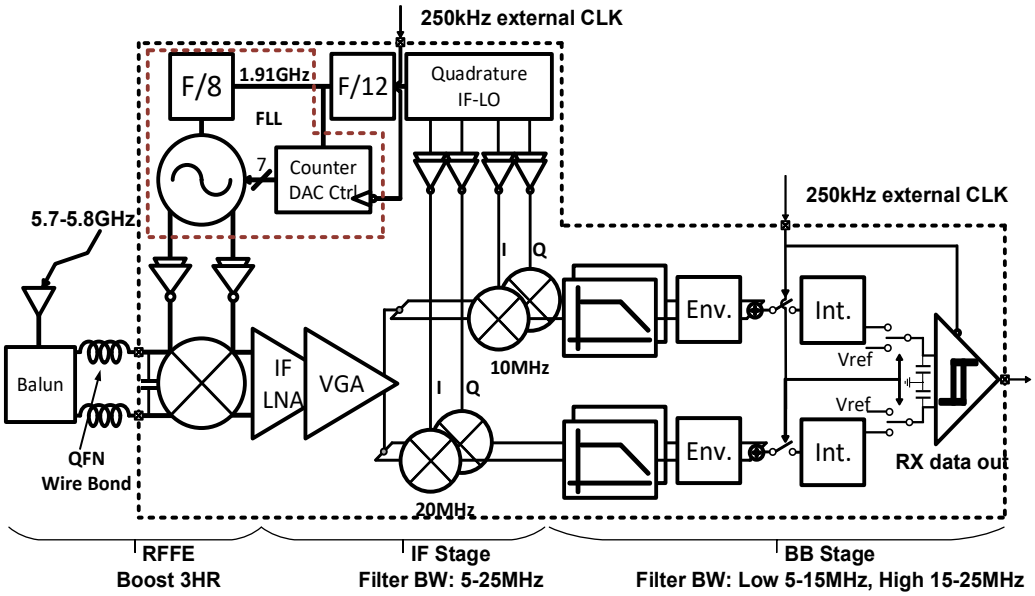


Figure 2.4 System block diagram of the ULP Wi-Fi back-channel receiver.

The goal of this implementation was designing a receiver with minimized power consumption, while receiving a back-channel signal with comparable link budget of existing 802.11 receivers which are around -70dBm when receiving its maximum data-rate. assuming a 1/d2 path loss, with a transmission power of the Wi-Fi router of 20dBm, a -70dBm 5.8GHz ULP radio can reach up to 30m. Figure 2.4 shows the receiver which is a passive mixer-first architecture and a 2-step down-conversion which help to reduce power, at the expense of increased noise factor. Aided by off-chip high-Q RF filter, the receiver can behave as a sliding-IF receiver. Also, the receiver down-converts the RF signal with an LO at 1/3 the RF frequency for power efficiency. The main power saving features of the design are 1) back-channel messages modulate information onto wideband FSK symbols transmitted by a standard Wi-Fi radio, which are detectable by ULP receivers; 2) the RF mixer down-converts 5.8GHz as the 3rd harmonic term from a commutating mixer switching at 1.9GHz. Because all LO paths switch at 1.9GHz, this significantly reduces power of the oscillator, LO buffers, and divider in the FLL, which are often the highest power blocks in an ULP radio; 3) low-noise amplification, filtering, and variable gain amplification is

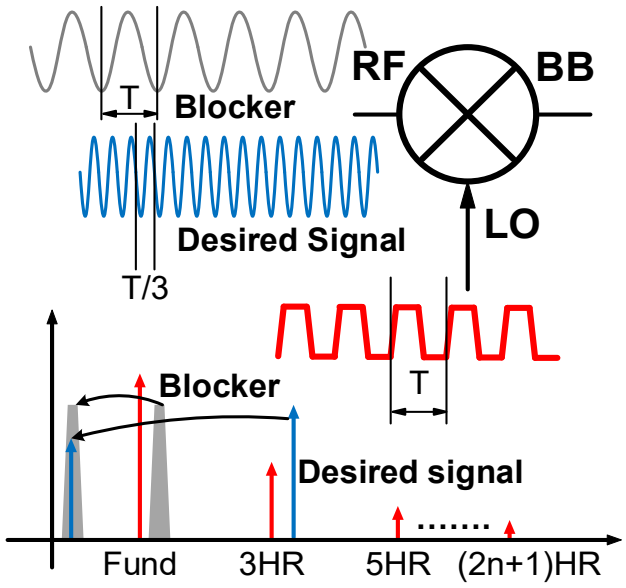


Figure 2.5 Blocker issue of the 3rd harmonics mixing.

performed at the first intermediate frequency (IF1); and 4) the IF1 signal is further down-converted by 2nd quadrature mixers (IF2 Mixer), whose LO is driven from the FLL, which separates the upper and lower halves of the back-channel FSK into two wideband energy-detection paths. The baseband circuits filter each half of the Wi-Fi channel, envelop detect and integrate them to measure and compare the energy in the low and high halves to make a bit decision.

2.3.1 RF Front-end

As shown in Figure 2.6, the RF front end is comprised of an off-chip balun, RF off-chip filter, and an on-chip double-balanced passive mixer. The capacitive in put impedance requires matching, and the series inductor induced by the wire-bond inside the QFN package provides some voltage boost at the resonant peak with some on-chip cap tuning at the RF input. The resonant LC tank on the RF front-end is not only providing voltage gain, but also filters out other harmonic components. To reduce the blocker issue that comes from the interferer whose operation frequency is close to fundamental mixing frequency, off-chip RF filter is cascaded before the off-chip balun,

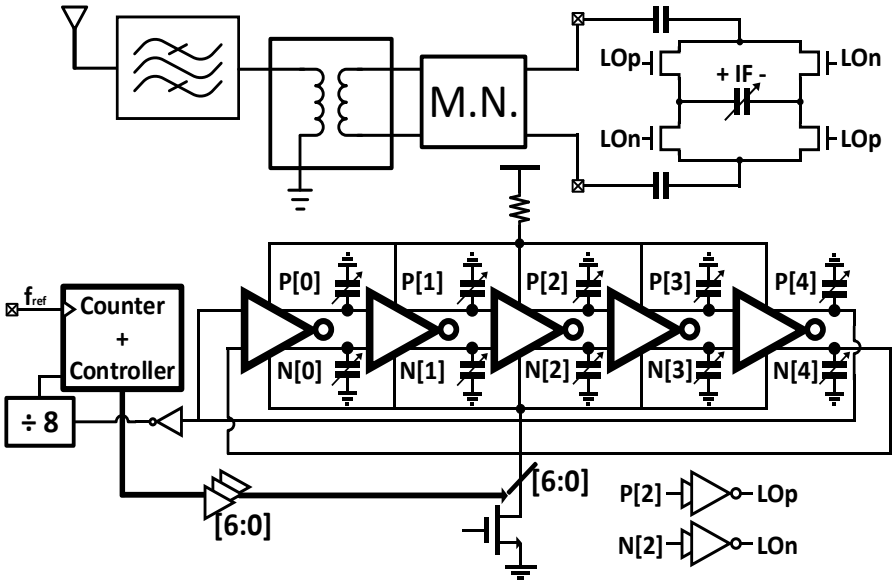


Figure 2.6 Circuit implementation of RF front-end (top), and FLL (bottom).

which eventually rejects the fundamental interferer more than 20dB. The filtered RF signal is fed into the dual balanced RF mixer whose gate potential is biased to maximize the conversion gain of the passive mixer. According to measurements, mixing with the 3rd harmonic term of the LO provides 10dB less conversion gain compared to the fundamental mixing term.

2.3.2 LO Generation

The FLL is composed of a current controlled differential ring oscillator with a counter based digital controller. As previously mentioned, the ULP back-channel receiver doesn't require high performance PLL which has high reference cycle, and low phase noise DCO, which leads to large amount of power reduction. As shown in Figure 2.7, the specification of the ring oscillator can be set based on the target input power, system noise figure, and data-rate. According to the reference [44], it is proven that as the Nth relative harmonics component of the ring oscillator output has higher phase noise comparing to the fundamental by 20log10(N), without pushing 1/f3 corner frequency. According to analysis, we targeted phase noise of the ring oscillator which is

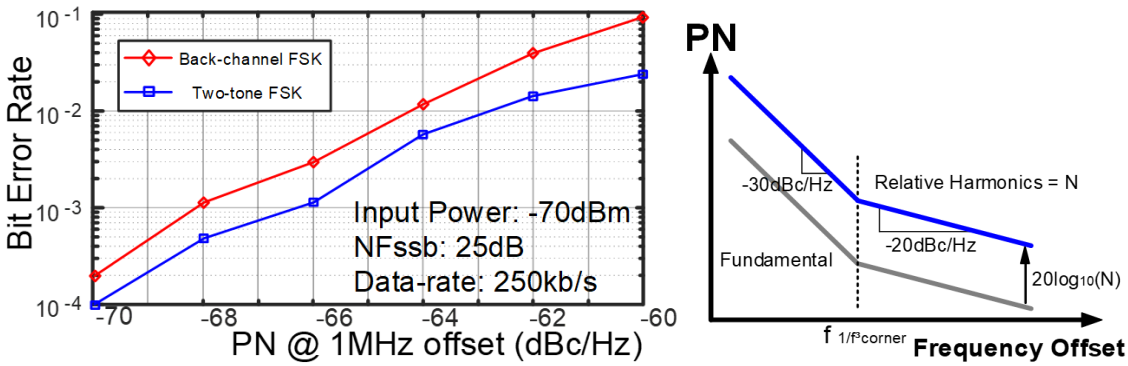


Figure 2.7 Phase noise specification analysis for wideband FSK demodulation.

around -70dBc/Hz at 1MHz offset, and came out with 5-stage differential ring oscillator considering the supply noise coming from the testing environment.

The digital controller counts the divided frequency over reference clock cycle periods, and compares this to the target. The loop filter then has two modes: 1) If the counter value is less than a threshold, it increments or decrements the binary control word of the current DAC by 1, approaching the final frequency with a slew rate; 2) If the counter value is above the threshold, meaning the DCO frequency is far from the target, the FLL enters a higher-gain mode and slews at a faster rate towards the target. The effective LO tuning resolution in the 5.8GHz band is 0.5MHz, sufficient for tuning to the center of a 20MHz Wi-Fi channel for demodulating back-channel FSK. The threshold of the digital controller, and the number of cycles is programmable. The 2nd LOs that drive the IF2 mixers are composed of I/Q square waves at 20MHz, and 10MHz for the high and low bands. Those are generated from the same FLL driving the RF mixer.

2.3.3 Intermediate Frequency, and Baseband Circuits

The first IF stage, IF1, is comprised of a low-noise amplifier (IF-LNA) and VGA which together provide all of the gain in the IF1 signal path (Figure 2.8, and Figure 2.9). An inverter-based self-biased common source amplifier is chosen for the IF-LNA due to its high input

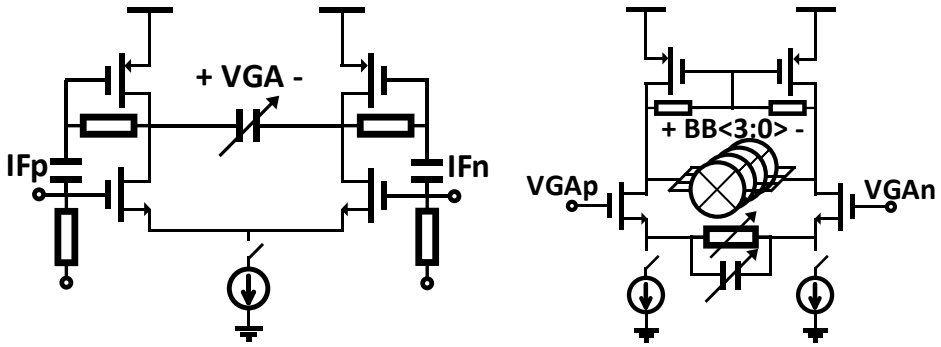


Figure 2.8 Circuit implementation of IF LNA (Left), and VGA+IF2 mixer (right).

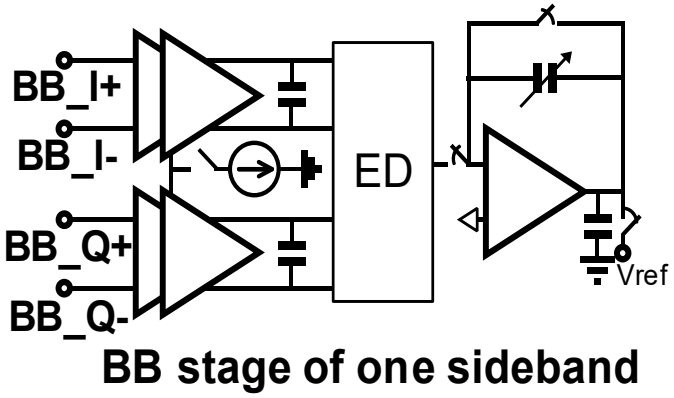


Figure 2.9 Baseband circuit implementation of one sideband.

impedance, and good gain-efficiency. The IF-LNA and VGA are self-biased through a replica circuit. These stages also perform the band-pass filtering of the down-converted IF1 signal from 5MHz to 25MHz.

The baseband stage collects the energy of each sideband of the OFDM symbol and compares these to demodulate the FSK back-channel signal. Signal energy is measured from the baseband stage by using quadrature down-conversion, squaring, and integration. This approach is chosen, rather than measuring the power at IF1, because of the asymmetric transfer function of the FSK band-pass filters which requires large current consumption with significant design complexity. The 5MHz-25MHz filtered IF signal is down-converted by quadrature mixers which are driven by two LOs which are generated from the main FLL. Each LO is centered on each

sideband. LPFs filters out the undesired band so that it captures only the in-band spectrum, however, due to its harmonic down-conversion, it is suggested to implement N-path filter [], or LPF in IF1 band. The topology of the LPFs is as same as the VGA, which use conventional source degenerated differential amplifiers, with the voltage gain controlled by source degenerated FETs for robust gain control and tuning range. The amplifier is cascaded, and loaded with adequate size of caps to cutoff >5MHz. After Filtering, the I and Q baseband signal is rectified (squared), and summed to a single node, which performs as I^2+Q^2. The rectified output is integrated by clocked integrator at the before the comparator, and every comparing cycle, the integrator is reset.

2.4 Measurement Results

The receiver was fabricated in a CMOS LP-65nm technology. The active area is 0.228mm². Figure 2.10 shows the BER performance versus input power at different back-channel data rates. The data-rate of the Wi-Fi back-channel FSK can be adjusted by combining multiple OFDM

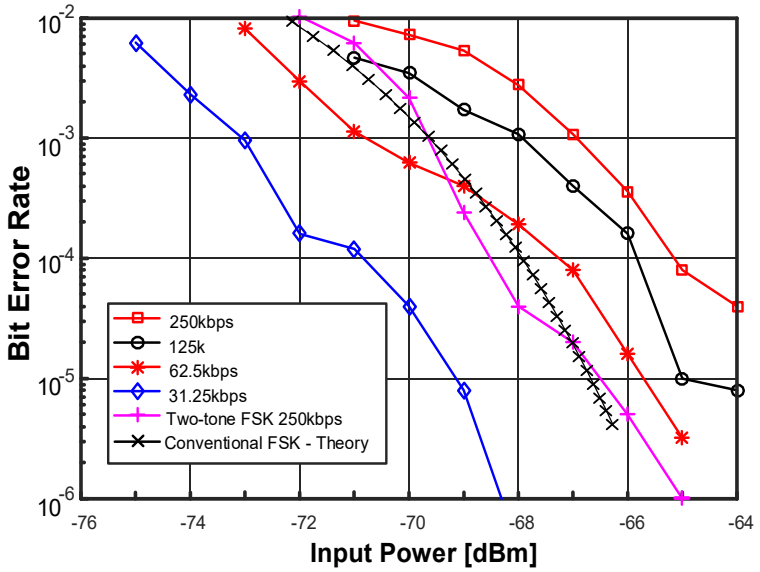


Figure 2.10 BER waterfall curve plot at different data-rate, and modulation.

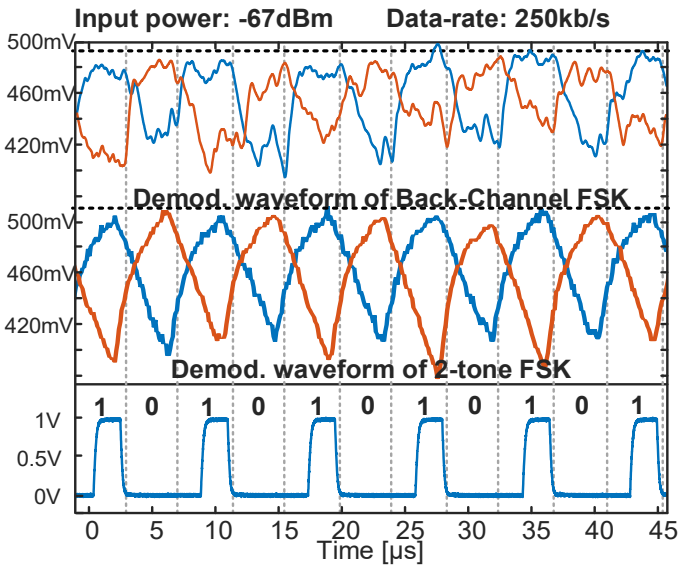


Figure 2.12 Demodulated waveform output, and RX data output from comparator.

symbols into one super symbol. For example, the sequence '1 0 0 1' with a data-rate of 125kb/s is generated by sending the Wi-Fi back-channel signal '11 00 00 11'.

The measured sensitivity at BER =10-3 is -67dBm when the data-rate is 250kb/s, and -72dBm when the data-rate is 31.25kb/s. Conventional two-tone FSK was also tested, which results in 1.5dB better performance than wideband FSK, because two-tone FSK captures more energy in the sideband comparing to wideband FSK when downconverted by noisy LO. Also, non-uniform transfer function of the receiver contributes to the difference in overall gain between two-tone FSK, and wideband FSK because center of the sidebands provides the highest gain, hence, the total gain provided for multiple-carrier wideband signals is effectively less than with pure tones. Figure 2.11 shows the signal to interference rejection ratio of the receiver. As can be seen, the SIR is 13dB for the adjacent higher channel, and 5dB for the adjacent lower channel because of imperfect image rejection. The LC resonant matching network on the RF front-end improves the voltage gain by 4dB. Off-chip RF filter and matching network attenuate the fundamental component, which eventually results in a gain difference between the fundamental (un-desired)

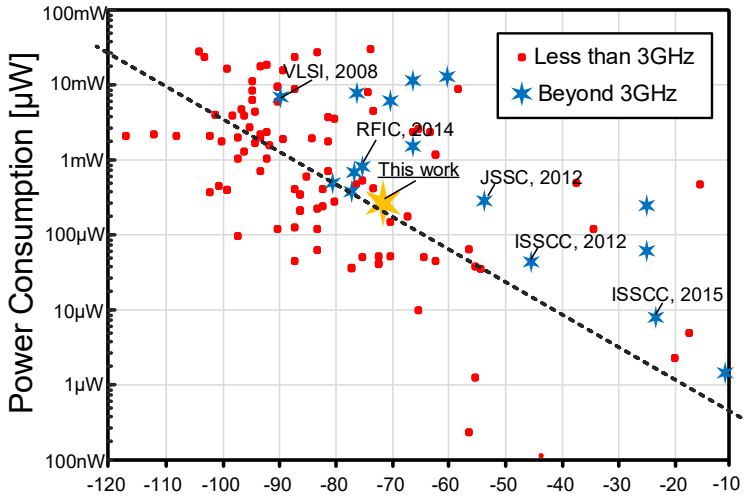


Figure 2.13 Data comparison on radio survey from 2005 to present. Data is collected from ISSCC, JSSC, VSLI, RFIC, CICC.

Table 2.1 Comparison with State-of-Art ULP Narrow Band Radios

	JSSC [63]	ISSCC [64]	ISSCC [65]	VLSI [66]	RFIC [67]	THIS WORK
PROCESS NODE	CMOS 65nm	CMOS 130nm	CMOS 65nm	CMOS 130nm	CMOS 65nm	CMOS 65nm
SUPPLY VOLTAGE	1.2V	3-3.6V	0.6V	1.5V	0.5V	1V, 0.85V
OPERATING FREQUENCY	5.6GHz	5.8GHz	5.8GHz	5GHz	5.85GHz	5.8GHz
MODULATION	PPM	OOK	OOK	OOK	OOK	FSK
ARCHITECTURE	Direct down-conversion	RF-rectification	RF-rectification	Super-regeneration	Direct down-conversion	Two-step down-conversion
DATA-RATE	1Mb/s	14kb/s	100kb/s	1.2Mb/s	300kb/s	250kb/s 31.25kb/s
ACTIVE POWER	290μW	15 μW	8.2 μW	6.6mW	830 μW	335 μW
SENSITIVITY*	-53.5dBm	-45dBm	-23dBm	-90dBm	-75dBm	-67dBm -72dBm
SIR**	-12dB	NA	NA	-30dB	NA	-13dB

* BER @ 10^{-3}
** Adjacent Channel

Table 2.2 Wi-Fi Back-channel Receiver Power Break-down

	FLL+RVCO	LO BUFFER	IF-LO GEN	IF STAGE	BB STAGE	BIAS
POWER CONSUMPTION	128μW	57μW	33μW	68μW	42μW	17μW

and 3rd harmonic (desired) component by 12dB. The overall gain of the receiver is 58dB at the

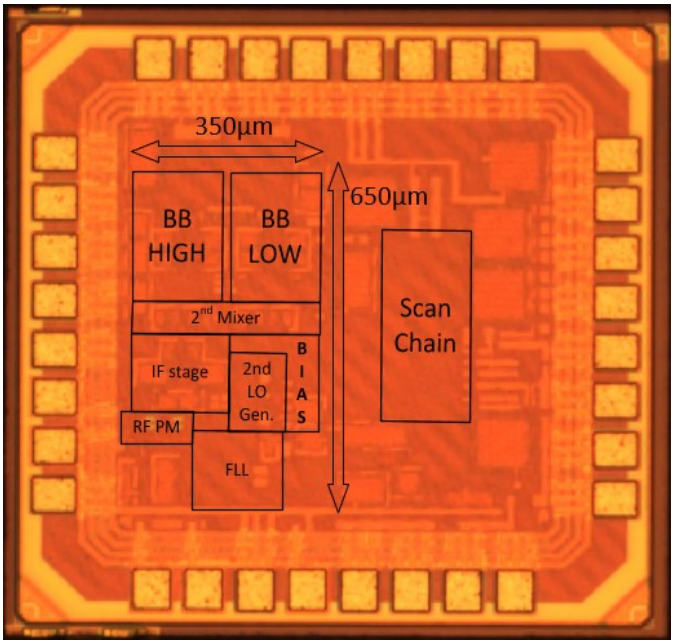


Figure 2.14 Chip die photograph.

output of the envelope detectors.

Figure 2.12 shows demodulated output waveform from envelope detection, and comparator output (captured from back-channel FSK), for both back-channel FSK, and 2-tone FSK signals. To show the difference of the output waveform clearly, symbols are alternated. A comparison between state-of-art narrow band ULP radios operating in the 5.8GHz band is shown in Table 2.1. Figure 2.13 shows sensitivity vs. power for state-of-art low power radios. This back-channel receiver is close to the Pareto-optimal line for all ULP radios operating above 3GHz, and the only one that is complaint with any IEEE standard.

2.5 Conclusion

An ULP FSK back-channel receiver in LP-65nm CMOS was presented. By utilizing binary FSK back-channel embedded in IEEE 802.11a packets, this receiver achieves ULP operation and compatibility with Wi-Fi standards. Down-conversion with the 3rd harmonic term

of the LO reduces the power consumption in the LO block significantly, at the expense of noise performance. The receiver consumes 335μW active power with a sensitivity of -72dBm at BER of 10-3.

Chapter 3 A 220µW -83dBm 5.8GHz 3rd-Harmonic Passive Mixer-First LP-WUR for IEEE 802.11ba

3.1 Introduction

Wi-Fi is the most utilized network protocol that has huge potential on widespread adoption of growing class of ULP IoT devices. However, as mentioned in Chapter 2.1, the commercial 802.11 radios consumes excessive power even with heavy duty-cycling, and on the other side, ULP radios are hardly utilized as IoT radios due to its custom network communication that limits the pervasiveness of the ULP IoT device. Recently, work has focused on bridging the gap between commercial 802.11 receivers and ULP radios, such as the 802.11ba task group for future deployments, and back-channel communication for backwards compatibility [45, 46].

The 802.11ba task group established a new standard to reduce the average power of 802.11 radios by integrating a low-power companion radio with the main 802.11 radio, which receives on-off keying (OOK) modulated signals (4 MHz, 13 subcarriers populated a long 20 MHz channel) from an 802.11 transmitter. The power budget of an active Wi-Fi network can be significantly reduced by leveraging a wake-up radio when the main Wi-Fi radio remains asleep [25, 47]. Wi-Fi back-channel communication is also presented [43], that generates a wideband, simple modulation scheme such as frequency shift keying (FSK), OOK, and pulsed phase shift keying (PPSK) by streaming a crafted bit sequence to the 802.11 data-path. Receivers were presented that support

these Wi-Fi wake-up modes, however, the sensitivity of -72 dBm [45, 46] is somewhat limiting compared to Wi-Fi radios at <-80 dBm.

In this Chapter, an ULP 802.11ba wake-up receiver is presented with a sensitivity of -83 dBm while consuming 220 μW with a ¼ coding rate. The receiver minimizes power by using a passive mixer-first architecture. Furthermore, 3rd harmonic down-conversion is used which requires a ring-based LO operating at 1/3 the RF frequency – reducing power in the LO and LO drivers. The receiver uses a 3-path 3rd harmonic mixer that enhances the 3rd harmonic component, while rejecting the fundamental component through the mixer. In addition, a 1:3 transform is used for passive voltage gain before the passive mixer to achieve an overall NF of 14 dB, resulting in the best sensitivity-power trade-off among >3 GHz ULP receivers, and Wi-Fi wake-up radios.

The Chapter is organized as follows. The 802.11 LP-WUR OOK frequency planning, and its (de)modulation is covered in Section II. Detailed circuit architectures and analysis of 3rd harmonic down-conversion and its matching network, and other circuit blocks in Section III. Measured results of the receiver, and a comparison with past ULP down-conversion receivers are discussed in Section IV. Finally, Section V concludes the Chapter.

3.2 Frequency Plan, and System Architecture

The frequency planning of the 802.11 LP-WUR is shown in Figure 3.2. Legacy Wi-Fi OFDM signals are generated by modulating sub-carriers in the frequency domain, converting sub-carrier symbols to the time domain, outputting them through a digital-to-analog converter (DAC), and finally up-converting the signal to RF. This OFDM architecture theoretically allows for a wide set of modulations such as OOK or M-ary FSK, although it is not specifically designed for this type of signal generation. By only updating the firmware of an 802.11 OFDM radio [25, 45], it is

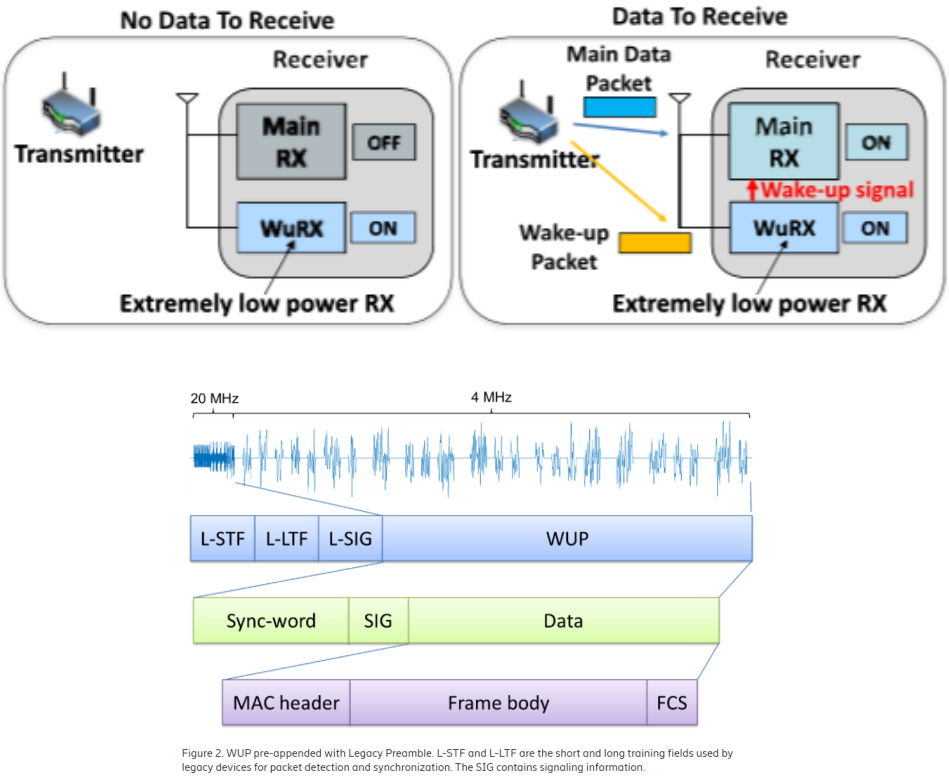


Figure 2. WUP pre-appended with Legacy Preamble. L-STF and L-LTF are the short and long training fields used by legacy devices for packet detection and synchronization. The SIG contains signaling information.

Figure 3.1 Conceptual diagram, and frame structure of 802.11 low-power wake-up companion radio [26].

possible to map narrowband OOK or FSK symbols onto OFDM subcarriers, and disable the remaining unused sub-carriers.

As shown in Figure 3.2, the 802.11 LP-WUR signal can be generated by selectively allocating power to a subset of sub-carriers, which are OOK modulated. The maximum symbol rate of the Wi-Fi wake-up data is 250 kS/s, the same as the OFDM symbol rate. As subcarriers are 312.5 kHz apart, the resulting 13 sub-carriers OOK WUR signal has a bandwidth of 4 MHz, which is wider than conventional ULP transceivers [25, 45]. The proposed frequency plan has a symmetric power allocation on double sided bands (DSB). According to studies that have been done in [25, 45], DSB symmetric power allocation with a single noisy LO with an extremely small loop bandwidth FLL (<10 kHz) does not introduce significant effect on the sensitivity compared

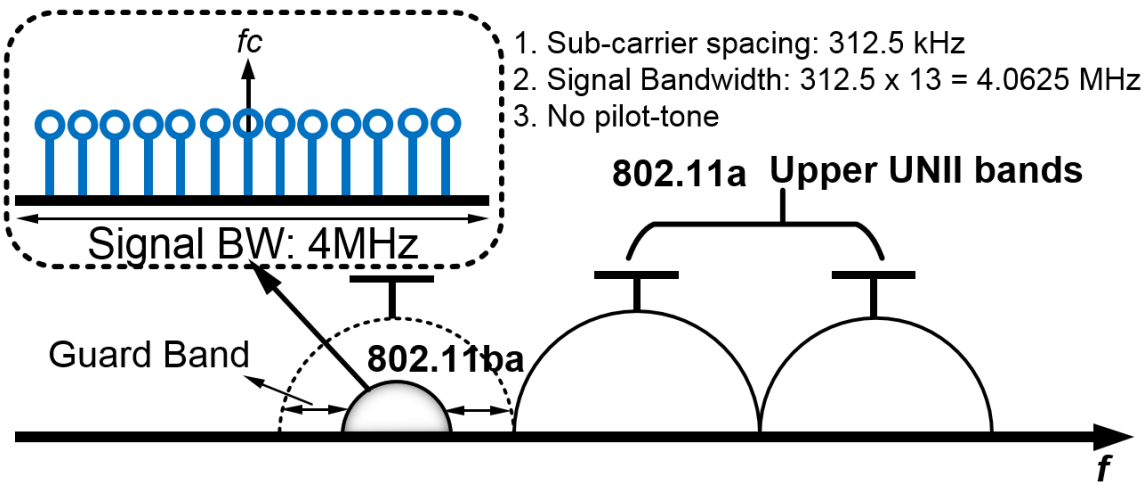


Figure 3.2 Frequency floor planning of 802.11ba (bottom).

to single side band (SSB) asymmetric power allocation without the image on the other side of the carrier. This removes the requirement for quadrature mixing at the receiver, and the multi-carriers are shifted slightly above the center frequency to avoid flicker noise floor when demodulating the wake-up signal.

As shown in Figure 3.2, 802.11ba is utilizing the existing 802.11a upper UNII bands so that it has a 4 MHz signal BW, with 8 MHz guard bands on each side, which relaxes the phase noise (PN) and filtering requirements of the receiver design. Compared to full band 802.11a that utilizes 52 sub-carriers, this saves 4 times the signal bandwidth and relaxes the required signal-to-noise ratio (SNR) of the receiver by 6 dB, while providing more margin on interferer rejection as well due to larger guard space between channels.

The system architecture is shown in Figure 3.3, which performs direct down-conversion. Although the WUR signal is generated from an 802.11 OFDM transmitter, the receiver does not require a highly linear RF front-end, high-resolution analog-to-digital converter, or significant digital baseband processing due to its relatively simple wideband (de)modulation scheme.

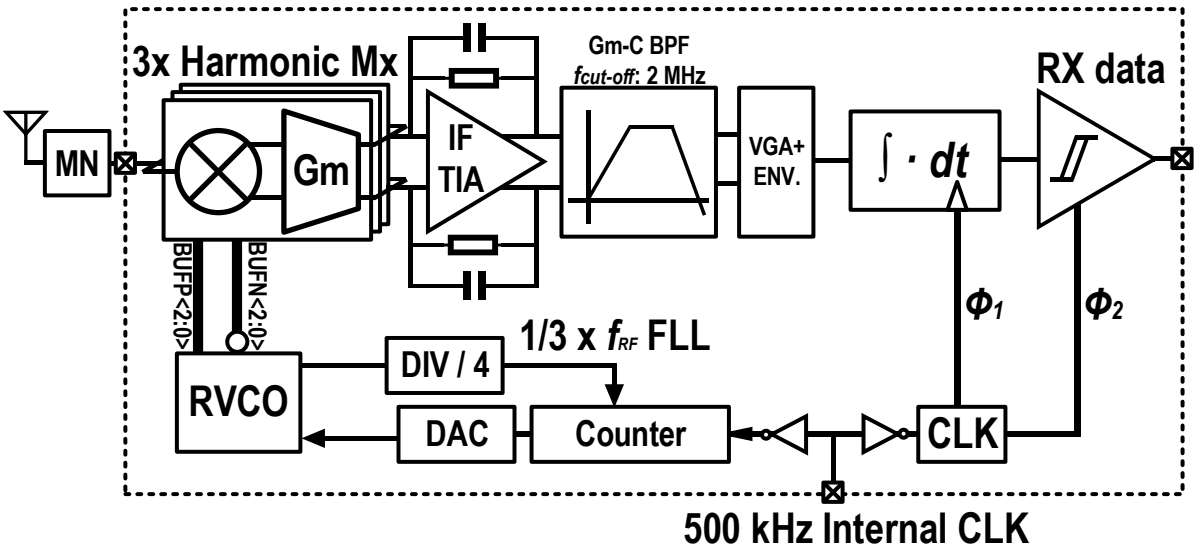


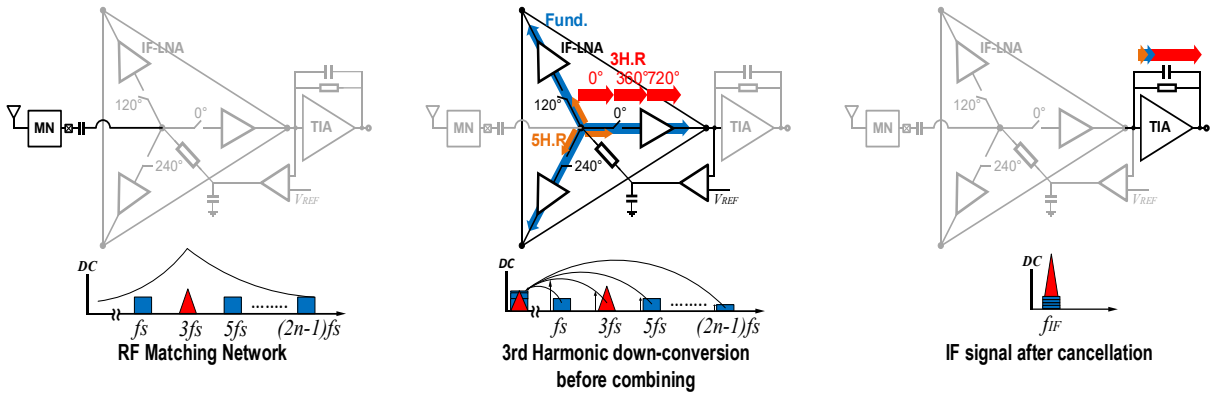
Figure 3.3 System block diagram of the receiver.

3.3 Circuit Implementation

For active wireless connectivity, the WUR has to achieve sensitivity of lowest data-rate of 802.11a transmitter, which is -82 dBm at data-rate of 6 Mb/s [48]. Thanks to the modulation explained in Section II, the minimum noise figure has been relaxed due to the relaxation of the SNR. This allows us to eliminate the power-hungry active RF gain stage in the WUR.

The system block diagram of the 802.11 LP-WUR is shown in Figure 3.3. The receiver is a passive mixer-first architecture with an off-chip matching network. Rather than using an LO-less RF energy detection architecture, which is common among ULP receivers because it results in the lowest active power, this receiver uses a ring-based voltage controlled oscillator (RVCO) to allow channel selection, improve selectivity, and operate at a lower active power than more power hungry LC-VCOs. The receiver receives 4 MHz wide OOK modulated RF signals in the 5.5-5.8 GHz band, compliant with the 802.11ba draft standard. These are down-converted with mixers that operate around 1/3 of the RF frequency.

To reduce power, no active RF gain stages are used. However, to maintain an adequate sensitivity, a passive voltage gain is implemented in the matching network. After the three mixer



(a) (b) (c)

Figure 3.4 RF front-end of the receiver using 3rd harmonics down-conversion in single mode (Actual RF front-end uses differential passive mixer). (a) RF matching, and filtering at RF input node. (b) 3rd harmonic down conversion. The IF-LNA after the passive mixer induces current from down converted voltage for current combination. (c) Induced currents are combined, improving 3rd harmonics while rejecting other harmonic components.

stages, the down-converted IF signals are combined in the current domain before amplification and filtering in TIA. After the TIA, the IF signal is filtered with a -40 dB/dec roll off. Finally, the filtered IF signal is rectified, and integrated by baseband circuits, and the RX data is retrieved. The following sub-sections will explain the details of each system block.

3.3.1 3rd Harmonic mixer-first RF Front-End

As shown in Figure 3.4, the ULP 802.11ba wake-up receiver uses a passive mixer-first RF front-end which down converts the 5.8 GHz 802.11 RF signal with the 3rd harmonic generated from the RVCO. This saves power because neither the oscillator nor LO buffer, which are the most power-hungry blocks as shown in the pie chart in Figure 3.18, are required to operate at 5.8 GHz. Sub-harmonic down-conversion architectures have been proposed [40, 49] for low-power receivers that perform frequency multiplication from a low frequency oscillator by using either

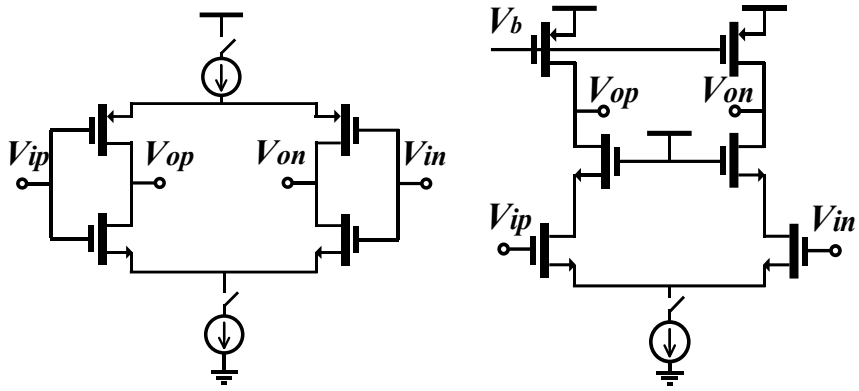


Figure 3.5 IF circuits. Left figure is a single cell of IF low-noise amplifier (LNA), and right figure is a trans-impedance amplifier (TIA).

logic, or injection locking of high frequency reference clocks. The drawback to this approach is they still require significant power in the LO buffers and fast logic circuits. In contrast, the highest frequency that is generated and/or used in this receiver is $f_{RF}/3$, or 1.933 GHz, thus significantly reducing the active power of the RVCO and buffers. Odd harmonic down-conversion was chosen rather than even harmonic down-conversion because it has a better flicker noise corner vs. power trade-off of the RVCO, which will be covered in Section III C.

The spectrum diagram in Figure 3.4 illustrates the behavior of each block that comprise the RF front-end. The RF signal is filtered, and impedance boosted as shown in Figure 3.4(a). A commutating passive mixer has a non-linear response, so that at Figure 3.4(b), when feeding an LO operating at f_{LO} to the mixer, it produces harmonic components at $(2n-1) \times f_{LO}$ (n is an integer). The actual passive mixer is differential pair that rejects even-order harmonics after down-conversion. Then, in Figure 3.4(c), the down-converted signals after each mixer a summed in the current domain using IF low noise amplifiers (IF-LNA) transconductors. Figure 3.5 shows the schematics of the IF-LNA and TIA. The IF-LNAs are self-biased by connecting each differential IF-LNA output to the mixer input with a triode resistor that provides large resistance, thus only regulating the DC common-mode voltage. The construction and destruction of each harmonic

components happen at Figure 3.4(c). By combining signals from *N*-paths with mixers operating at a 360º/*N* phase difference each, the N^{th} harmonic signals at the outputs of the *N* mixers will be in-phase at baseband, while the other harmonic components are out-of-phase and cancel.

The behavior of the N^{th} harmonic down conversion can be expressed with an equivalent mathematical expression. The RF signal at the input of the passive mixer can be expressed as $V_{rf}(t)$, and the RF switch based mixer can be expressed as the Tayler series of a square wave. As shown in (1), after voltage-current conversion from the IF-LNA input (*Gm*), the down-converted RF signal before the TIA can be expressed as

$$G_m V_{rf}(t)\left[\sum_{k=1}^{N}\sum_{n=1}\frac{A_0}{2n-1}\cos\left((2n-1)\left(\omega_{LO}t+\frac{2\pi}{N}k\right)\right)\right]$$

$$=G_m V_{rf}(t)\sum_{l=1}\frac{NA_0}{N(2l-1)}\cos(N(2l-1)\omega_{LO}t) \qquad (1)$$

The noise figure of the 3rd harmonic passive mixer front-end can be determined by the insertion loss of the passive mixer, and noise folding from the higher/lower harmonics. As the number of paths, *N*, increases, the insertion loss increases, along with the number of higher/lower harmonics up to the frequency of interest. The switch noise is suppressed with current summation after the IF-LNA because the correlated down converted RF signal add constructively in current, while the uncorrelated switch noise only adds in power. Simulation results of the power and NF for each harmonic passive mixer down-conversion is shown in Figure 3.6. Increasing *N* beyond a value of 3 offers diminishing returns in NF vs. active power. Comparing to edge combining duty-

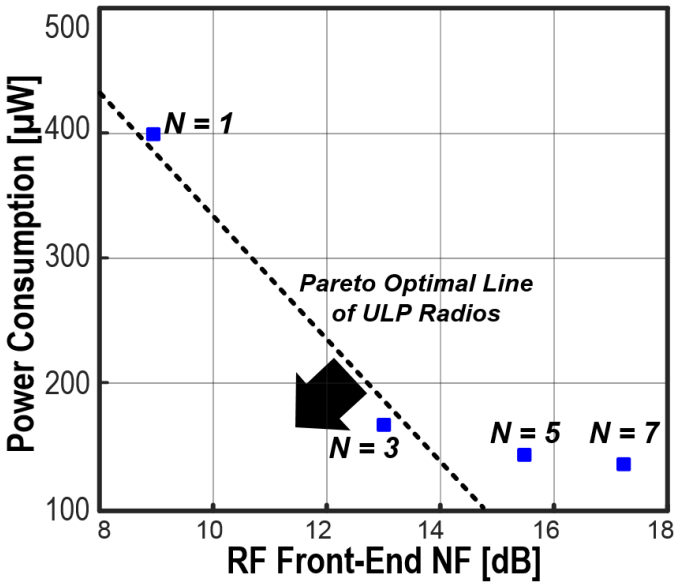


Figure 3.6 Simulation results of NF vs. Power trade-off of Nth harmonic Passive mixer RF Front-End. The line represents the Pareto optimal line of state-of-art ULP receivers.

cycled frequency multi-plication mixer, this save decent amount of power because it uses small number of RF switches, and does not require any high-speed complex logic circuits. Considering noise analysis, and mismatch calibration, this architecture shows an optimal trade-off between performance and power with $N = 3$, so that a 3rd harmonic 3-path passive mixer is implemented.

Including differential RF signaling, the 3rd harmonic passive mixer architecture requires $2N = 6$ mixers operating at f_{RF}/N. The number of LO buffers and RF switches used for the RF front-end is 2 times fewer than in [40], a harmonic mixing architecture using injection locking. These buffers wind up being the dominant factor of the overall ULP receiver power consumption. Furthermore, this architecture doesn't inevitably require a high-Q RF filtering stage in front of the mixing stage due to undesired harmonic spurs generated from the sub-sampling mixer down-converting unwanted signals to the IF band, as in [49]. Instead, these unwanted signals cancel in the current-domain at baseband after the mixers, because they arrive out of phase. As shown in

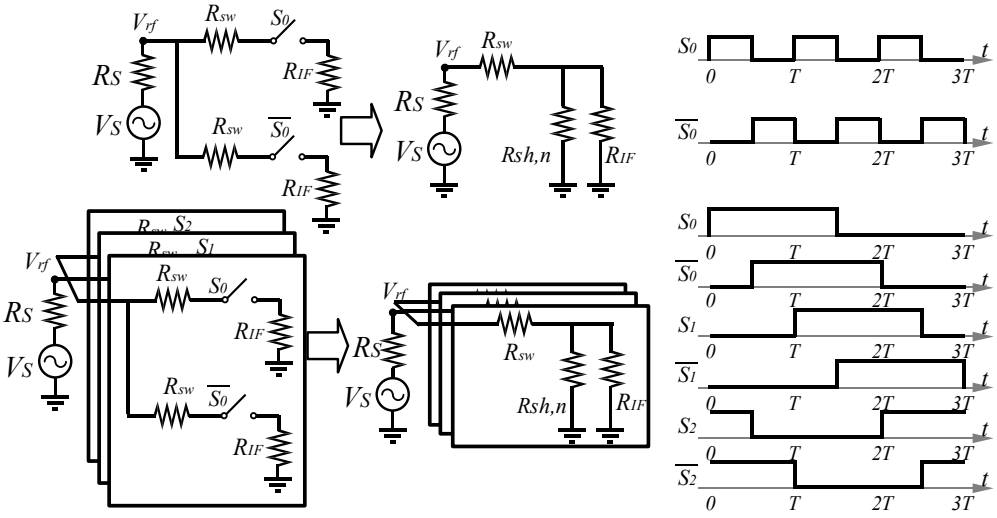


Figure 3.7 Two path passive mixer linear time invariant equivalent model (top) [22, 52], and 3rd harmonic linear time invariant equivalent model (bottom).

Figure 3.4, the sub-harmonic passive mixer only requires *N* narrowband IF-LNAs, which is a good trade-off for ULP radio designs because these operate at significantly lower power than RF stages.

3.3.2 Matching Network, and NF Optimization of RF Front-End

Many mixer studies have been published on methods to improve the linearity of receivers [50, 51]. These references go through a noise analysis assuming sufficient wideband matching to a 50 Ohm terminal, assuming a low switch resistance (usually < 50 Ohm). Low switch resistance is achieved by wide FETs, driving up the LO buffering requirements and thus the power. This mixer-first architecture has much higher high switch resistance from the mixer switches because it has a low VDD, and narrow FETs to reduce the power from the LO buffers. In this work, a FET of 3 μm/60 nm is chosen which has a switch resistance of more than 300 Ohm at 5.8 GHz. Therefore, the input impedance at the RF node is large, which would usually require a high quality factor off-chip matching network to provide sufficient matching.

The 3rd harmonic passive mixer can be easily matched with a 50 Ohm interface with high resistive switch resistance. According to the equation from [21, 51], $R_{sh,n}$ in Figure 3.7 is expressed as

$$R_{sh,n} = \frac{2\gamma(R_S + R_{sw})R_{IF}}{2(R_S + R_{sw})(n^2 - \gamma) + R_{IF}(n^2 - 2\gamma)}.$$

$$n = 1, 3, 5 \ldots. \quad (2)$$

The input impedance of the 2-path passive mixer can be derived based on the linear time invariant equivalent model as

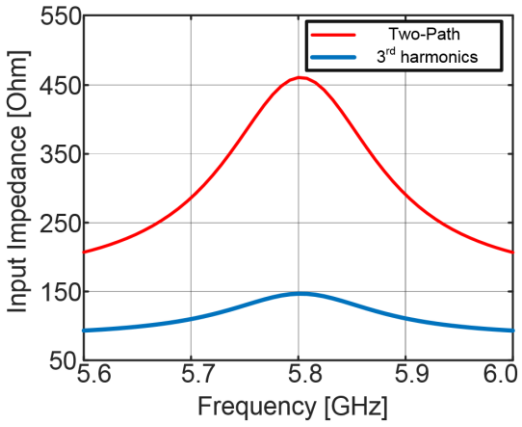
$$Z_{in}(n\omega_{LO} + \omega_{IF}) = [R_{sw} + (R_{sh,n}||R_{IF})||\left(\frac{1}{jn\omega_{IF}C_{IF}}\right)].$$

$$n = 1, 3, 5 \ldots. \quad (3)$$

The Input impedance of 3rd harmonic passive mixer in Figure 3.7 can be expressed as

$$Z_{in-3HR} = \frac{Z_{in}(3\omega_{LO})}{3} = \frac{R_{sw} + (R_{sh,3}||R_{IF})}{3}. \quad (4)$$

Assuming that $R_{IF} = \infty$, setting $R_{sw} \cong 2.82\ R_S$ will match the 3rd harmonic passive mixer input impedance Z_{in-3HR} to R_S. For example, if matching to a 50 Ohm terminal, the switch resistance



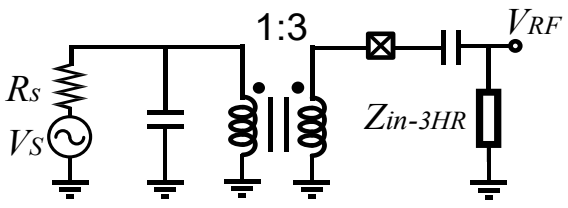


Figure 3.8 Input impedance of the two-path passive mixer, and 3rd harmonic passive mixer (left). RF matching network of 3rd harmonic passive mixer (right).

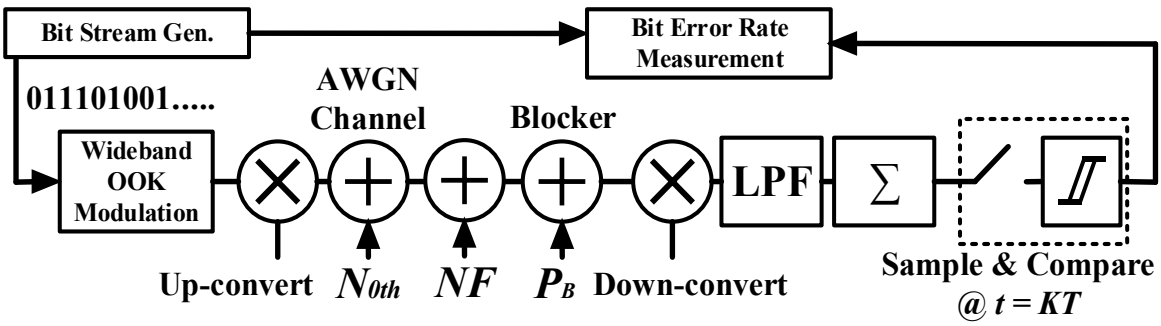


Figure 3.9 Equivalent Model of WUR for PN, and Blocker analysis

has to be roughly 141 Ohms for a 3rd harmonic passive mixer. Figure 3.8 shows the input impedance of a two-path, and 3rd harmonic passive mixer over frequency.

For acceptable noise figure, with good matching, the low-power mixer first architecture requires a step-up transformer [50]. The effective input impedance seen from the RF node is around 1/3 of a single balanced passive mixer. As can be seen in Figure 3.8, the RF node is interfaced with 1:3 RF transformer to provide matching and passive voltage gain. This approach helps achieve the required sensitivity with a NF <16 dB (calculated from a -82 dBm sensitivity requirement).

Ideally, the front-end can perfectly reject the fundamental RF component while down-converting signals at the 3rd harmonic frequency. However, two mismatch factors affect this rejection ratio (3rd harmonic / fundamental). Mismatch in the delay cells of the RVCO generate phase mismatch which reduces the rejection ratio as this mismatch increases. However, the dominant factor is gain mismatch in the first inverter-based IF stage, which impacts the rejection ratio due to its common mode offset between IF-LNAs. According to simulation, a phase error less than 5% results in a rejection ratio up to 40 dB.

To minimize the gain mismatch, self-biased current steering differential IF amplifiers are used with fine resolution gain tuning. Without calibration, there were large variations observed

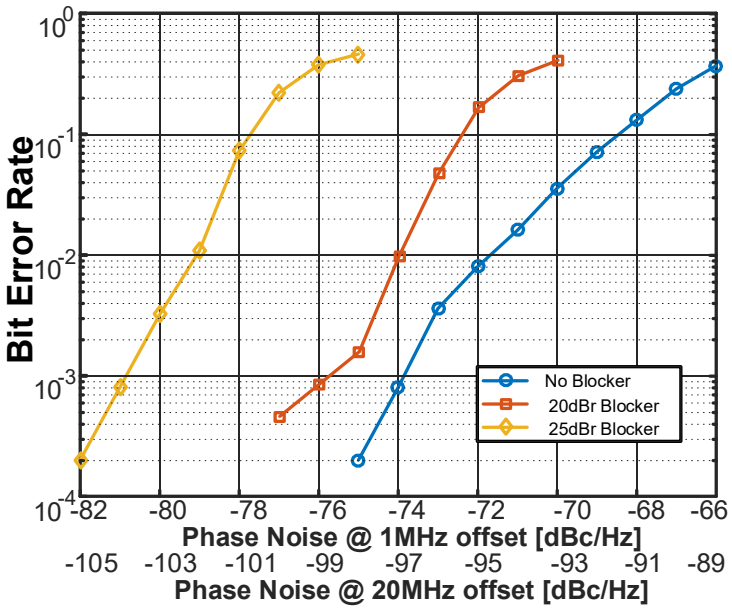


Figure 3.10 BER versus phase noise analysis with different blocker power. NF, and target sensitivity were considered in this plot.

chip to chip, and the worst rejection ratio measured was 25 dB. After calibration, the worst rejection ratio measured was 37 dB, including passive RF matching before the RF front-end.

3.3.3 LO Analysis, and Generation

For low power design, an RVCO is used for the RF oscillator, however, this can result in degradation of the sensitivity due to tone spreading from the high phase noise of the RVCO. High phase noise also limits the blocker tolerance [52] of the receiver. This section explains how phase noise of the RVCO was chosen, and the impact on system performance.

Figure 3.9 shows the equivalent model of the 802.11 WUR that was implemented to define the phase noise profile that achieves a sensitivity of -82 dBm, considering a target NF, while rejecting interferers of >20 dB. The following describes the design and simulation procedure. First, the number of samples was chosen that can easily show the BER performance, then, the bit sequence for each sample was randomized. Based on the current bit, a 13 sub-carrier, 4 MHz wide

OOK modulated baseband signal was generated. The baseband signal was up-converted with an input power of the target WUR sensitivity level. Then, thermal noise with the WUR's noise figure, and blocker power were added to the RF signal, which was then direct down-converted. After 2nd order low pass filtering and integration, the signal was sampled and compared every 4 μs. The retrieved bit sequence was compared with the input randomized bit sequence, and BER was measured.

First of all, we focused on the phase noise at a frequency offset of <2 MHz because it directly relates to the in-band power loss due to the tone-spreading. This approach was been done to achieve the optimal point of the LO design that minimizes the tone spread along the 4 MHz signal bandwidth, while also minimizing the active power consumption of the RF oscillator. Figure 3.10 shows the BER results as a function of phase noise of the RVCO for the desired channel, and the adjacent channel. According to the simulation, the in-band phase noise of -75 dBc/Hz at offset frequency of 1 MHz is been chosen that achieves BER of 10^{-3} with in signal level of -82 dBm. Then, blocker RF power at adjacent channel (20 MHz offset frequency) was inserted along the AWGN channel to specify the phase noise at high frequency offset over 10 MHz. Theoretically, phase noise profile for out-of-band blocker rejection can be chosen by (5). Assuming noise from the blocker's tone spread due to the phase noise dominates the total noise floor ($N_{Blocker} \gg N_{thermal}$), the *SNR* of the receiver when the blocker is present can be expressed as

$$SNR_{blocker}[dB] = (P_C - P_B)[dBm] - \mathcal{L}_{LO}(\Delta f)[dBc/Hz] - 10\,log\,BW\,[dBHz] \quad (5)$$

where P_C is the carrier power on the desired channel, and P_B is the blocker power [14]. To achieve adjacent channel blocker rejection of >20 dB with minimum required *SNR* of 12 dB [25],

$$\mathcal{L}_{LO}(\Delta f = 20\ MHz) \leq -20[\text{dB}] - 10\,log(4MHz)[dBHz] - SNR_{blocker,min}[dB] = -98[\,dBc/Hz]. \quad (6)$$

With practical understanding the a low active power RVCO's noise corner of $1/f^3$ easily exceeds 1 MHz , we applied a phase noise slope of <-20 dBc/Hz^2 above a 1 MHz frequency offset.

To achieve this phase noise specification with minimum active power, time-interleaved RVCOs (TI-RVCOs) from [44] is used for LO design that can achieve better phase noise specification at a certain offset frequency for narrowband application that can provide better power efficiency when compared to conventional RVCOs. Using a harmonic component from a lower-

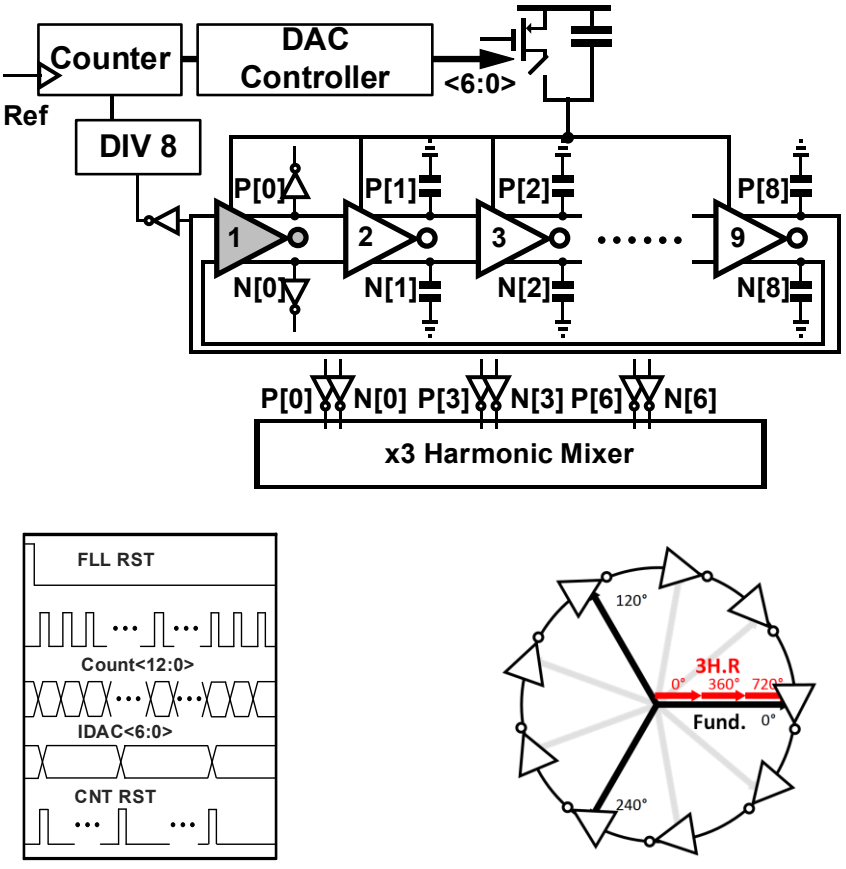


Figure 3.11 Frequency locked loop of the receiver (top), timing diagram of the FLL (bottom left), and conceptual diagram of phase aggregation for 3rd harmonic improvement (bottom right).

operating-frequency TI-RVCO results in a lower $1/f^3$ frequency corner at the target RF frequency when compared to an RVCO that operates directly at the target RF frequency. This results in better phase noise vs. power efficiency for harmonic TI-RVCOs. Furthermore, the power dissipated from the divider in a TI-RVCO based FLL operates at a lower frequency, further reducing power. In [44], logic cells are used to multiply the frequency of a TI-RVCO. However, in this design the low-frequency LO signals are directly applied to the mixer which performs harmonic mixing, saving power from high-speed logic.

To aggregate 3 phase offsets from the RVCO that runs at $f_{RF}/3$, a 9-stage differential RVCO was chosen. As shown in Figure 3.11, the LO is comprised of a 9-stage differential TI-RVCO, and counter-based programmable FLL with a low frequency reference for frequency calibration. The DAC counter decides to in/decrease the RVCO current based on a duty-cycled counter value. The counter counts frequency pulses from the divider for several reference cycles to improve the center frequency resolution. When the counted value exceeds the target reference value, the IDAC current is reduced, and vice versa when the value is lower than the reference value. For fine settling, the FLL updates its code word every 16 reference cycles, which is 32 μsec. For coarse settling, the IDAC changes with larger steps with 2 reference cycles when the absolute value difference between the counter and reference is over a programmable threshold.

3.3.4 Intermediate Frequency, and Baseband Circuits

After 3rd harmonic down-conversion, the OOK data is retrieved after IF gain stages and energy collection stages. As shown in Figure 3.4, The IF signal is low pass filtered with an IF center frequency below 2 MHz. 2nd-order Gm-C filters with gyrators were used for each filter design that can mitigate the distortion that comes from the down conversion of out-of-band blockers [50]. To achieve an adjacent channel SIR better than -20 dB, -40 dB/dec roll-off is required with the given RVCO PN profile. The baseband filter has a high pass corner frequency of 20 kHz, which is close to one-third of WRX data-rate. Utilizing a scrambler in the 802.11 data path, we avoid a bit stream of more than 4 consecutive equal bits, which is sufficient to stay above the high-pass corner. The filtered signals are envelop-detected and then integrated, then finally compared with an on-chip voltage reference with a 1-bit comparator. The integrator is oversampled by an external clock to determine the symbol boundaries. The measured gain provided from baseband is 23 dB.

3.4 Measured Results, and Comparisons

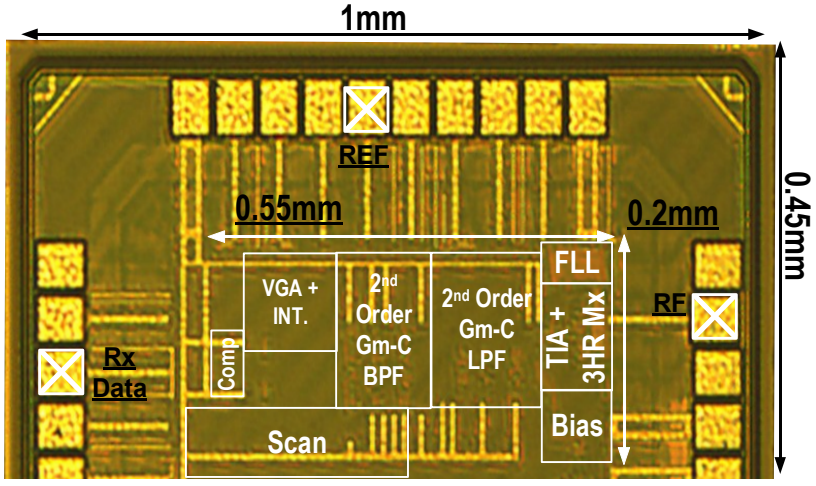


Figure 3.12 A CMOS 40nm chip photograph.

The 802.11 WUR was fabricated in a CMOS 40 nm technology with an active area of 0.151 mm2, as shown in Figure 3.12. The receiver is operating at 5.5-5.8 GHz with signal bandwidth of 4 MHz, which utilizes only part of the 802.11a upper UNII band. The 802.11 WUR uses 500 kHz external clock, and transformer as off-chip components. Figure 3.13 shows a measured BER waterfall curve. The BER is measured with alternated 802.11ba data. The sensitivity of 802.11 WUR is -83 dBm at BER of 10-3, and data-rate of 62.5 kbps. The sensitivity got 3 dB increment

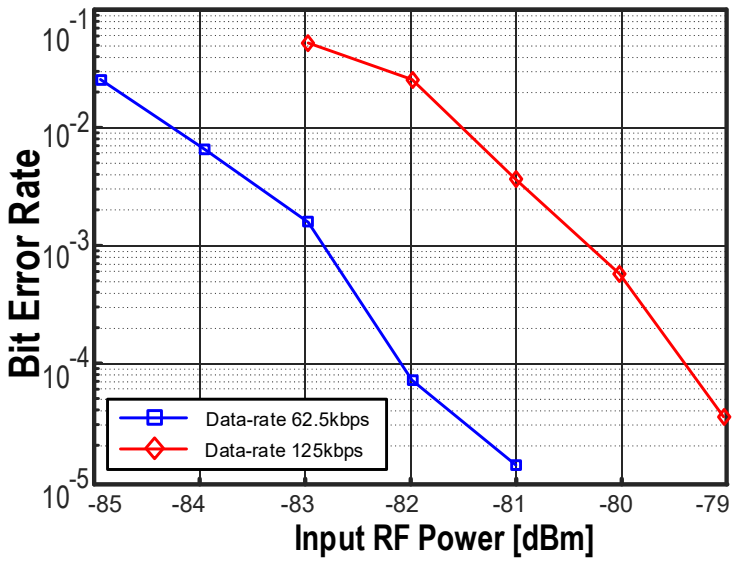


Figure 3.13 BER waterfall curve at different data-rates.

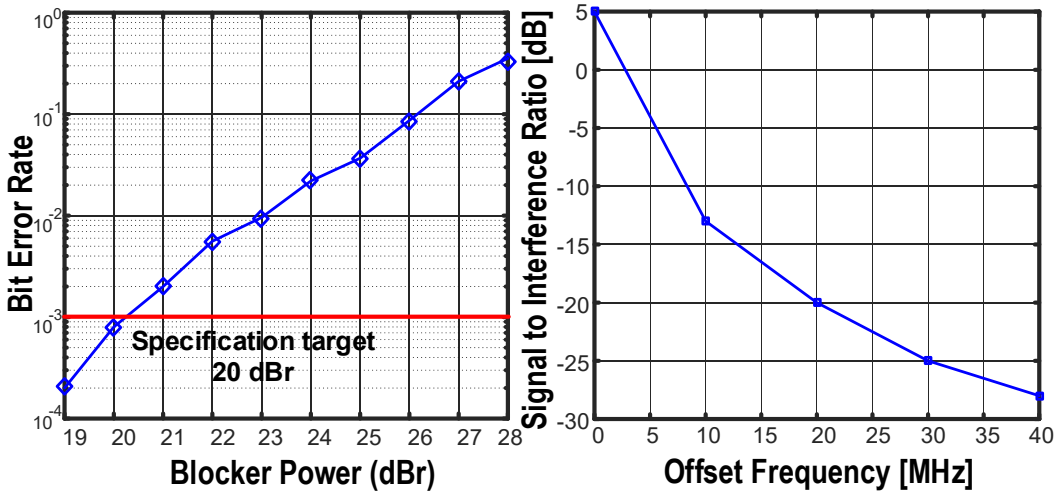


Figure 3.14 BER versus blocker power of adjacent channel 1 (left), and signal-to-interference ratio (SIR) versus offset frequency (right).

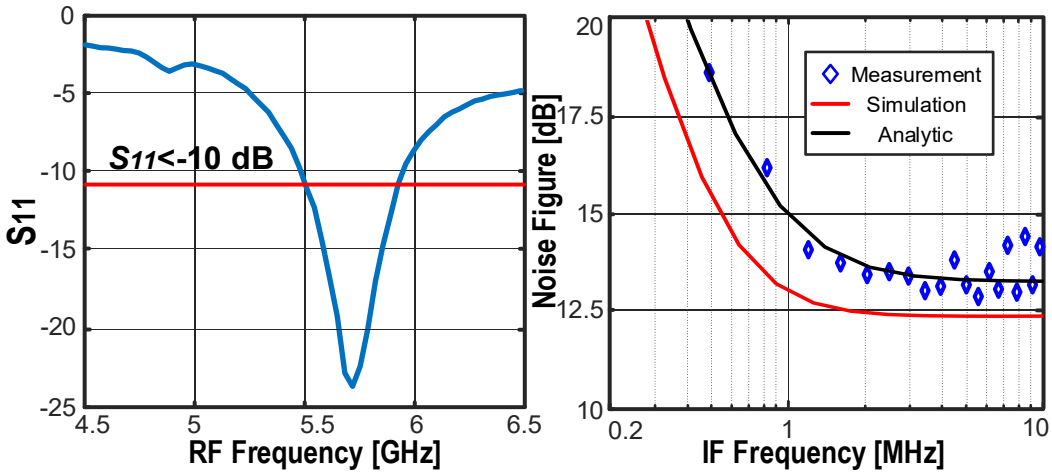


Figure 3.15 S11, and Noise Figure of the receiver.

as the data-rate increased twice, which is 125 kbps. The tone-spread of down-converted RF signal due to phase noise degraded power captured in 4 MHz bandwidth by 1 dB.

Interferer measurements are done with randomized binary data. Figure 3.14 shows blocker performance of the 802.11 WUR. The left figure in Figure 3.14 shows BER performance in different blocker power at adjacent channel 1, which has 20 MHz offset from the desired center frequency. The SIR of adjacent channel 1, and 2 are -20 dB, and -28 dB, respectively. The interference performance can be limited by the PN of the RVCO, thus, for narrow band receivers,

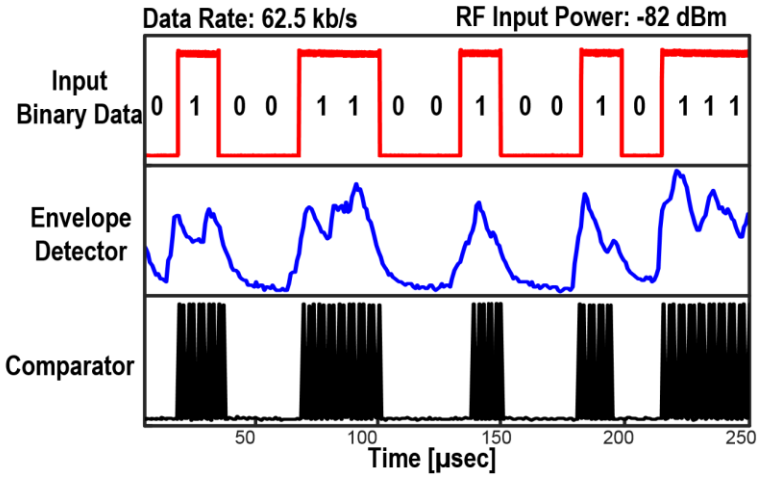
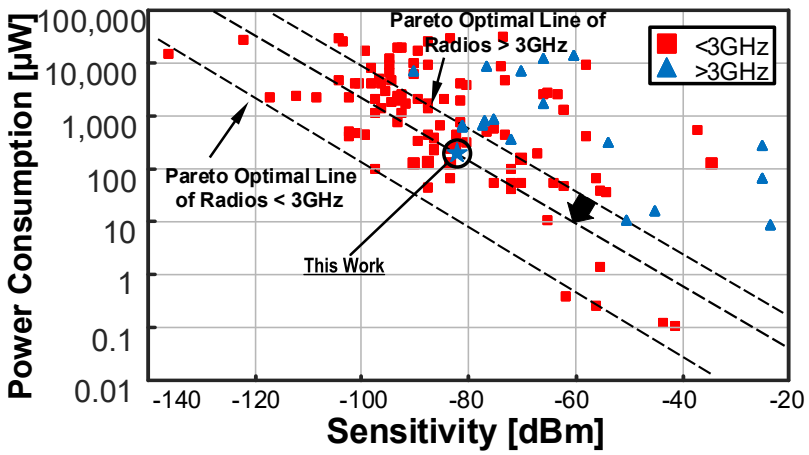
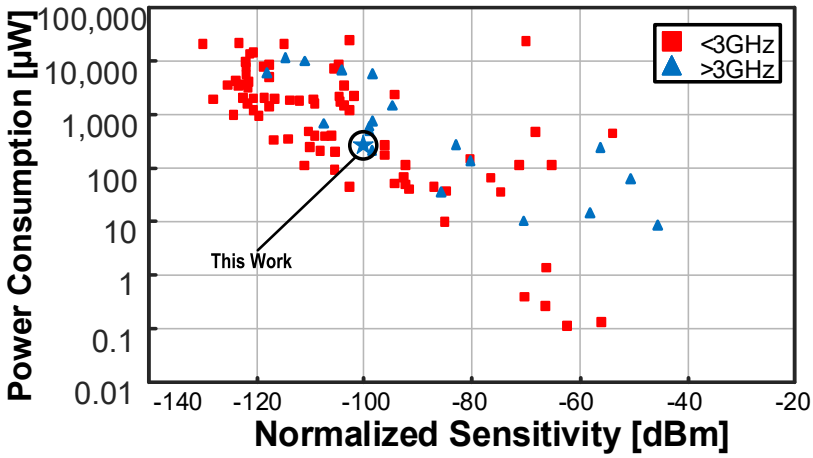


Figure 3.16 Receiver outputs from final bit decision inter stages. The 802.11ba data is randomized with ¼ coding rate.



(a)



(b)

Figure 3.17 ULP radio survey from 2005 to present [17]. The data of the radio survey is from top conferences (ISSCC, VLSI, RFIC, CICC) and commercial TRx chips. (a) Sensitivity vs. power consumption. (b) Normalized sensitivity vs. power consumption that is weighed to data-rate in kbps.

SIR performance is dominated by PN rather than the order of the filter when the order is reasonably high (≥3).

The measured noise figure, and S11 is shown in Figure 3.15. The noise figure of the system is 14 dB across the signal bandwidth, which matches simulations very well. However, the measured flicker noise corner had a slight deviation between the simulation result, which was

Table 3.1 Comparison with State-of-Art ULP Radios

	[62]	[22]	[46]	[47]	THIS WORK
CMOS TECH. [NM]	90	65	14 FinFET	65	40
ACTIVE AREA [MM^2]	0.9	0.058	0.19	0.228	0.151
EXTERNAL COMPONENT	1 MHz External Clock	High-Q inductors	32 kHz RTC	250 kHz External Clock Off-chip RF Filter	500 kHz External Clock Off-chip Transformer
CARRIER FREQUENCY [GHZ]	3-5	2.4	2.4	5.8	5.5-5.8
VOLTAGE [V]	1	0.5	0.95	1	0.95/0.55**
MODULATION	FM-UWB	OOK	OOK	FSK	OOK
SENSITIVITY [DBM] @ 10^{-3}	-80.5	-97/-92	-72	-72	-83
ACTIVE POWER [µW]	580	99	95	335	220
NOISE FIGURE [DB]	6.6	20***	23.5***	25***	14
DATA RATE [KB/S]	200	10/50	62.5	31.25	62.5
LO GENERATION	No LO, RF Env.	Unlocked LC-VCO	Ring with FLL	Ring with FLL	TI-RVCO with FLL
SIR*[DB]	-28	-25/-22	-20****	-13	-20
WIFI WUR	N	N	Y	Y	Y

* Adjacent Channel **0.5V for VCO, 0.95V for Analog Blocks

*** *Back calculated from Sensitivity* [dB] = -174 + *signal BW.* + *NF* + *SNRout.* **** ACI rejection measurement

Table 3.2 5.8 GHz 802.11 Wake-Up Receiver Power Break-down

	RVCO+FLL	IF-LNA	TIA	GM-C FILTER	ENV.	INT.	BIAS CIRC.	EXT. CLOCK
POWER [µW]	137	30	15	15	5	5	10	3

within the range of PVT variation. By boosting the input impedance, the receiver was able to achieve S11 < -10 dB across desired band 5.5-5.8 GHz.

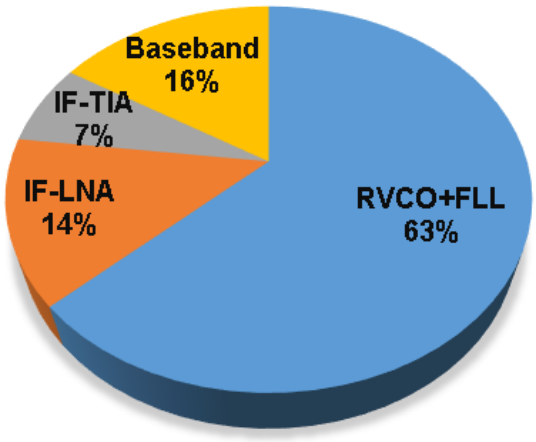


Figure 3.18 A power breakdown pie chart of receiver.

Figure 3.16 is showing demodulated randomized RF data. The down-converted signal is integrated, and oversampled by the comparator by 8 times to find the symbol boundary. The input RF power was -82 dBm.

The measured LO leakage power at the RF input was -92 dBm at 5.8 GHz. The active power of the 802.11 WUR is 220 μW, and its detail power break-down, and pie chart are depicted in Figure 3.3. As shown in the pie chart, 2/3 of the power is consumed by the RF blocks. The 500 kHz reference clock generation which can be realized with a 3 μW crystal oscillator, is included. Table 3.1 summarizes the performance of the receiver with state of art Wi-Fi wake-up radio, and high operating frequency ULP receivers which have the best performance in sensitivity-power trade-off. According to ULP survey shown in Figure 3.17(a), the receiver advances the Pareto optimal line of >3 GHz receivers in sensitivity-power trade-off. Based on the data-rate of the receiver, Figure 3.17(b) shows the ULP receiver survey with normalized sensitivity that is expressed as

$$P_{Sense,Norm} = P_{Sense} - 10\log_{10}\left(\frac{Datarate}{1kbps}\right). \qquad (7)$$

The sensitivity is normalized to data-rate in unit of kbps.

3.5 Conclusion

An IEEE 802.11ba LP-WUR receiver is presented. The receiver demodulates OOK modulated messages generated by an 802.11 OFDM Wi-Fi transmitter operating at 5.8 GHz. The 3rd harmonic down-conversion receiver reduces active power consumption, while rejecting unwanted harmonic components. Sufficient noise figure was achieved by using a 1:3 transformer that provides gain to a high switch-loss mixer-first RF front-end with good matching across 5.5-5.8 GHz. The receiver achieves a sensitivity of -83 dBm while consuming 220 μW at a BER of 10-3 and data-rate of 62.5 kb/s, which shows the best sensitivity-power trade-off among >3 GHz operation frequency receivers.

Chapter 4 A 0.2V, 578µW 2.4GHz 802.11ba WiFi Wake-Up Receiver with -91.5dBm Sensitivity for MELs Phantom Energy Reduction

4.1 Introduction

4.1.1 Node Controlling SoC for MELs

Miscellaneous electric loads (MELs) are electric appliances that plug into outlets, like coffee makers, printers, televisions, etc. The power consumption of MELs is significant, accounting for 30% of total electricity consumption in residential buildings and 36% in commercial buildings according to the U.S. Department of Energy (DoE) [53]. More importantly, those MELs still consume watt-level power even if they are turned off, which is called phantom energy by the DoE. These loads are projected to increase over the next decade, and the next generation of MELs require zero energy consumption when they are off and

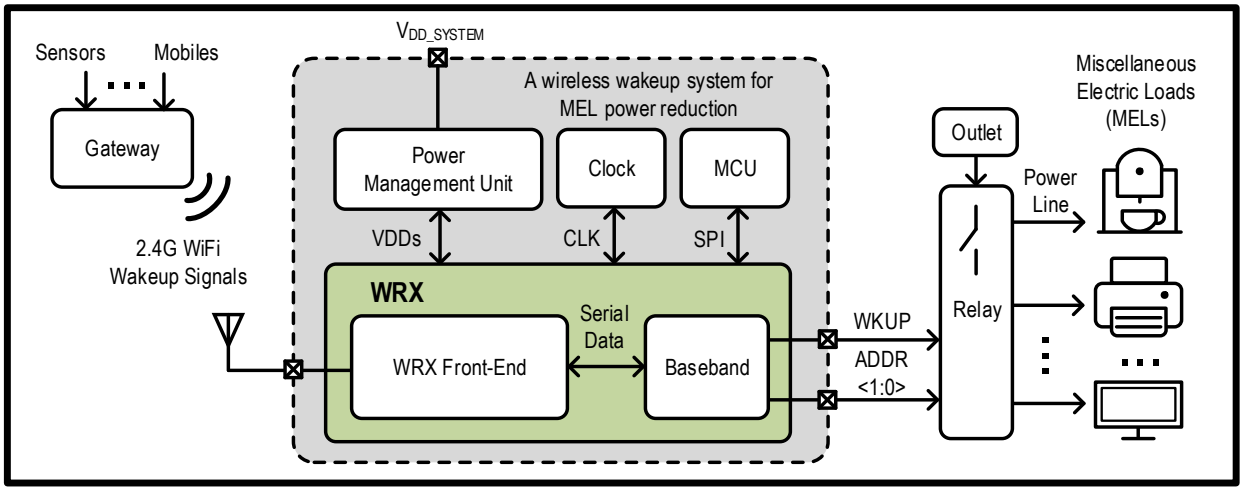


Figure 4.1 Block diagram of a smart switch system for controlling MELs.

wireless communication to manage active, standby, and non-active modes to save power further. However, a large portion of the MELs are comprised of consumer electronic devices, which are traditionally not focused on reducing energy consumption at the device-level.

This work aims to provide a solution to effectively control the power modes of MELs when they are being used and eliminate their phantom energy when they are turned off. As shown in Figure 4.1, a wireless wake-up and control system, which includes a wake-up receiver (WRX), a node controller and a duty-cycled RF transceiver, can be used to cut the power line of the MELs directly from the outlet power and reconnect them when they are needed by users, detected through sensors or mobiles. After power line connection, the control system should be able to manage the power modes of MELs according to different use cases.

Figure 4.2 shows the architecture of the traditional node controller, which is duty-cycled to save energy and can be woken up from a WRX. A traditional single-channel digital baseband is not suitable for the multiple appliance wake-up and management application. In this work, we improve the traditional architecture through the following four aspects. First, by making the digital circuits and SRAM work in the subthreshold region, a nW-level digital processing block, including a MCU and a correlation block, has been achieved. With such low power, we can make the controller work in an always-on mode and eliminate the need to wake up the MCU, which otherwise may consume significant energy and time to restore SRAM data when it powers on after being duty cycled off. Second, instead of one correlator, we integrate a 16-channel correlator to control up to 16 MELs and generate the address signals. Third, two clock domains

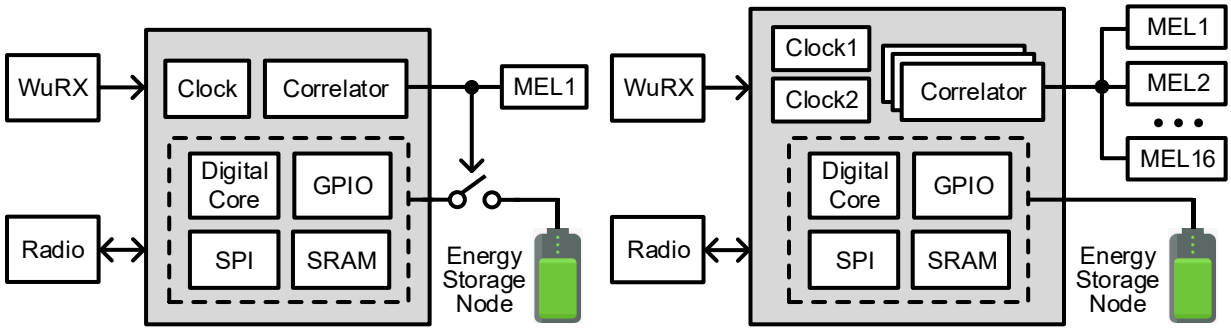


Figure 4.2 A traditional duty-cycled controller vs. proposed always-on controller with a multi-channel correlator and dual clock domains.

have been adopted for the correlator and MCU separately to save more power since the correlator clock frequency needs to match the WRX baseband frequency, which could be much higher than the digital processing frequency of the MCU for the MEL control application.

Fourth, to easily integrate with a WRX, the proposed SoC generates the voltage supplies, clocks, and Serial Peripheral Interface (SPI) for the WRX eliminating the need of extra components to make the WRX work.

4.1.2 802.11ba WRX

MELs consume significant power (~Watts) even when they are turned off, which the DoE calls phantom energy. One solution is to add a smart switch on every MELs device to cut power and wirelessly reconnect it when users are detected. The smart switch should connect over a wireless standard that is pervasive, such as WiFi. Power consumption of the smart switch will be dominated by the radio and should ideally be <1mW. This Chapter presents an ultra-low voltage (ULV) 578µW 802.11ba WiFi wakeup receiver (WRX) as a part of a 120VAC smart switch controller for reducing phantom energy consumed by MELs when in standby mode.

Recently, several receivers were proposed that operate in the sub-mW range with decent sensitivity performance [54, 41, 55, 23]. A mixer-first 99μW receiver provides decent sensitivity of -97dBm, however, rely on high-Q inductors for high impedance matching at the front and low power consumption on LC-VCO [41]. Some recent designs are pushing the voltage supply extremely low to improve power efficiency of transceivers and to enable operation from low voltage energy harvesters. A 0.3V ULV RX is reported with -94dBm sensitivity using coupled transformers and cascaded N-path filtering at IF [55]. The RX utilized low threshold voltage (LVT) devices to avoid sub-threshold operation and improve robustness across PVT. A 0.18V BLE RX is reported using quadrature outputs without any matching network [23]. Neither of these ULV receivers address RF frequency synthesis, which is particularly challenging at low voltage and low power.

In this Chapter, a complete system ULV 2.4GHz WiFi WRX is presented that operates from a single 0.2V supply associated with a sub-threshold, ultra-low power SoC. The receiver provides decent interferer rejection, and sensitivity that is comparable to state-of-the-art WiFi WRX.

The Chapter is organized as follows. The circuit implementation of 802.11ba ULV WRX is covered in Section II. Measured results of the receiver, and a comparison with prior art receivers are discussed in Section III. Finally, Section IV concludes the Chapter.

4.2 Ultra Low Voltage WRX Circuit Implementations

The primary circuit contributions of this WRX are 1) an ULV balun noise-cancelling LNA with step-up transformer; 2) an ULV FLL with 3rd-harmonic down-conversion to minimize current, and 3) a Q-enhanced RF gain stage for 1st-harmonic rejection. The WRX achieves a

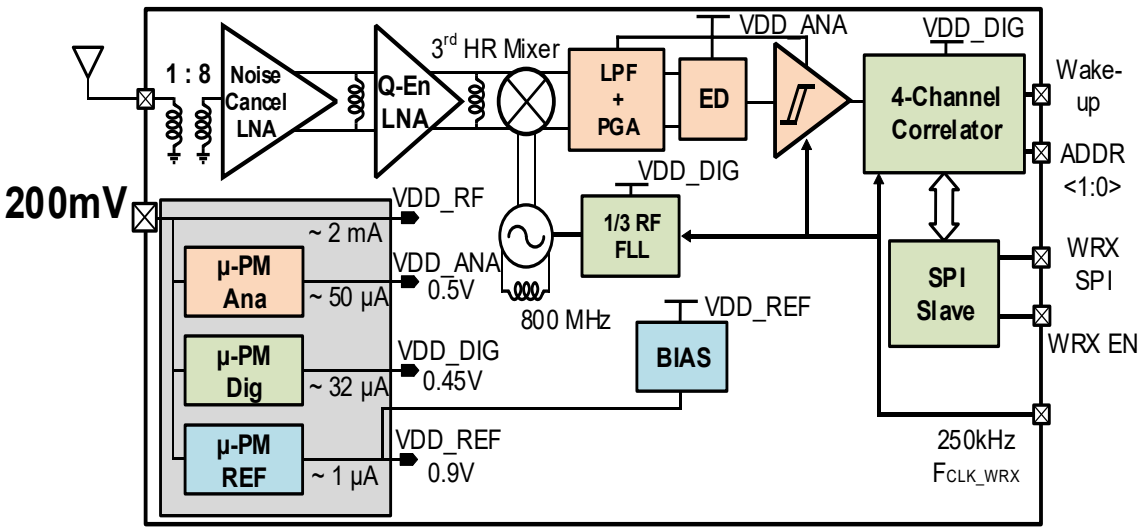


Figure 4.3 A ULV 802.11ba WiFi wake-up receiver (WRX).

sensitivity of -91.5dBm at 0.2V and 578µW by driving all high-current RF blocks directly from the 0.2V supply without any step-up in voltage. The WRX detects 802.11ba wake-up messages for future widespread adoption, low power, and low latency [47]. The data is modulated with ¼-rate Manchester-encoding and 4 multi-carrier on-off keying (MC-OOK) with 4µs symbol duration. A block diagram of the WRX is shown in Figure 4.3. The ULV LNAs, 3rd-harmonic mixer, and LO consume the highest currents, so they operate directly from the 0.2V supply. µPMs provide boosted regulated voltages for lower frequency analog and digital blocks to reduce power [23]. The 2-stage ULV narrowband LNAs are implemented before the 3rd-harmonic mixer to compensate for insertion loss on the mixer and reduce NF and to reduce both the required baseband gain and the load on the analog µPM. No off-chip component is used for the WRX, however, it receives baseband clock, and SPI signals from a companion ultra-low power SoC.

4.2.1 ULV RF Front-End

The narrowband LNA first RF front-end is chosen for providing extended range with improved total noise figure. Figure 4.4 shows the 1st-stage ULV pseudo-balun noise cancelling

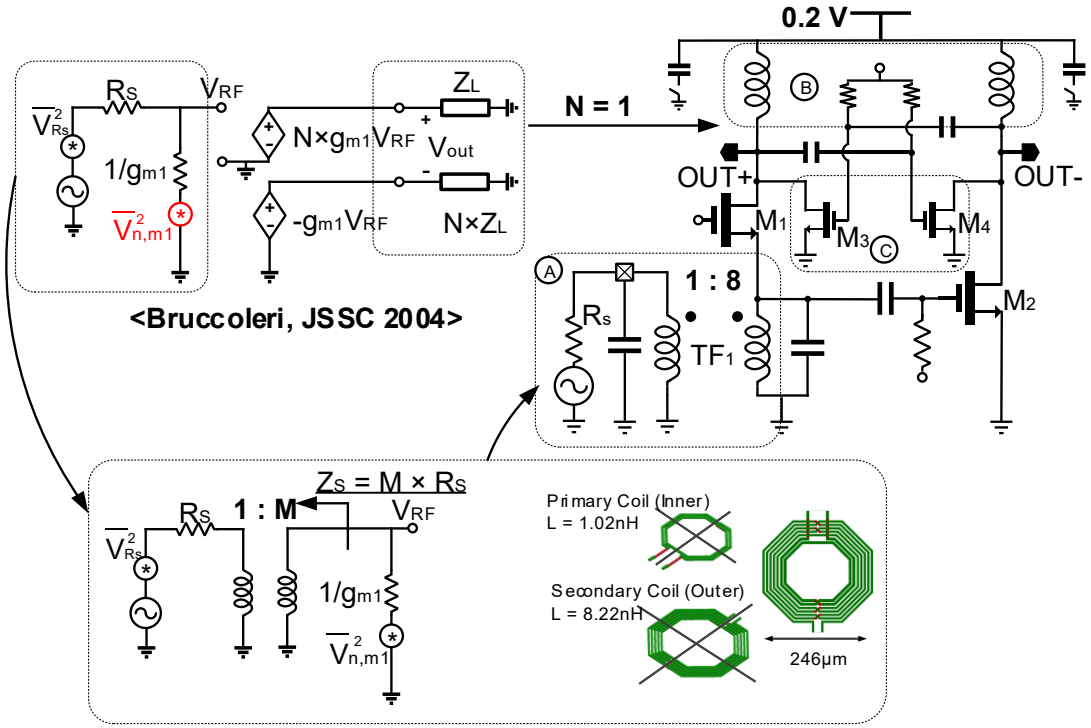


Figure 4.4 The ultra-low voltage (ULV) pseudo-balun noise cancelling LNA, 1:8 step-up transformer, and measured S11 result.

LNA. Similar to the wideband noise cancelling balun LNA in [56], the LNA cancels noise on M1 when the input of the LNA is matched to a 50Ω terminal. However, in [56] M1 must be biased with sufficient current so that 1/gm1 equals 50Ω, thereby cancelling the M1 noise. Our design introduces 3 techniques to cancel noise, reduce voltage, and save power, noted A-C in Figure 4.4. A) A high-turn step-up transformer is inserted between the 50Ω source and the CG-CS LNA input to boost the input impedance by the step-up radio, M, reducing the bias current of the CG amplifier required to cancel M1 noise. From HFSS simulations, the 1:8 step-up transformer has a 1.02nH primary coil (inner ring) and 8.22nH secondary coil (outer ring), a k-factor of 0.62, and Q of 12.3, providing 7dB of voltage gain. B) Stacked active devices are switched into a differential inductor so the LNA can operate with low headroom and still ensure robust operation across PVT ($V_{DS,M1} > V_{GS,M1} - V_{TH} > 0$). This provides high current efficiency that leads to low active power. The

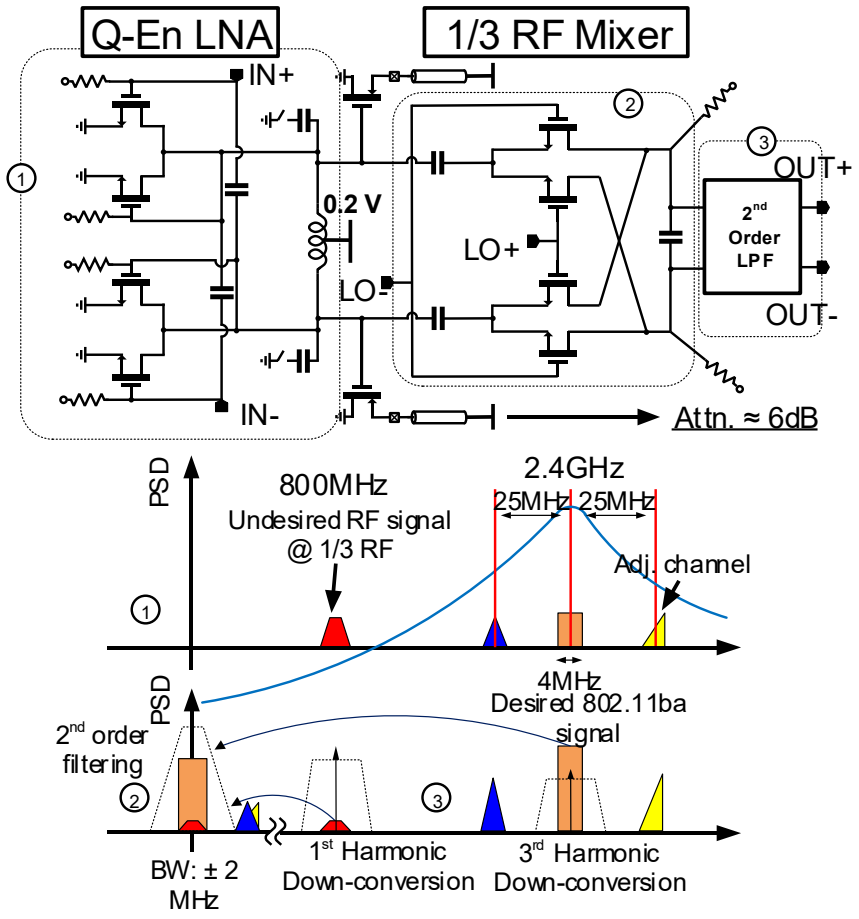


Figure 4.5 Q-enhancement 2nd stage LNA, and 3rd-Harmonic Mixer (top), and frequency plan (bottom).

impact of noise cancellation is maximized as the transistor ratio N increases, but our design uses N=1 for simplicity and passive load matching. C) Lastly, M3 and M4 are cross coupled to provide Q-enhancement gain before the mixer with a moderate 1dB impact on overall NF.

A 3rd-harmonic mixer is used to reduce the required LO frequency by 3x, also reducing power primarily of the LO divider and buffers in the FLL. However, the single phase 3rd harmonic mixing can introduce an interferer from the unwanted fundamental spur that down converts to the demodulation path. The frequency planning for the WRX is shown in Figure 4.5, with 1-3 noted on the schematic and PSD plot to indicate frequency content at the different stages. 1) The 4MHz wide 802.11ba signal is located in the 2.4GHz band, and unwanted adjacent channels are located

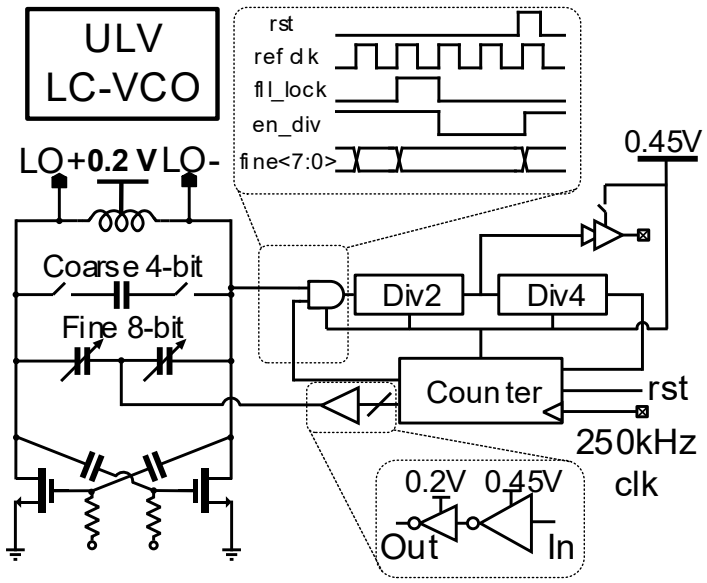


Figure 4.6 ULV LC-VCO integrated frequency locked loop.

25MHz apart from the desired signal. The RF gain stages provide gain in the desired band before the 3rd-harmonic down-conversion mixer. A high order RF filter is needed to attenuate signals at the 800MHz LO fundamental, since the mixer also down-converts from this band. The filtering is done by the Q-enhanced LNA, which is inserted primarily to enhance the selectivity of the RF gain stages. 2) The undesired signal at ⅓ RF is attenuated before 3rd-harmonic down-conversion. 3) The baseband signal is filtered by a feed-forward 2nd-order low-pass filter (LPF) with a cut-off frequency of 2MHz, followed by a baseband gain stage.

4.2.2 ULV 1/3 RF Local Oscillator

The RF LO is an ULV LC-VCO with a counter-based FLL controller that is locking the frequency to a 250kHz clock reference from the external node controller (Figure 4.6). The center frequency of the ULV LC-VCO is chosen to operate around 800MHz primarily to reduce the power of the LO digital buffers and FLL counter that reduces the current requirements from the micro power manager, thus leads to lower active power. The 4-bit coarse frequency control of the

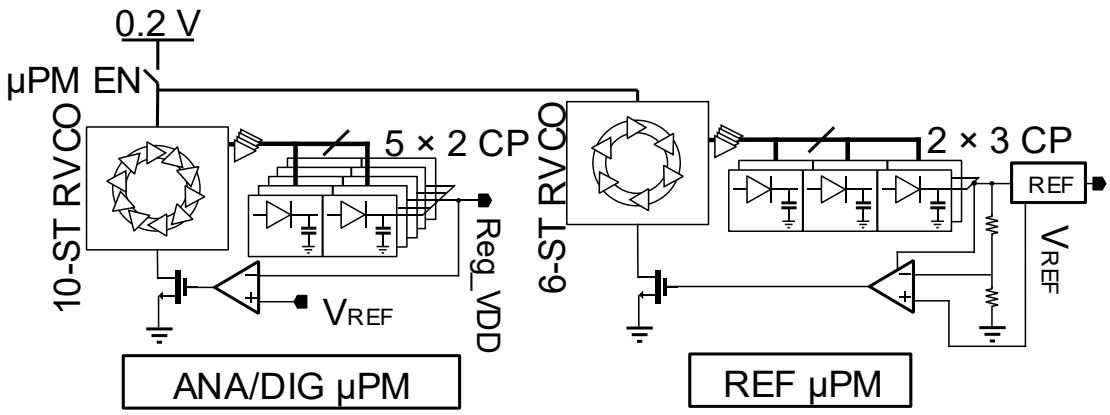


Figure 4.7 5 by 2 charge-pump micro-power manager for ULP analog/digital domain, and 2 by 3 charge-pump micro-power manager for reference domain [24].

ULV LC-VCO is implemented with MOM capacitors and a switch powered at 0.5V from the analog μPM that has a frequency resolution of 25MHz at the 3rd-harmonic frequency. For low-noise fine control, the 8-bit fine frequency tuning is done by varactors whose voltage is controlled by 0.2V inverters, and covers 40MHz range at the 3rd-harmonic frequency. The total current of

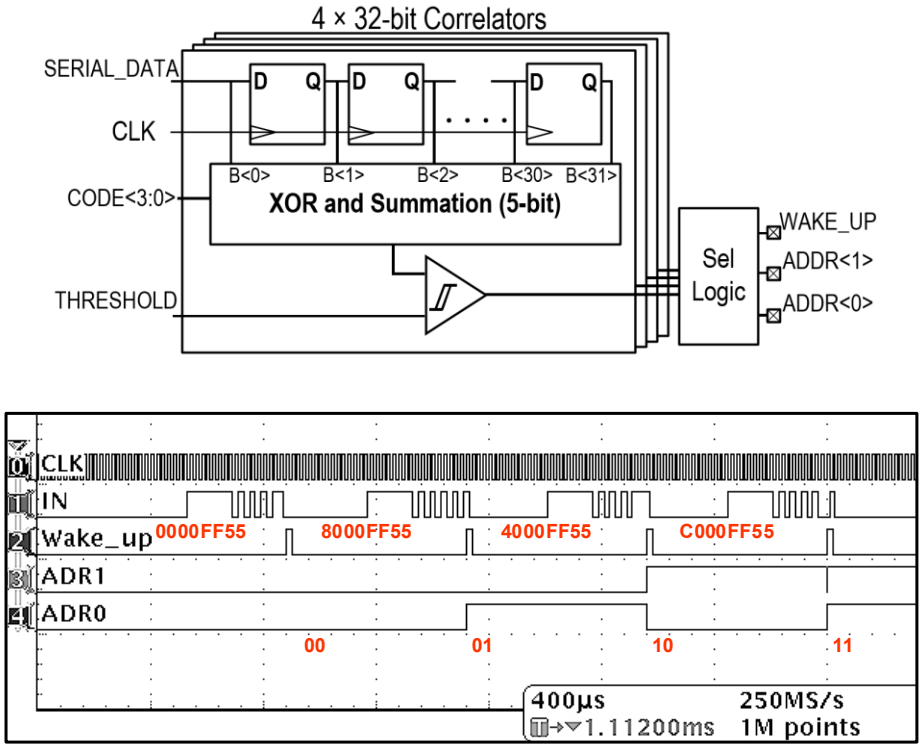


Figure 4.8 Measured wake-up signals for the first 4 channels of the correlator.

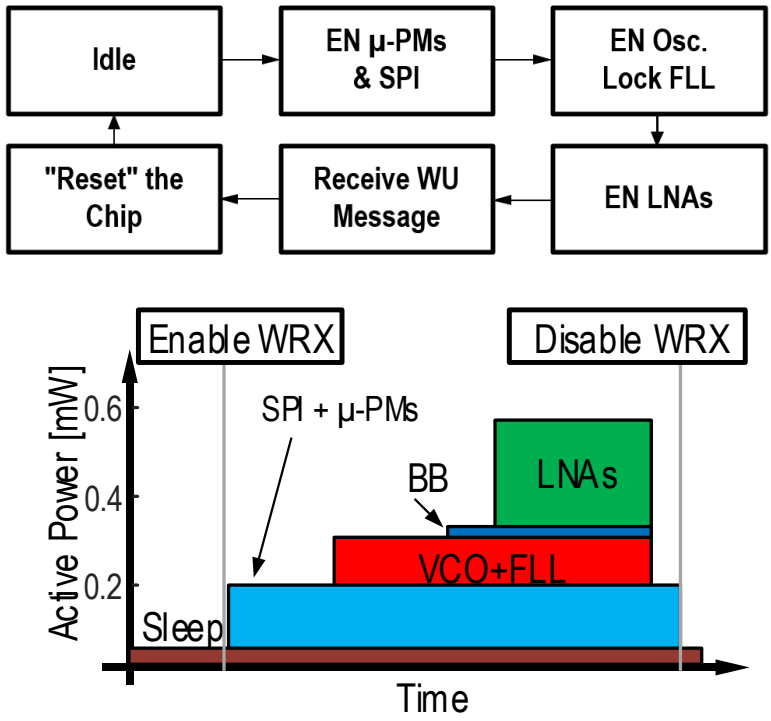


Figure 4.9 Diagram and transient operation of duty-cycled WiFi wake-up receiver, 4-channel correlator, and micro power managers (µPM).

the FLL is only 28µA. When lock is detected by the FLL controller, the counter disables the divider path and freezes the fine codewords to save power, until it is reset by the system.

4.2.3 Micro Power Managers

Micro power managers regulate a low voltage supply by using a bootstrapped inverter to drive a charge pump which operates active devices in the ULV domain in saturation mode with the help of ultra-low power bias circuits [23]. Higher voltages can be also useful for fast digital circuits such as the FLL that is very unstable in the sub-threshold voltage regime. By aggregating more phases, the charge pump can load more current on the output load. The series connection of charge pumps increases the output voltage, however, these are significantly current starved. Likewise, parallel charge pumps produce higher currents at lower voltages. The current capacity

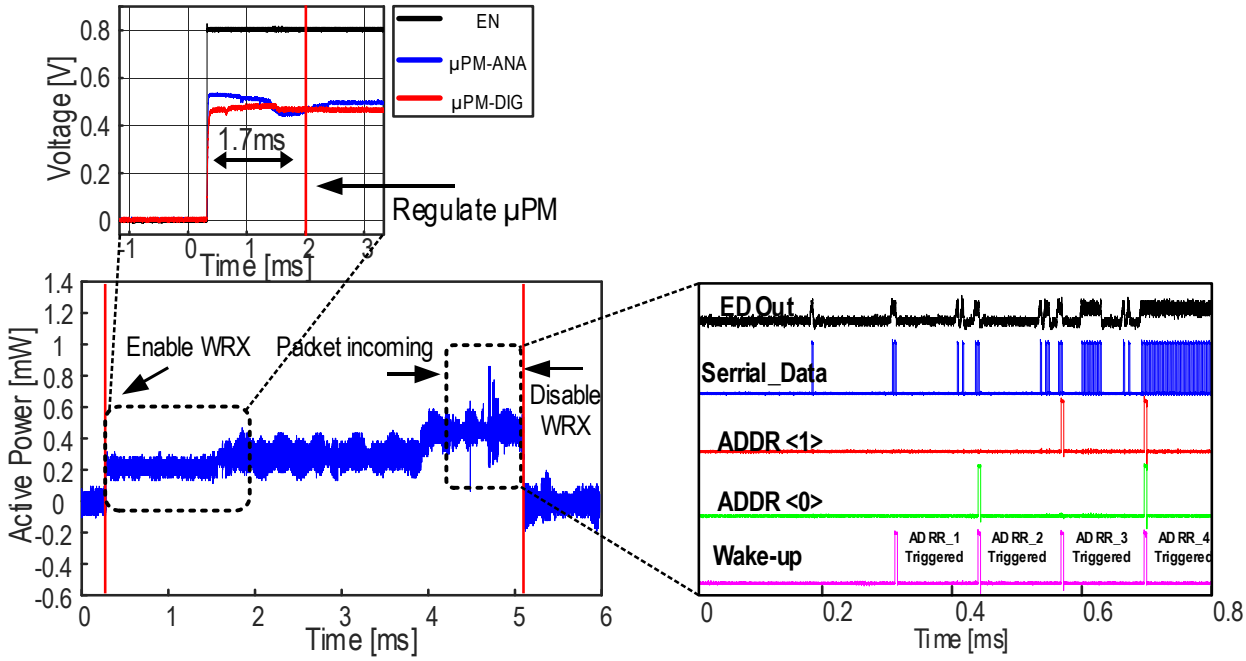


Figure 4.10 Diagram and transient operation of duty-cycled WiFi wake-up receiver, 4-channel correlator, and micro power managers (µPM).

of the micro-power manager is limited, and the efficiency degrades rapidly as current handling is increased. Therefore, they are not used for power hungry RF blocks.

The number of stages (phases) of bootstrapped Ring VCO, and the combination of charge pumps for each micro power manager was chosen based on its required current consumption for the block it is driving. For digital and baseband analog power domains, as shown in Figure 4.7, the micro-power managers are composed of 5 (parallel) by 2 (series) charge pumps that aggregates 10 phases. For reference, micro-power manager that provides a reference voltage to the other micro-power managers, is comprised of 3 by 2 charge pumps.

4.2.4 Energy Detection, and Wake-Up Detection Stages

After the baseband gain stage, a pseudo differential energy detection is inserted before dynamic comparator for bit decision followed by a wake-up detection digital block. Four parallel

32-bit correlators are inserted, and used to trigger wake-ups from desired addresses. With external 250kHz clock given by the node-controlling SoC.

The rest of the WRX is controlled using a SPI-slave. Figure 4.8 illustrates the operation of duty-cycled WRX. When initially enabled, the µPMs turn on and power the SPI in the WRX. The WRX is then configured through SPI, and RF and analog blocks are enabled. When a correlator triggers wake-up from a programmed address, an interrupt is asserted, and the WRX is externally placed back in the idle state. The measured transient operation of WRX is shown in Figure 4.10. This entire power-up sequence takes <5ms, and the latency of a single channel wake-up is 128µs.

4.3 Measured Results

4.3.1 Measured Results of 802.11ba WRX

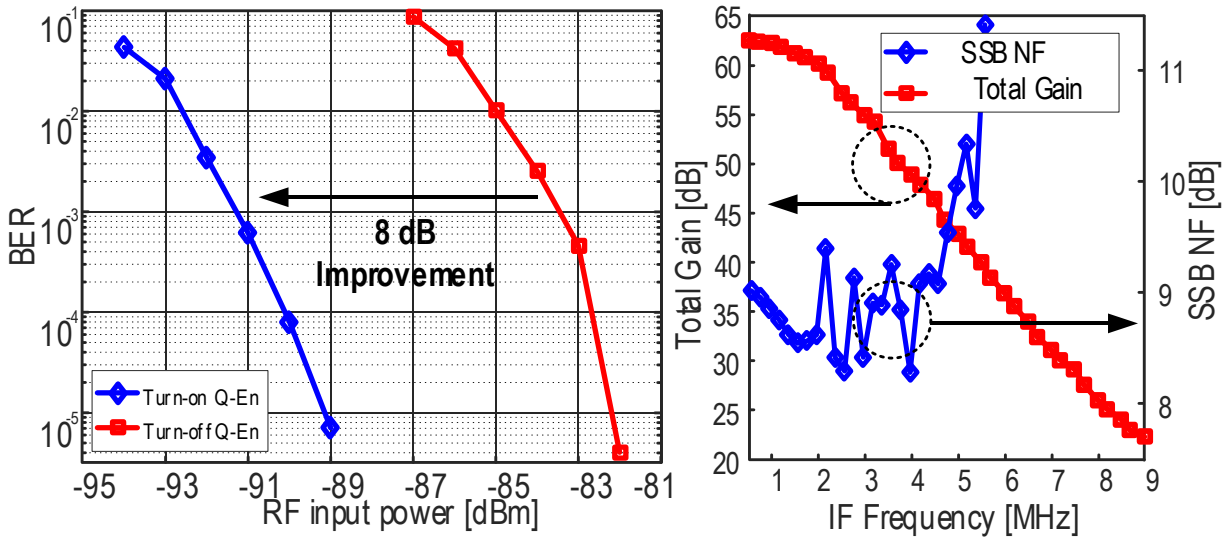


Figure 4.11 Bit error rate (BER) waterfall curve plot (left), and single side band noise figure (NF) , and total gain from PGA buffer output plot (right).

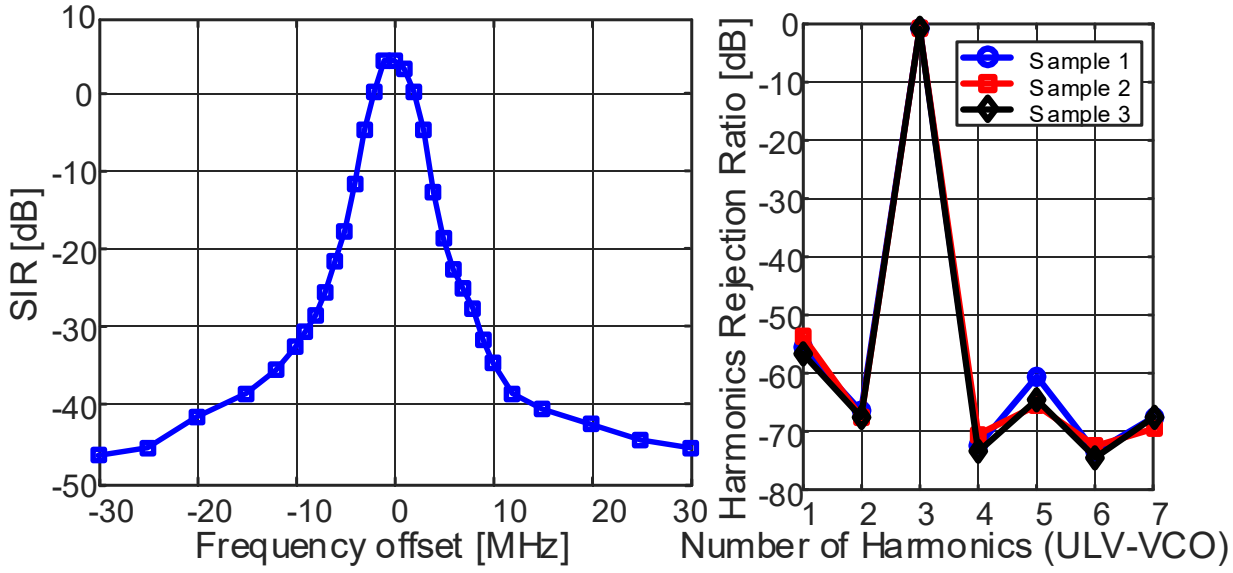


Figure 4.13 Signal to interferer ratio plot (left), and the plot of RF harmonic rejection ratio at IF LPF output vs. number of harmonics of ULV-VCO.

The ULV WiFi WRX was fabricated in 40nm CMOS. Measured results are shown in Figure 4.11, Figure 4.13, and Figure 4.10. The WRX achieves -91.5dBm sensitivity at a BER of 10-3 and data-rate of 62.5kbps while consuming 578µW. The Q-enhancement LNA improved the sensitivity of the WRX by 8dB. The measured IIP3 of the RF front-end was -18dBm with 5 and 10MHz two-tone spacing.

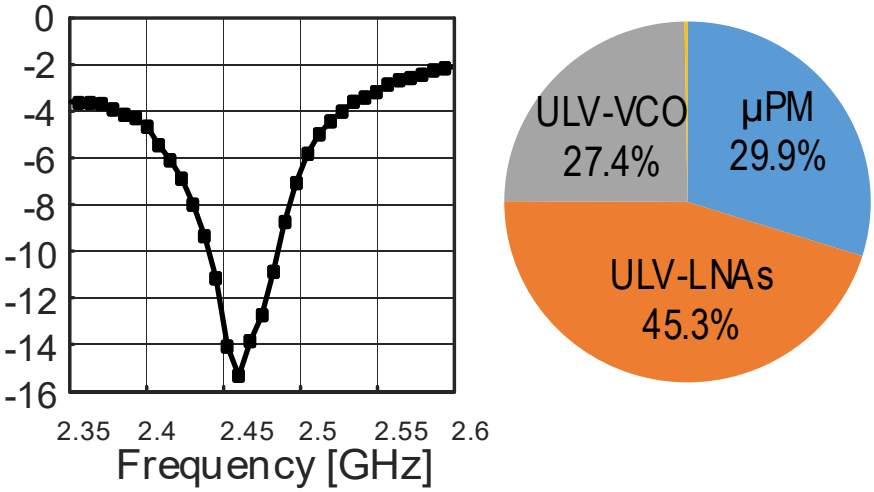


Figure 4.12 S11 plot (left), and power breakdown of ULV WRX.

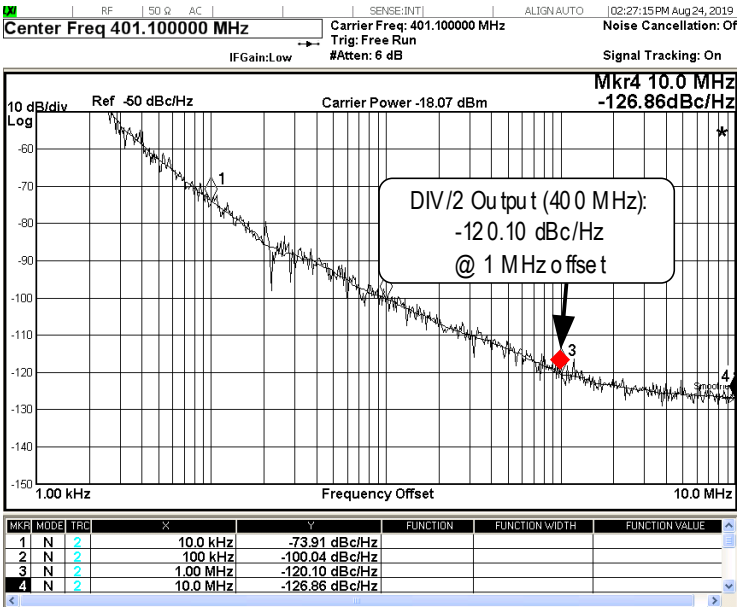


Figure 4.14 Diagram and transient operation of duty-cycled WiFi wake-up receiver, 4-channel correlator, and micro power managers (µPM).

The WRX has no direct access to the VCO core. Instead, the output of the divider is measured and has a phase noise of -120.1dBc/Hz at 1MHz offset, which implies the VCO achieves <-100dBc/Hz at 1MHz offset at 2.4GHz according to simulations. The SIR of the 1st-adjacent channel (25MHz) is -45dB. The worst recorded harmonic rejection ratio from measurements of three chips was -52dB. The overall single sideband NF is 8.7dB. The S11 is <-10dB (Figure 4.12), and no external matching was required to provide noise cancellation in the ULV-LNA. A breakdown of power is shown in Figure 4.12, along with comparison to state-of-the-art. Compared to prior work, this design achieved the lowest voltage among WRXs and best NF among prior WiFi WRXs.

4.3.2 MELs System Demonstration

To show the proposed SoC can be integrated into a wireless system and work successfully with a WRX, we connect the SoC with a WiFi-based WRX chip, whose set-up is shown in Figure 4.15. The two LDOs provide 0.2 V and 0.4 V for the WRX, and the clock frequency of the correlator is set to be 50 kHz. The WRX is fully powered by the controller including the voltage supplies, the clock, and the SPI for control-bit configuration. A wake-up signal is shown in Figure 4.16 which proves that the SoC can fully integrate with a WRX.

Table 4.1 Performance summary and comparison to prior art receivers

Parameters	ISSCC'15[3]	ISSCC'13 [4]	ISSCC'17 [5]		RFIC'19 [2]	This Work
CMOS Technology	65nm	65nm	28nm		28nm	40nm
Frequency [GHz]	2.4	2.4	2.4		2.4	2.4
Applications	Non-Standard	Non-Standard	BLE		802.11ba	802.11ba
Features	Dual-IF Multi N Path Filter	Transformer Coupling + Folded CGLNA + Cascode Gm-Boosting + N Path Filter	Power-Gating LNA + ULV Class-D VCO + Passive I/Q Gen. + Micropower Manager		Mixer-embedded Dynamic Baseband LNA + Micro LDOs	ULV Noise Cancelling Narrowband Balun LNA + Q-Enhaced LNA + ULV FLL & 3H.R. Mixer + Micropower Manager
External Components	2 inductors + off-chip frequency calibration	1 inductor + 2 caps + LO for injection locking	LO for injection locking		32.768kHz RTC	250kHz clock from node controller
Supply Voltage [V]	0.5	0.3	0.18	0.3	1.1[1] (0.6/0.9)	0.2
Active Power [μW]	99	1600	382	1305	495 / 667[2]	578
Noise Figure	N/R	6.1	11.3[3]	8.8[3]	11	8.7
Modulation	OOK	BFSK	GFSK		MC-OOK	MC-OOK
Sensitivity [dBm]	-97/-92	-94	N/A		-92.6	-91.5[4]
Data Rate [kbps]	10/50	200[5]	N/A		62.5[6]	62.5[6]/250
SIR[7] [dB]	-25/-22[8]	-30[9]	N/A		-57	-45
DBB Integration	No	No	No		Yes	Yes
Active area [mm^2]	0.0576	2.496	1.65		0.13	0.681

1. On-chip μ-LDO regulates 0.6/0.9V.
2. 495μW for standalone, 667μW with WiFi system supply.
3. Double sideband noise figure.
4. When data-rate is 62.kbps
5. *Psens.* = -91.5dBm at this data-rate.
6. Standard chip-rate, ¼ Manchester-coded.
7. SIR of 1st adjacent channel, 25MHz for 802.11ba.
8. CIR at 1MHz offset frequency.
9. CIR at 3MHz offset frequency.

The final goal of this work is to use the on-chip correlator and MCU to wake up the MELs, to control their different power modes, and to cut off the power line when the MELs are turned-off.

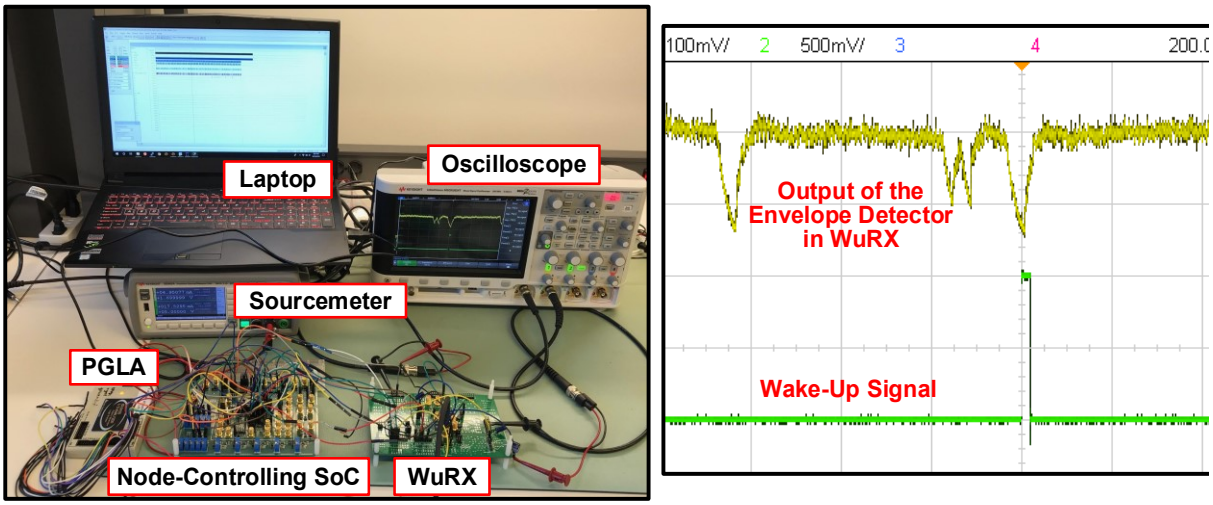


Figure 4.15 Experimental set-up of the controlling SoC with a WRX and measured wake-up signal for the wake-up and controlling system.

Figure 4.16 shows a state transition diagram of the control program running on the MCU. When there is a wake-up signal, it wakes up the MEL to make it to work in active mode, and then go to the standby mode indicated by the busy signal. There is a 3-bit input from the RF transceiver to changethe power mode of the MEL based on the user need. If there is no input, then the MEL goes from standby, to non-active, and finally to cut-off mode after two timers.

To demonstrate this function, we use a Link Instruments IO3200 pattern generator to simulate the input from RF transceiver and wake-up data from WRX in the experimental set-up. Figure 4.16 shows a power-mode control case, where a MEL wakes up from the correlator and finally goes back to the cut-off mode. After a wake-up is detected for the MEL, the MEL state changes from cut-off to active, and the busy indicator is on. After finishing all the tasks, the MEL goes to cut-off again. This application demonstration successfully shows that the node-controlling SoC can control the power modes of the MEL to reduce average power and eliminate its phantom energy.

4.4 Conclusion

A standalone 0.2V 578μW ultra-low voltage (ULV) 2.4GHz 802.11ba WiFi wake-up receiver (WRX) is presented. The ULV techniques include operating current-hungry RF blocks directly from the 0.2V supply and leveraging passives for noise-canceling and Q-enhancement. The WRX achieves -91.5dBm sensitivity at 10-3 BER and data-rate of 62.5kbps, while rejecting

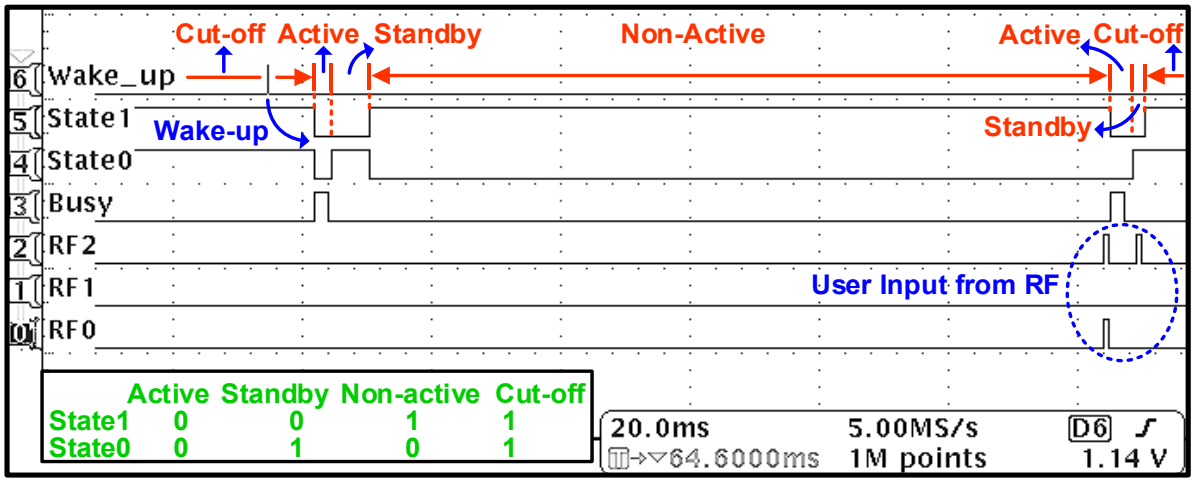
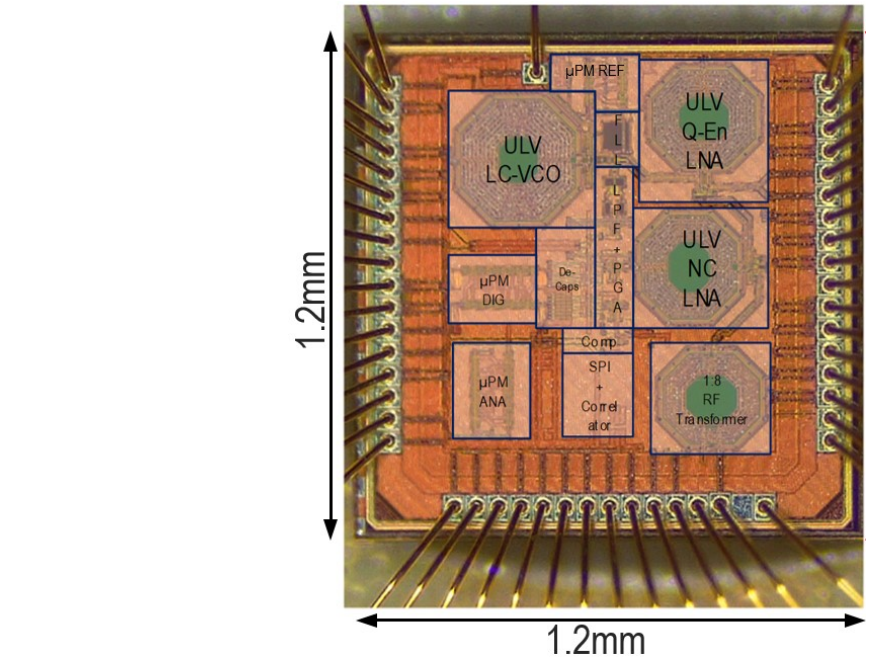
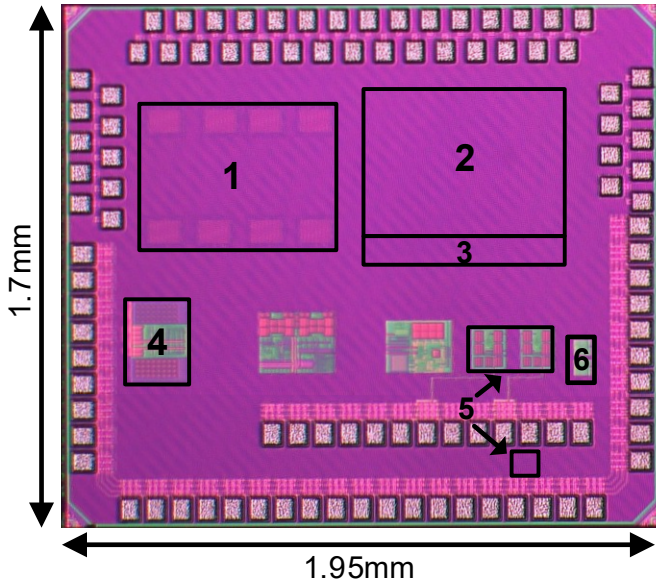


Figure 4.16 Measured transient waveform showing the MEL power-mode control.

45dB of adjacent blocker with only 0.2V supply. The WRX includes an energy-efficient 5ms startup sequence which interfaces to an external node controller.





Components	Area (mm^2)
1. SRAM	0.29
2. Digital core and IOs	0.36
3. Correlation	0.045
4. Buck converter	0.05
5. LDOs	0.044
6. Clocks	0.007
Total	0.796

Figure 4.17 Photograph of WRX chip (top), and Node-controlling SoC (bottom).

Chapter 5 A 62-69GHz Crystal-Less Transceiver with 12 Channels Tuned by a Transmission-Line-Referenced FLL in 0.13µm Bi-CMOS

5.1 Introduction

The progress towards smaller WSNs has opened the possibility of ubiquitous sensing applications, such as body area networks. However, the minimum form-factor of a WSN is limited due to bulky off-chip components, mainly the crystal reference and antenna for wireless data transfer. Recently, several prior works have focused on removing the off-chip frequency reference from the node [1, 2, 3]. Some rely on a base station signal to compensate for frequency drift [2], or send uncalibrated RF data to a high quality base station (software defined radio), obligating it to synchronize to the node's RF signal. The other disadvantage of these prior work is that it isn't applicable in dense active network areas. In addition, up to recently, no pure node-to-node communication has been demonstrated at >1GHz without an external reference. This chapter proposes a crystal-less wireless transceiver (TRx) that uses an integrated transmission-line to lock and tune the RF frequency across non-overlapping 12 channels that is applicable for wirelessly dense environments, while also enabling node-to-node communications. The integrated 3-port slot antenna supports transmission (Tx) and reception (Rx) modes without a TRx switch. The on-off keyed (OOK) based uncertain IF TRx architecture enables node-to-node communication with 16dB channel selectivity, without requiring an external reference.

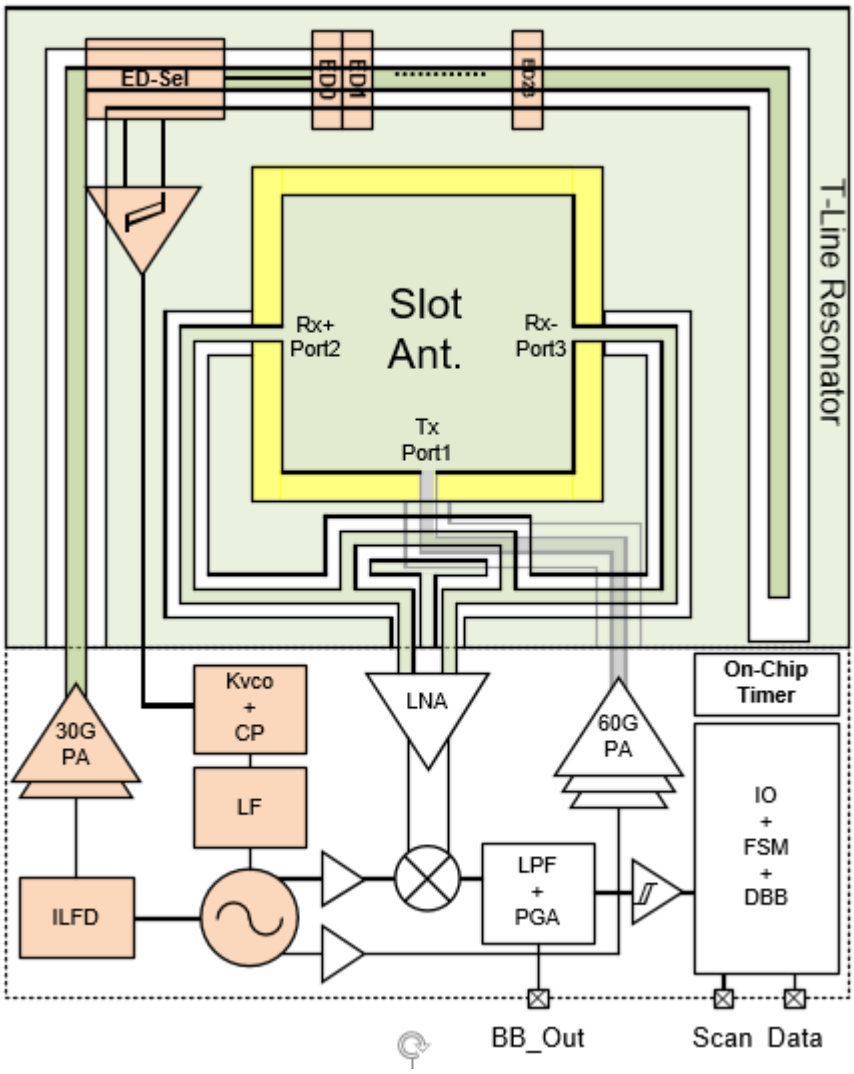


Figure 5.1 System block diagram of crystal-less transceiver.

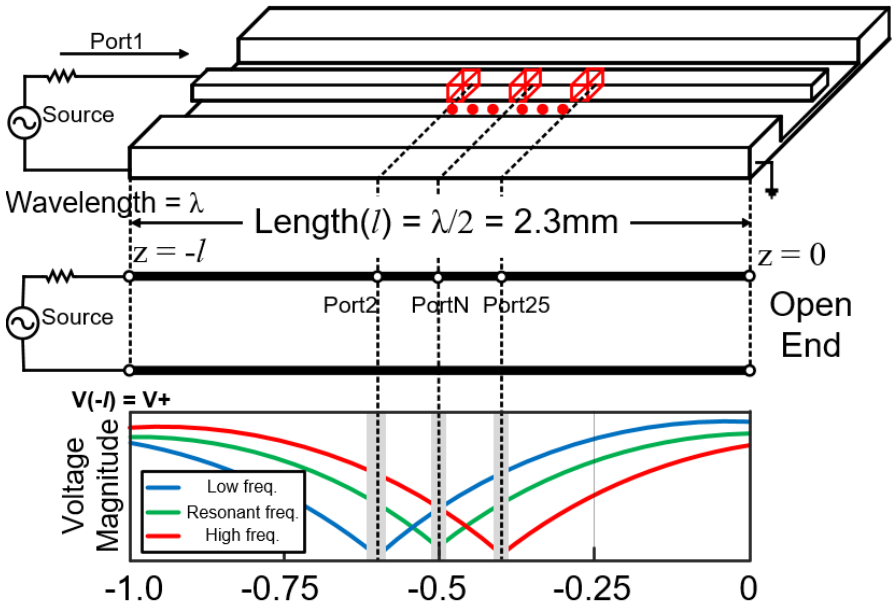
5.2 12-Channel 60GHz Crystal-Less Transceiver

The transceiver has two key components integrated on-chip that reduce the from-factor of the system: fully-integrated T-line reference and slot antenna. The system block diagram of the multichannel crystal-less transceiver is shown in Figure 5.1, featuring the on-chip T-line resonator and the slot antenna. The on-chip T-line resonator is used as an on-chip reference that helps transceiver system not rely on bulky off-chip reference, and also supports multiple channel from 62GHz to 69GHz. On-chip slot loop antenna that supports both transmission (Tx) and reception

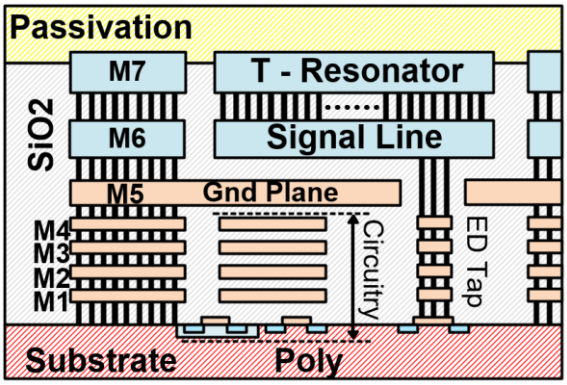
(Rx) modes by utilizing the orthogonality of the square shaped slot-loop [4]. The following sections will cover detail descriptions of the system.

5.2.1 On-chip T-Line Based Frequency Locked Loop

The on-chip T-line-based FLL provides a multi-channel LO from 60GHz to 67GHz, locked to the geometry of the T-line. The dimensions of the T-line can be precisely controlled on-chip due to the advanced CMOS manufacturing, therefore the variation across multiple chips is expected to be low. The basic concept of the on-chip reference relies on the voltage distribution of the standing wave in an open-ended λ/2 T-line. Prior art provides an on-chip reference utilizing a patch antenna that also utilizes the standing wave pattern on the antenna, however, undesired radiation during frequency locking is inevitable, and it only supports a single carrier frequency [58]. In this work, the resonance frequency of the T-line is chosen to be at 30 GHz (½ of the RF operating frequency) in order to minimize the coupling between T-line and TRx. As shown in Figure 5.2(a), the T-line resonator exhibits a standing wave pattern at the resonance frequency (LTL=λ/2 or λ/4). For an open ended λ/2 resonator, the standing wave forms a null region near the center of the T-line if the source frequency is equal to the resonance frequency. The null location shifts based on the source frequency relative to the resonance frequency as depicted in the figure. The frequency locking mechanism is achieved by inserting several voltage taps along the T-line to detect the profile of the standing wave near the center, and then regulating LO frequency-divided-2 in a feedback loop to drive the standing wave null to the x-location corresponding to the desired frequency. As can be seen in the Figure 5.3, 24 ED input taps show different voltage



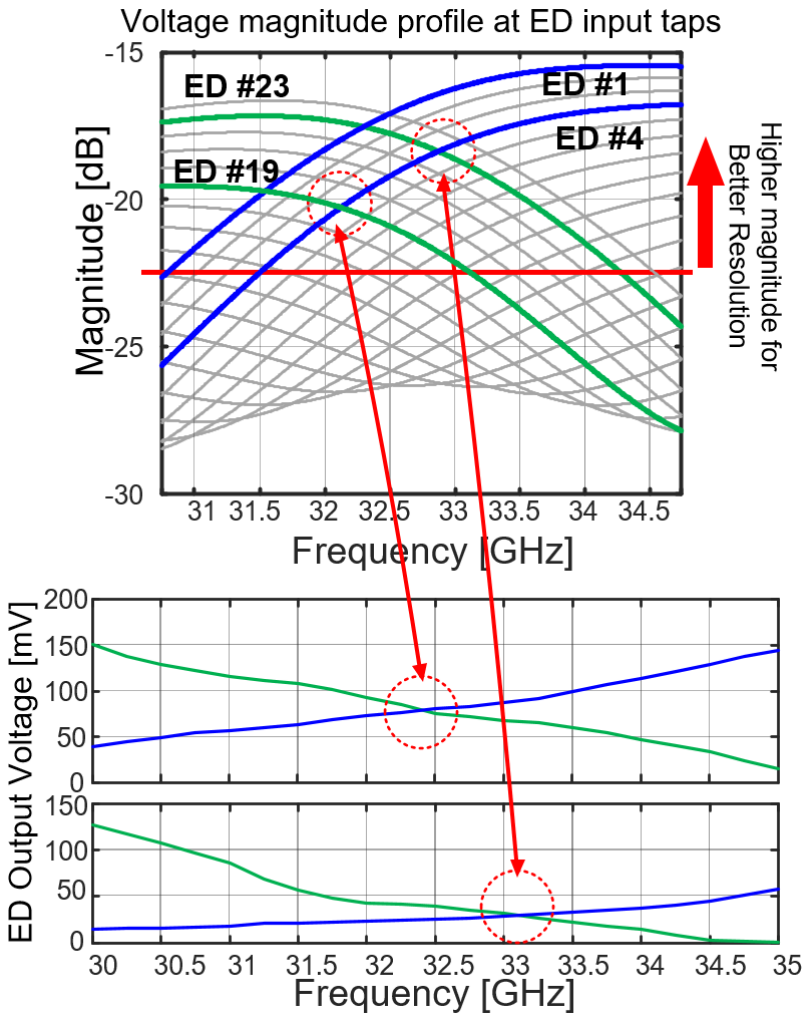
(a)



(b)

Figure 5.2 (a) Conceptual diagram of multiple band frequency locking on-chip reference. (b) Cross-view of on-chip reference circuitry, and physical implementation including T-line resonator, ED taps, FLL active circuitries.

profiles across frequency. Each combination of ED pair intersects around a frequency of interest that regulates the LO frequency close to it by the FLL. For example, if ED tap 19 and 4 are selected, the LO frequency-divided by-2 will be regulate to the frequency where their voltage profile



ED Pair	Interception Freq. (Simulation)	Interception Freq. (Measured)	Frequency Error (MHz/%)
1,16	30.96 GHz	30.25 GHz	710 MHz / 2.4%
1,18	31.39 GHz	30.85 GHz	540 MHz / 1.8%
1,20	31.72 GHz	31.25 GHz	470 MHz / 1.6%
1,22	32.11 GHz	32.05 GHz	60 MHz / 0.2%
24,1	32.48 GHz	32.5 GHz	-20 MHz /-0.01%
24,3	32.86 GHz	33.25 GHz	-110 MHz / -0.4%
24,5	33.27 GHz	33.75 GHz	-480 MHz / -1.6%
24,7	33.63 GHz	34.15 GHz	-520 MHz / -1.7%
24,9	34.00 GHz	34.45 GHz	-450 MHz / -1.5%

Meas. lock frequency deviates more from center

Figure 5.3 Simulated voltage magnitude profile on ED input taps over frequency (top), measured interception frequencies from measured ED output (middle), and the simulation vs. measurement interception frequency comparison (bottom).

intersects around 32.2GHz. For better frequency resolution the pair that has high voltage

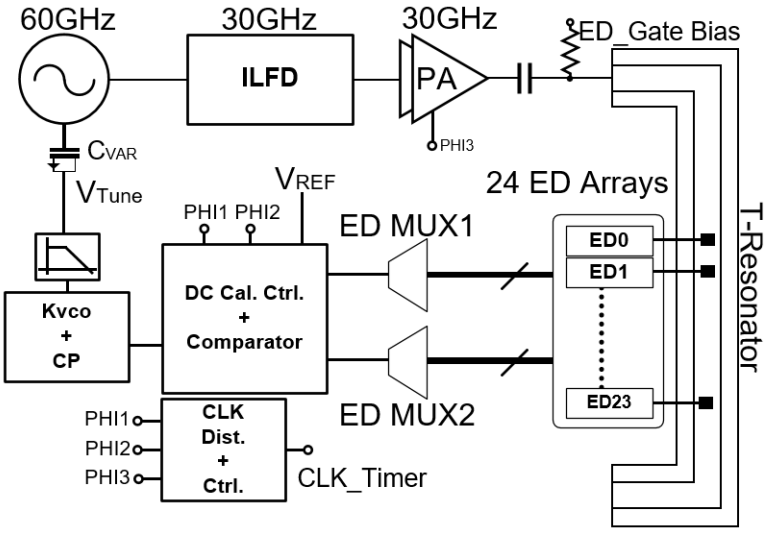
magnitude intercept point has been chosen for tuning each frequency of interest. The T-line based resonator is shielded with a ground plane resulting in a simulated 60dB attenuation in the radiated power from the T-line. As can be seen in the comparison table on the bottom of Figure 5.3, the measured interception frequency shows frequency deviation from the center channel frequency comparing to the simulated interception frequency that can be interpreted due to the loss factor of the T-line resonator.

Chip-to-chip frequency accuracy of the on-chip frequency reference is a critical factor of crystal-less TRx operation, especially from node to node. To minimize variation of the T-line reference across multiple chips, several requirements need to be addressed. First, the resonator has to be stable enough over process variation. Also, the loss of the T-line has to be minimized to avoid process-dependent attenuation along the path which leads to frequency locking inaccuracy. Finally, a large input voltage to the ED array is required to overcome the process-dependent distortion and offset in the active circuits and comparator. As shown in Figure 5.2(b), the resonator was designed using the top two metal layers (M6, M7) to provide low metal sheet resistance for minimizing signal attenuation along the T-line. The ground plane is drawn in M4, and area beneath reused for active circuits, which reduces the circuit layout complexity and mismatch. According to measurements, the input impedance of the resonator was 148Ω at its impedance peak around 32GHz with less than 10% variation across the band.

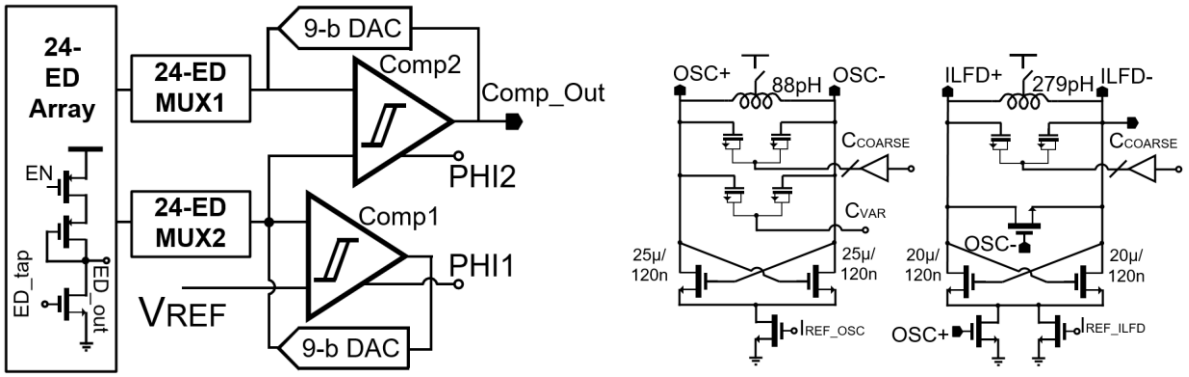
The system block diagram of the proposed FLL is shown in Figure 5.4(a). For circuit simplicity, and optimizing active area beneath ground plane of T-line resonator, a pair of ED mux have been implemented that can make an arbitrary comparison between any 2 ED from a 24 ED array. However, the route asymmetry of each ED taps, and process variation on active device FLL circuitry causes DC offsets which leads to deterioration in chip-to-chip frequency accuracy. For

minimizing the variance of the chip-to-chip frequency resolution, the proposed FLL digitally calibrates the DC offset before the comparison phase for frequency locking. The ED pair calibration circuitry is depicted in Figure 5.4(b). Each ED pair calibrates its common mode voltage to V_{REF} for its optimized gain performance while minimizing the DC offsets from each comparator and ED pair by feedback current DACs that were calibrated precisely by the feedback 9-bit current DAC with <1mV of 1LSB. For mm-Wave circuit implementations, BJTs or MOSFETs were used selectively considering the performance requirements on each block. For the VCO, and injection-locked frequency divider (ILFD), shown in Figure 5.4(c), NFETs were used due to its high process

accuracy despite its low gain efficiency comparing to BJTs. For high gain intermediate buffer stages, BJTs were preferred, however, an NFET driver is been used for the 30GHz FLL PA output that interfaced with the T-resonator to optimize the frequency accuracy.



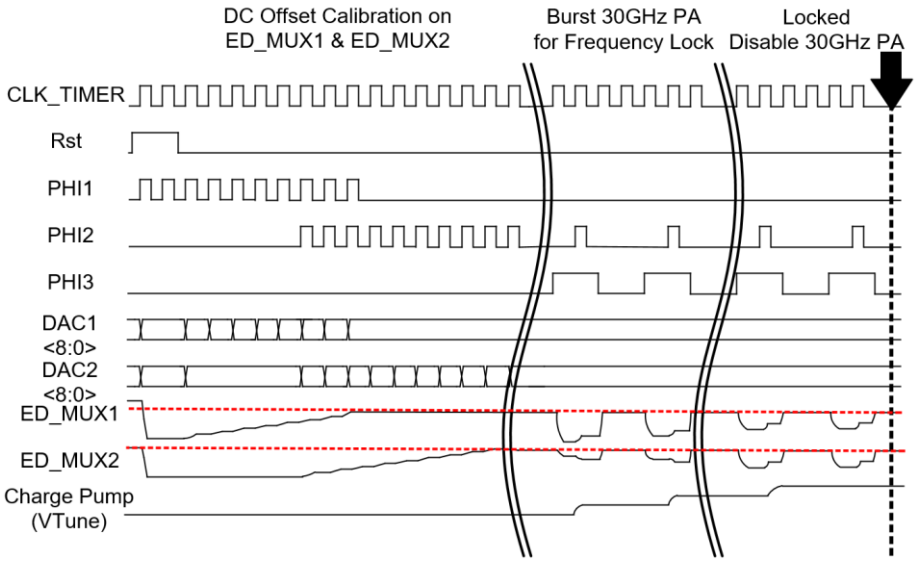
(a)



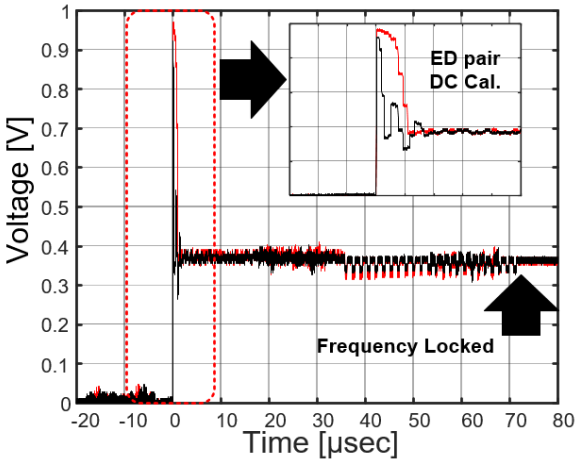
(b) (c)

Figure 5.4 (a) System block diagram of on-chip reference based frequency locked loop. (b) Detail circuitry of power detection, DC calibration, and comparison blocks. (c) mm-Wave oscillator and injection locked frequency divider (ILFD).

The detailed sequence of the FLL operation is shown in Figure 5.5(a). First, the selected ED pairs are calibrated sequentially. The ED selected by MUX2 is calibrated first, followed by MUX1 to minimize the DC offsets. Then, the 60GHz VCO and the injection-locked frequency divider (ILFD) are enabled. The ILFD signal is buffered, and applied to the resonator through the



(a)



(b)

Figure 5.5 (a) Timing diagram of FLL. (b) Measured FLL behavior on ED output in transient domain.

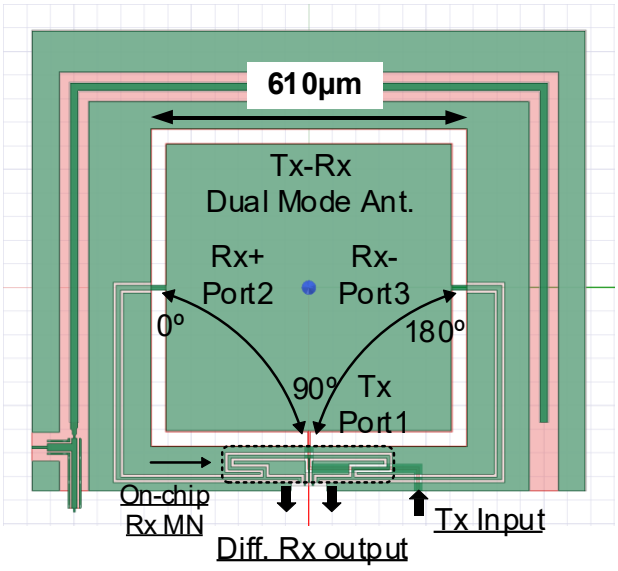
30GHz PA that is duty-cycled by PHI3, and ED pairs detect the standing wave of the incident signal along the T-line. Each ED pairs have their own intersection point in the frequency domain, and eventually locks its frequency to the point, in other words, locking the LO frequency to the desired channel. The VCO and ILFD are widely tunable from 60 to 67GHz. According to the measurements, the FLL was able to lock 12 non-overlapping channels with approximately 580MHz frequency spacing to the adjacent channel. The FLL settling behavior on ED outputs is measured in the transient domain, as shown in Figure 5.5(b). As shown, the LO frequency is regulated within 70μs.

As shown in Figure 5.13, more than 90% of the FLL circuitry except mm-Wave blocks were integrated under the ground plane, saving area while reducing the complexity of the floor planning without harming the mm-Wave performance.

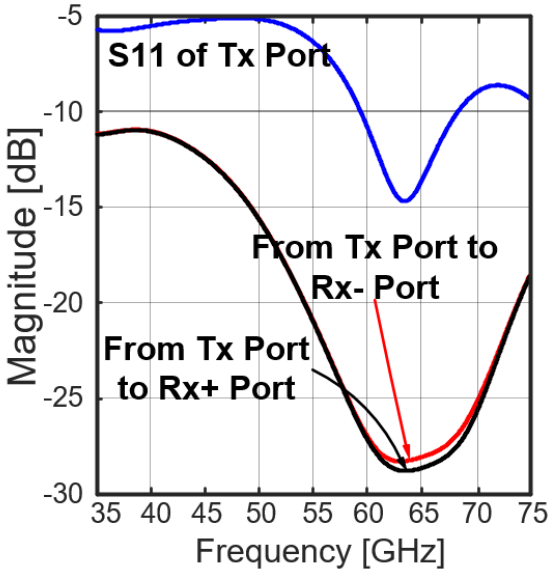
5.2.2 On-chip Slot-Loop Antenna and TRx System

The crystal-less TRx not only provides an on-chip frequency reference for precise mm-Wave channel, but also an on-chip slot-loop antenna with good radiation efficiency across the desired band. Figure 5.6(a) shows the on-chip slot-loop antenna with signal traces that supports both Tx and Rx modes by utilizing the orthogonality of the square shaped slot-loop [4]. According to [59], the on-chip loop antenna has better radiation efficiency than a patch antenna due to limited depth of metal layers in a CMOS process. Thinning the height of the ground plane, and signal

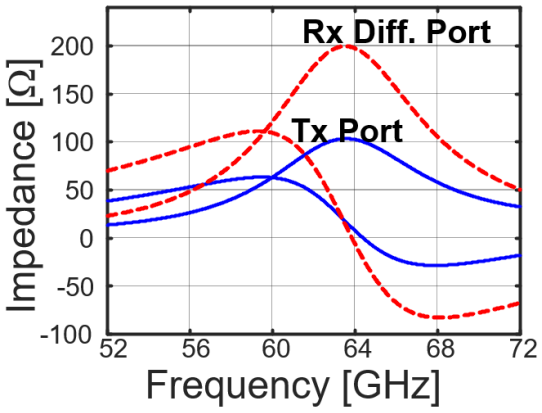
plane of the patch antenna degrades its efficiency [31, 57], which is significant when implemented in CMOS that has a few tens of micrometer for metal routing thickness. On the other hand, the on-



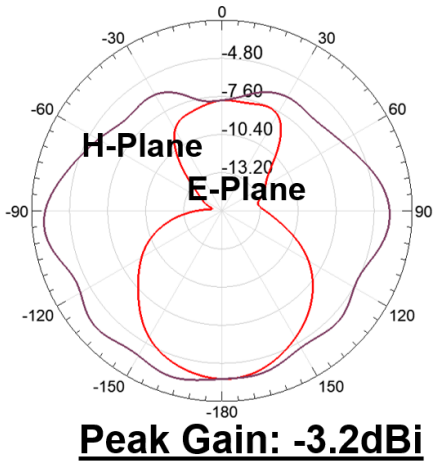
(a)



(b)



(c)



(d)

Figure 5.6 (a) On-chip dual mode slot-loop antenna that has single Tx port, and differential Rx ports. (b) Simulated Tx power magnitude response seen from Tx input, and differential Rx outputs. (d) Simulated antenna radiation pattern.

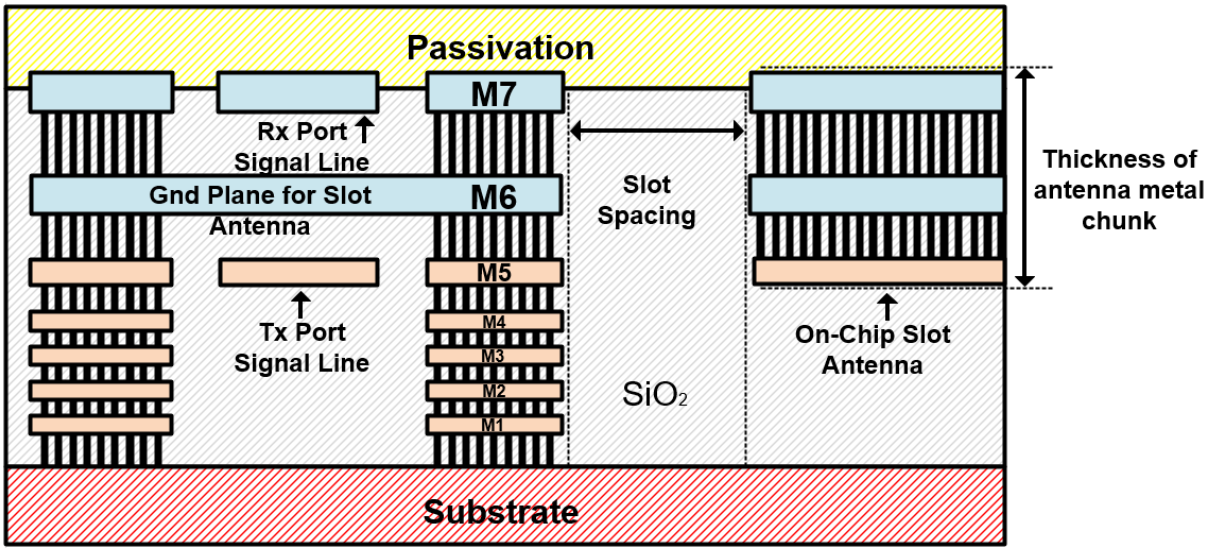
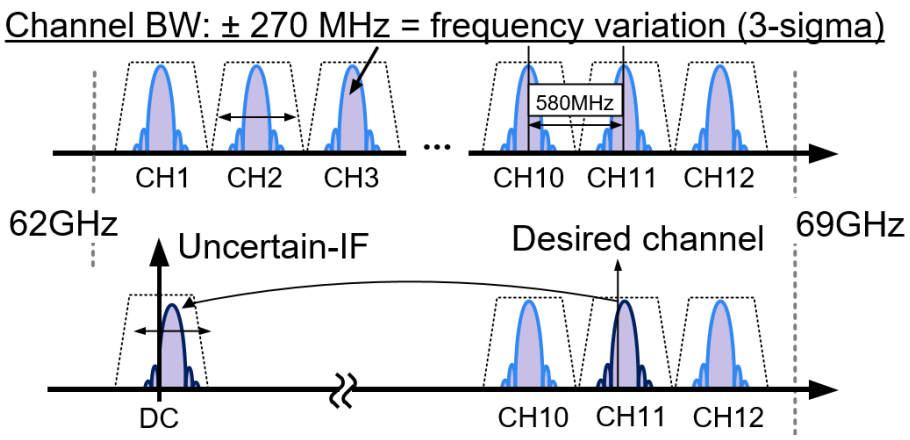


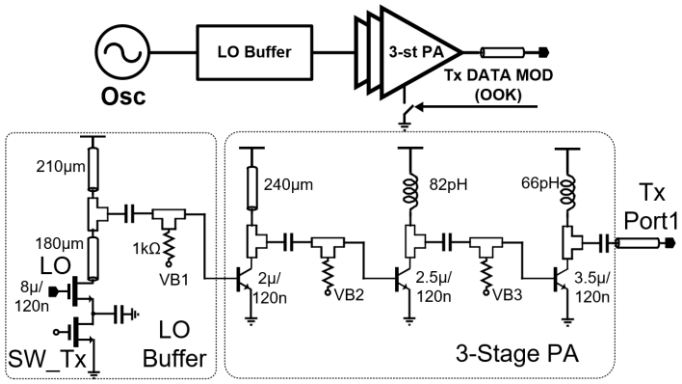
Figure 5.7 Cross-view of on-chip slot loop antenna, and TRx matching network.

chip slot-loop antenna is not limited by the metal height of the CMOS process because it radiates based on horizontal spacing of the signal plane and ground plane. Furthermore, the slot type antenna is chosen, due to its benefits on the integration in systems. The slot loop antenna can be fabricated and concealed it within metallic objects that could otherwise impact antenna performance due to other objects in close proximity. As shown in Figure 5.6(b), the Tx-to-Rx isolation of the antenna itself is 27dB, comparable to active TRx switches at 60GHz. In addition, the differential Rx path (from Port2,3 to differential Rx output) does further common mode rejection on the attenuated Tx signal that is leaked Port1. The total Tx leakage rejection seen from differential Rx output was 38dB according to simulations. As shown in Figure 5.6(d) the on-chip slot-loop antenna provides a simulated -3.2dBi peak gain with <-10dB S11 matching across the desired band and 42% antenna efficiency.

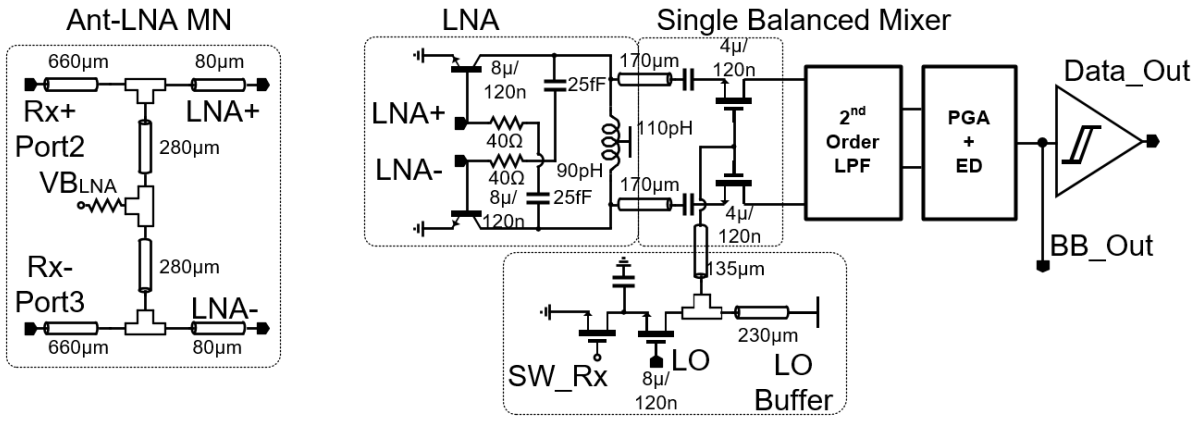
The implementation of the slot loop antenna in CMOS is shown in Figure 5.7. The on-chip slot loop antenna is composed of metals M5-M7, and each layer is connected with VIAs that forms



(a)



(b)



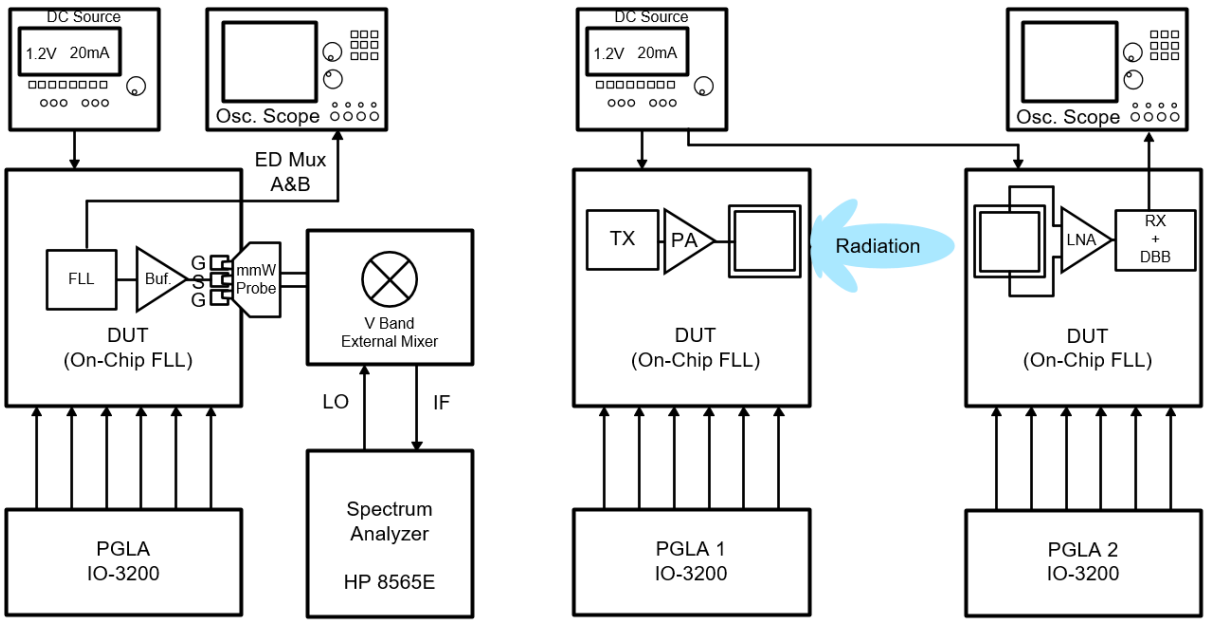
(c)

Figure 5.8 (a) TRx frequency planning diagram. (b) OOK based Tx architecture with 40dB Tx leakage suppression. (c) Receiver architecture with antenna-LNA matching network.

a conductive wall. The VIAs in the antenna behave as a metal wall at 60GHz, so does the ground

wall for Tx, and Rx signal lines. To avoid path overlap, and maximize isolation between Rx and Tx signal paths, each signal path was placed on either M5 or M7, with a ground plane in M6 in the middle. The Tx signal line is assigned to M5 that has higher sheet resistance (thin layer) because it has a much shorter path compared to the differential Rx path. The metal wall of the ground plane prevents the on-chip slot antenna and signal lines from being affected by the off-chip environment. An on-chip matching network is inserted along the Rx signal line that utilizes the area on the ground plane, and saves on overall chip size. Combined with cross-coupled LNA differential inputs, the on-chip matching network on the ground plane boost the input impedance of the on-chip slot loop antenna.

The TRx starts up as the FLL regulates the LO frequency to the desired channel, controlled by the finite state machine (FSM). The frequency plan is shown in Figure 5.8(a). As mentioned in



(a) (b)

Figure 5.9 Test setups. (a) on-chip passive component characteristics measurement, FLL measurement. (b) TRx chip-to-chip measurement.

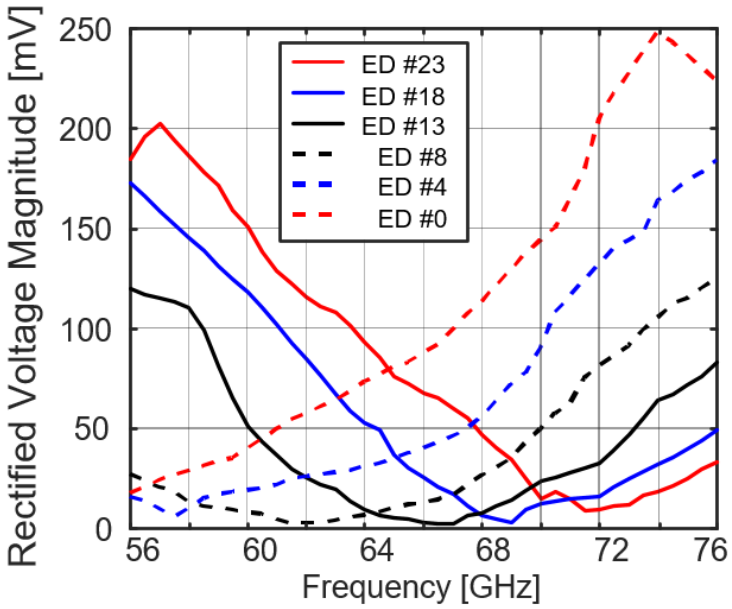
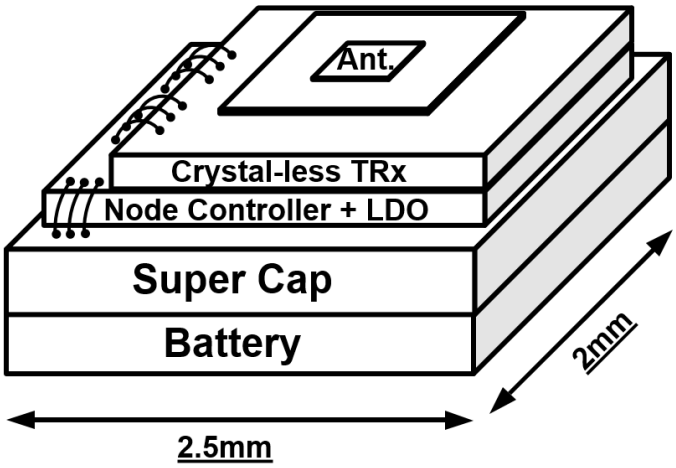
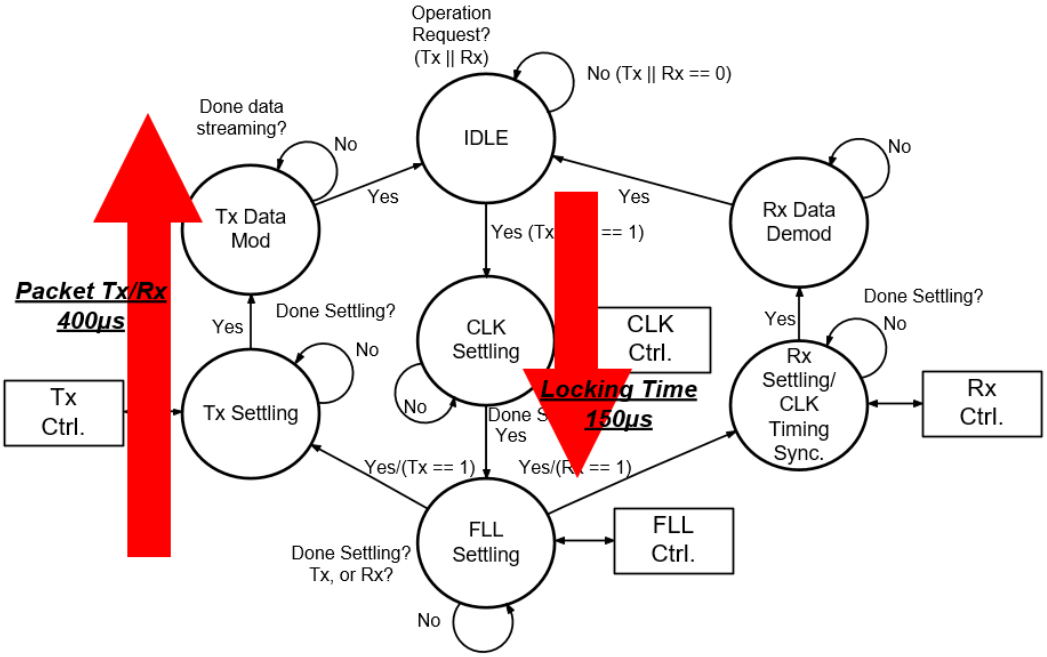


Figure 5.10 Measured voltage profile on ED output with 6 different taps vs. measured VCO frequency.

sub-section 5.2.1, the 12 non-overlapping channels are spread from 60GHz to 67GHz with approximately 580MHz. The TRx does OOK data (de)modulation, and the receiver does uncertain IF demodulation with a channel bandwidth of 3 times the frequency variance (3σ) that is reported in Figure 5.12(a). The detailed circuit block diagram of the TRx is shown in Figure 5.12(b), and Figure 5.12(c). For the power hungry blocks, FETs were used for better matching right after the 60GHz LO output, and BJTs were chosen for efficient gain performance, especially in the 60GHz PAs, and LNA. For Tx design, leakage suppression from the LO to Tx port has been consider for robust dual-mode TRx operation when the PA is not in use. The three-stage single-ended PA is implemented as shown in Figure 5.12(b). The number of stages is chosen by the desired sensitivity of the Rx with a target node-to-node link budget of 2m in this work. According to simulations, 40dB of leakage suppression on the PA was adequate for -70dBm sensitivity Rx including the leakage suppression on the dual-mode antenna. The pulse based OOK Tx modulates the data with the 3-stage PA by alternating the power of BJT drivers in the PA to enable the PA when sending



(a)



(b)

Figure 5.11 (a) System integration diagram. (b) Finite-state-machine (FSM) of the digital baseband in crystal-less TRx.

'1', and disable the PA when sending '0'. To optimize the active power of the mm-Wave TRx, while reducing the complexity of the structure, each mode in the TRx uses only uses a single phase

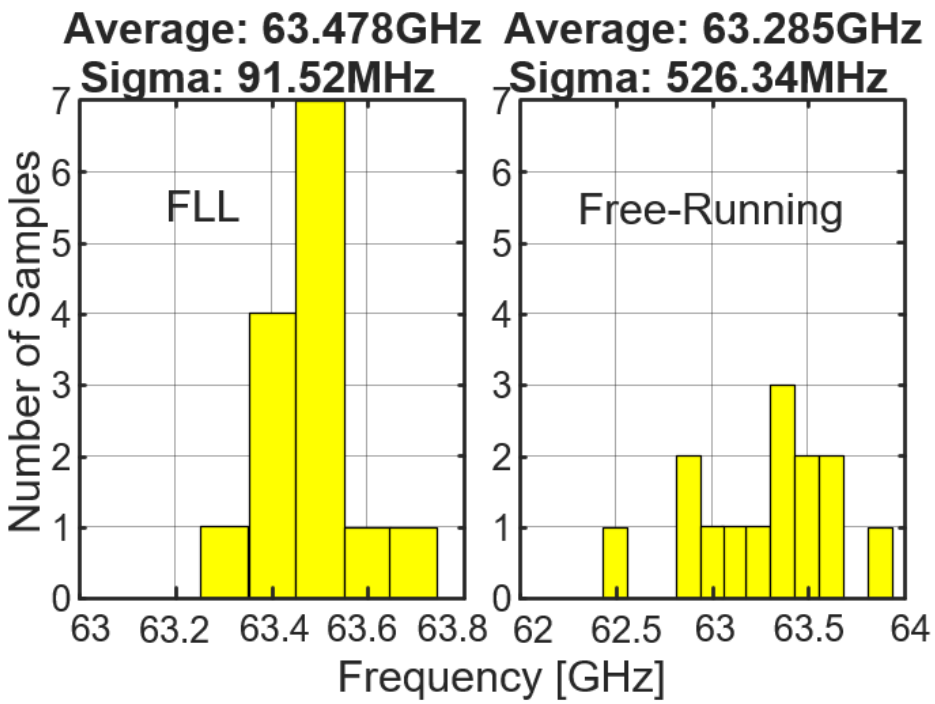
LO. The Rx path has a differential LNA for cancelling the Tx common mode signal, enhancing the gain on the LNA output, and removing even harmonics when down-converting with a single phase LO signal. The down converted IF signal is energy detected, and demodulated to recode the digital bit stream.

5.2.3 System Operation

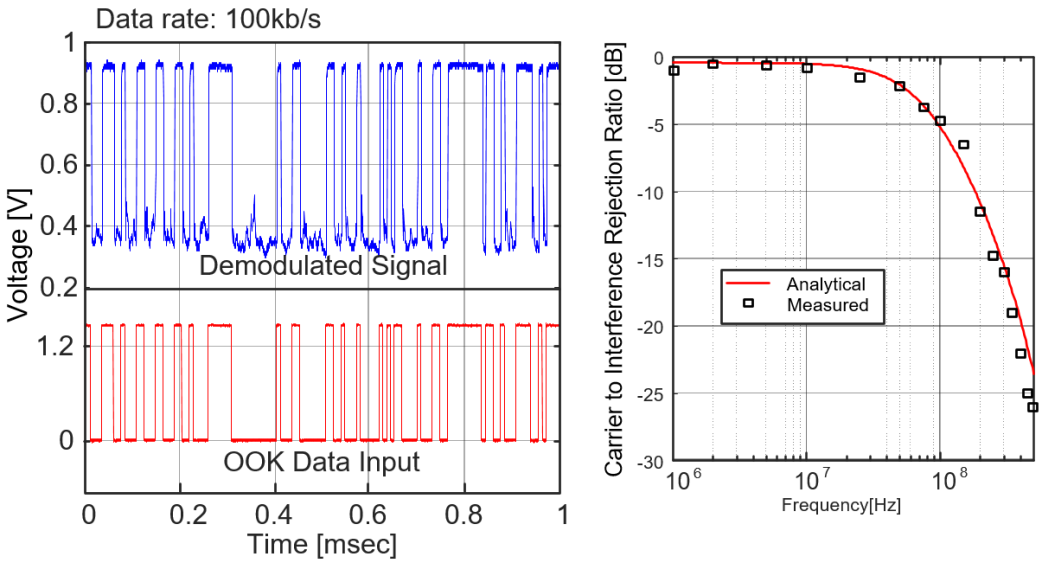
The crystal-less TRx has relatively high active power ranged from 10mW to 20mW due to its high operation frequency that hardly operates with mm^3-scale micro batteries which have very a limited output current limit (few tens of μA). The system integration diagram of the WSN is shown in Figure 5.11(a). The mm^3-scale system consists of a TRx chip, a LDO integrated node controller chip, 7μF charging cap, and a 3.3V micro battery. The crystal-less TRx duty cycles its operation using the FSM in the digital baseband, which can be externally controlled by the master node. The master node triggers TRx chip when the super cap in WSN stores sufficient current from the micro battery. The finite-state-machine (FSM) of the crystal-less TRx is shown in Figure 5.11(b). According to the measurement, the FLL requires 150μs of locking time. With the packet length of 400μs, the LDO needs to provide 18mA for 550μs that requires charging cap of 7μF based on the equation

$$I \times \Delta t_{Operation} = C_{Supercap} \times \mathrm{V}. \qquad (8)$$

The average power of the system is 110μF with 0.55% duty-cycle.



(a)



(b) (c)

Figure 5.12 (a) Chip-to-chip frequency accuracy with free-running VCO (right), and FLL enabled (left). (b) Measured OOK data reception on Rx energy detector output. (c) Measured TRx carrier-to-interference rejection (CIR) ratio.

Table 5.1 Performance summary and comparison to prior art receivers

	ISSCC 2012 [2]	JSSC 2013 [3]	JSSC 2011 [1]	This Work
Technology	90nm CMOS	0.18μm bi-CMOS	0.13μm CMOS	0.13μm bi-CMOS
Type	External reference (RF)	UWB	On-chip reference	On-chip reference
Full TRx?	Yes	Yes	No	Yes
Tx power	380μW	291μW	29.6mW	9mW*
Rx power	480μW	306μW	NA	7mW*
FLL power	NA	NA	NA**	19mW
Frequency	915MHz (Rx), 2.4GHz (Tx)	9.8GHz	60GHz	64GHz
On-chip reference frequency accuracy***	NA	NA	9869 ppm	4325ppm
Channel selection	Yes	Yes (9-10GHz)	No	Yes (60-68GHz)
Antenna	2 Off-chips (915MHz, 2.4GHz)	Off-chip	On-chip	On-chip
Chip area	$1.54mm^2$	$2.73mm^2$	$2.85mm^2$	$2.5mm^2$
Data-rate	5Mb/s	30kb/s	NA	100kb/s
Sensitivity	-15dBm	-77dBm	NA	-71dBm

* VCO power excluded
** Included in total Tx power
*** 3-sigma of chip-to-chip frequency variation

Table 5.2 Crystal-less Transceiver Power Breakdown

Block	VCO+ILFD	Receiver	Transmitter	FLL Circuits + Others
Power	18mW	7mW	9mW	1mW

5.3 Measured Results

The crystal-less TRx was fabricated in a Bi-CMOS 130nm technology. The total chip size is 2.5mm2 (Figure 5.13 Chip photograph (Top), and layout of 60GHz TRx.). As can be seen, the

chip is efficiently utilizing its area by inserting low frequency circuits beneath the custom passive devices. The on-chip FLL circuitry, and passive device characteristics have been measured using RF probes, and system tests have been done using the setup shown in Figure 5.9 (a). The measured chip-to-chip accuracy is shown Figure 5.9(b). The operation frequency was measured from 14 different chips, and as can be seen, chip-to-chip frequency variance is 4325ppm that is improved by 5.6 times compared to the free-running VCO thanks to T-line resonator implementation, and the DC calibrated FLL circuits. Compared to [58], the frequency variance is improved by 2.1 times. The voltage profiles of six EDs are shown in Figure 5.10 that interpret the standing wave on the T-line resonator. A node to node communication experiment was done to measure carrier to interference ratio (CIR), and transient measurements (Figure 5.12). The CIR was measured by shifting the operation frequency of the Tx with the Rx fixed. The receiver has a CIR of -16dB at 300MHz frequency offset, due to the uncertain IF receiver and channel select filtering. The Rx envelope detector output is shown in Figure 5.12(b). The sensitivity of the Rx was -71dBm at BER of 10^{-3} and data-rate of 100kb/s.

The FLL consumes 19mW, while the Tx, and Rx consumes 9mW, and 7mW, respectively as shown in Table 5.2. The crystal-less TRx is compared with prior reference-less RF systems in Table 5.1. Comparing to prior arts, this TRx has the ability to communicate node-to-node without any external frequency reference, using an integrated antenna, with 12 non-overlapping channels.

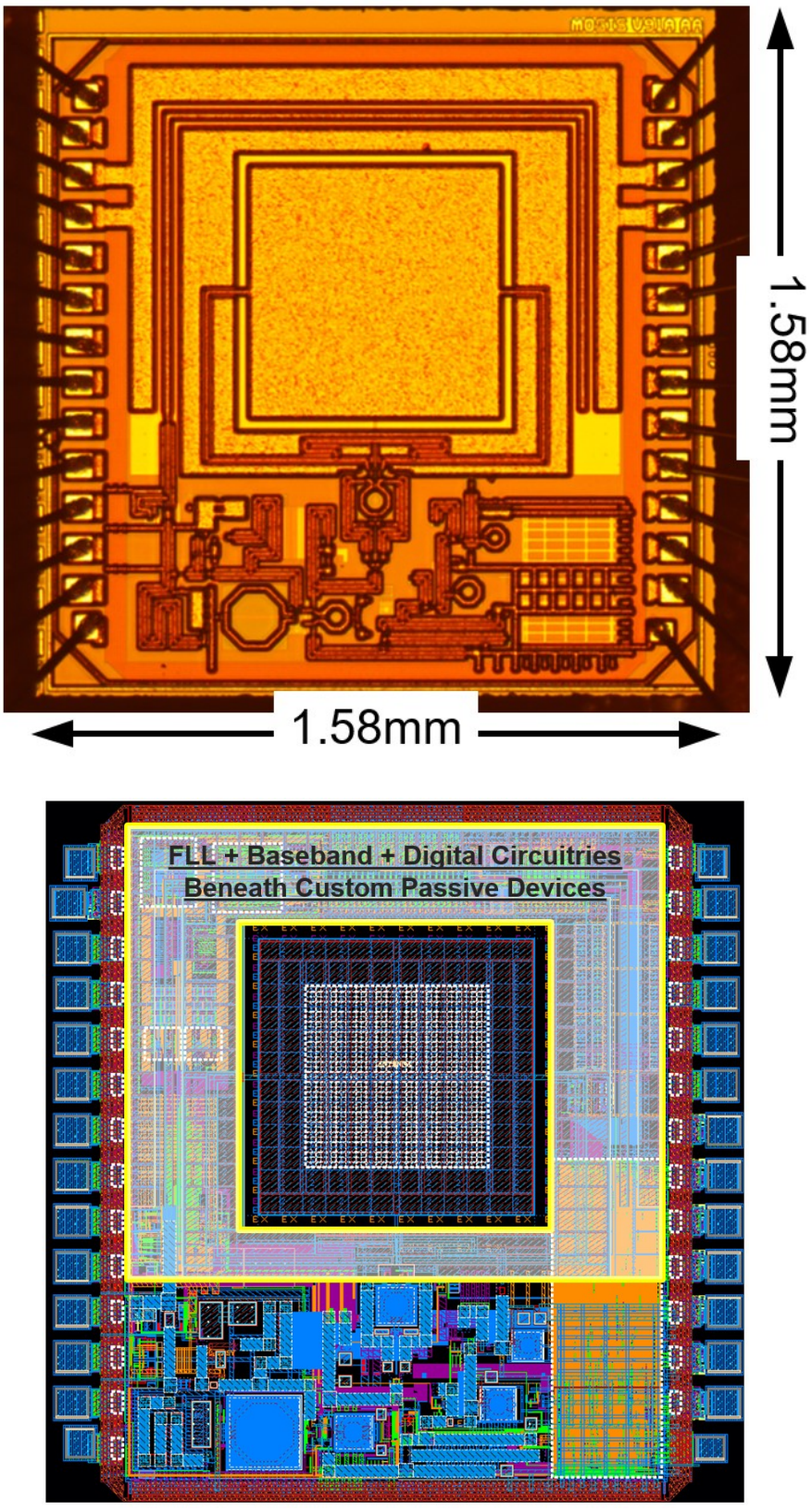


Figure 5.13 Chip photograph (Top), and layout of 60GHz TRx.

Chapter 6 Conclusions, and Future Works

6.1 Conclusions

A new class of computing devices emerges approximately every decade as a “minimal” computer that provides a new platform with a new network, interface, and information processing system for a new computing environment. Recently, WSNs for ubiquitous computing take center stage as the next trend in computing devices that are sharing their information through the internet, and we call this representative candidate the “Internet of Things” (IoT).

To maximize the widespread adoption of the “minimal” IoT device that is projected to reach 10s of billions of devices in early 2020s, some specifications have to be addressed and solved such as active power of the device, utilization of standard network protocols, and the integration of the computing device. The RF system in the “minimal” IoT device is the most challenged by these specifications. The excessive power consumption of pervasive wireless network protocols, such as WiFi, LTE, Bluetooth consumes significant power which leads to requiring a bulky battery. State-of-art ULP radios can solve the battery issue, however, most of the radios are not available to listen, or talk through the commercial network protocols. This limits their widespread adoption.

They also have issues related to interferer tolerance, and wireless range, limiting their performance in a dense wireless network with shared spectrum. The bulky off-chip crystal is required for most RF systems, and no reference-less node-to-node RF communication has been reported. The size of the off-chip antenna limits the form-factor of the device to ensure efficient radiation. Recent research contributions are beginning to solve each challenge to provide the potential of ubiquitous of "minimal" IoT devices.

In chapter 2, An ULP back-channel receiver for binary FSK back-channel signals embedded in 5.8GHz IEEE 802.11a Wi-Fi OFDM packets is presented. The proposed back-channel receiver architecture employs a two-step down-conversion where the first mixing stage utilizes the 3rd harmonic of the LO for power efficiency. The radio uses an off-chip SAW filter, balun and a 250kHz reference crystal as external components. The receiver uses a 1V supply voltage for analog blocks, and 0.85V for digital blocks including the LO and FLL. The LP-65nm CMOS receiver consumes 335µW with a sensitivity of -72dBm at a BER of $\mathbf{10^{-3}}$ and data-rate of 31.25kb/s.

In chapter 3, A 40 nm CMOS IEEE 802.11ba low-power wake-up receiver (LP-WUR) is presented. It receives 802.11ba messages generated by an 802.11 orthogonal frequency-division multiplexing (OFDM) transmitter operating at 5.8 GHz. The power consumption of the RF front-end is minimized by removing active RF gain stages, and using a 3rd harmonic passive mixer with ring-based LO operating at 1/3 the RF frequency. The noise figure is 14 dB, taking advantage of a 1:3 transformer that provides passive voltage gain in front of the high switch loss mixer-first RF front-end, and matching across 5.5-5.8 GHz with <-12 dB S11. The receiver achieves a sensitivity

of -83 dBm and -20 dB adjacent channel signal-to-interference ratio (SIR) while consuming 220 μW at a bit-error-rate (BER) of 10-3 and data-rate of 62.5 kb/s, which shows the best sensitivity-power trade-off among >3 GHz receivers.

In chapter 4, a stand alone, fully integrated 0.2V 578μW ultra-low voltage (ULV) 2.4GHz 802.11ba WiFi wake-up receiver (WRX) is presented. It includes a current-efficient ULV noise cancelling LNA with high turn step-up transformer, and Q-enhanced RF gain stages for low noise figure. For minimizing the current load on the micro-power manager, the 1/3 RF mixer, and ULV FLL are implemented. It achieves -91.5dBm sensitivity at 10-3 BER and data-rate of 62.5kbps, while rejecting 45dB of adjacent blocker with only 0.2V supply. The WRX includes an energy-efficient 5ms startup sequence which interfaces to an external node controller over SPI.

In chapter 5, a crystal-less, fully-integrated 60GHz transceiver (TRx) is presented. The radio is designed for mm-scale wireless sensor nodes (WSN) eliminating the need for a bulky off-chip reference. An on-chip transmission-line-referenced frequency locked loop (FLL) employing a digitally calibrated DC-offset cancellation circuitry allows locking to the desired channel frequency within 4325ppm chip-to-chip variation, and supports 12 non-overlapping channels across the 60-68GHz band. The design exploits a band integrated on-chip slot antenna due its high gain efficiency. The antenna supports two orthogonal modes for simultaneous transmission and reception while minimizing Tx-to-Rx leakage on-chip. The TRx has been fabricated using 130nm Bi-CMOS technology. The FLL consumes 19mW, and the Tx and Rx consume 9mW and 7mW, respectively.

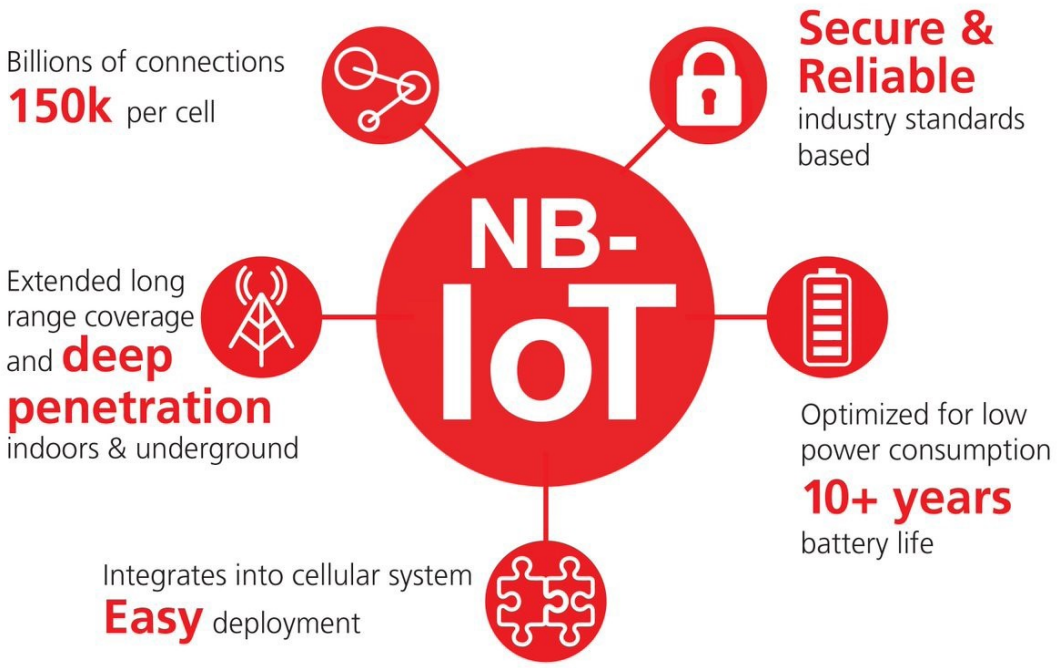


Figure 6.1 In/guard-Band deployment of NB-IoT (top), and SC-FDMA based (de)modulation (bottom) [60].

6.2 Future Works: NB-IoT wake-up receiver for MELs phantom power reduction

The WRX for Miscellaneous electric loads (MELs) energy reduction has been presented in Chapter 4. The project is ongoing with improved flexible wireless connectivity module that substantially reduces the power consumption of MELs. Although the wireless connectivity module with WiFi WRX is good for ubiquitous deployment, to maximize the potential of ubiquity of this application, the wireless connectivity module of MELs application has to provide energy-efficient, long-range cellular communications.

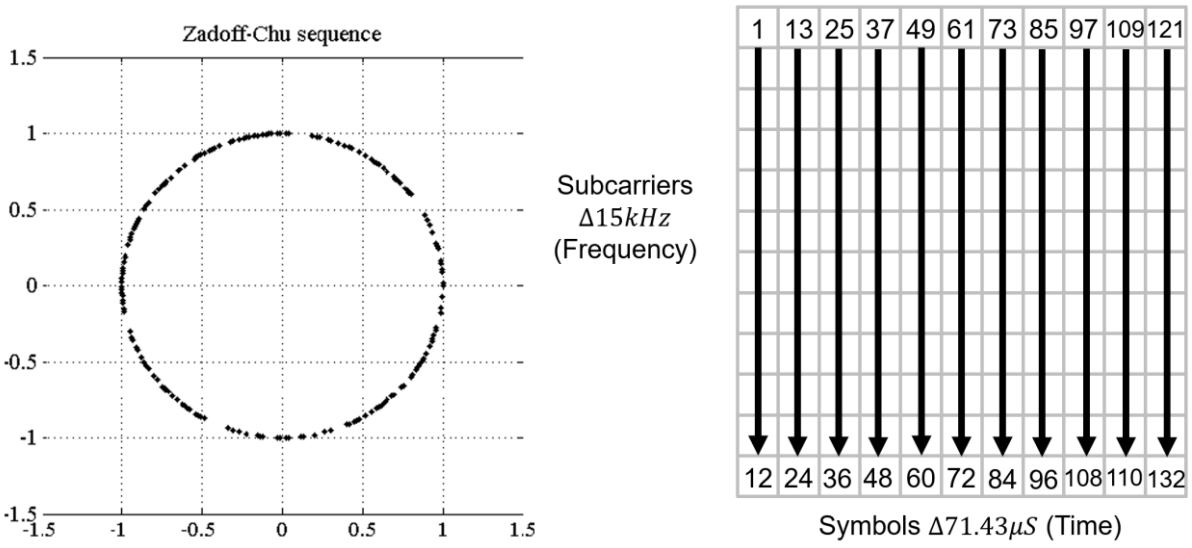


Figure 6.2 Zadd-off Chu sequence coded WUS data in I/Q constellation plot (left), and 132 resource elements in a sub-frame (right) [61].

As mentioned in Chapter 1, there are few cellular networks that are aimed for IoT applications, especially NB-IoT that are adopted for long-range, secure IoT devices. As shown in Figure 6.1, those standards have attractive qualities such as extremely broad coverage, and high security, Also the communication system doesn't require additional local network because it communicates with cellular towers nearby that has large network capacity as well [60]. Those transceivers, however, are very power hungry despite of its low data-rate because their adopted features in LTE standard that is time-multiplexed, and wideband (OFDM) that requires a lot of load on hardware perspective. Therefore, to achieve extremely long 10+ battery life, extremely aggressive discontinuous reception cycle (DRX) is inevitable that exceeds much more than 10s. To support various functionality of the network, the cellular IoT radio has to consume excessive power, even greater than 50mW. To support latency critical applications that requires <10s of

wake-up, automotive, and continuous data gathering, a very low power, high latency solution is needed.

Recently, the 5G standard development organization, 3GPP, added new wake-up signal (WUS) feature in NB-IoT according to the most recent release 15 [61]. The radio will occasionally turn on to look for a unique wake-up signal called a paging event. By deploying a companion radio on main radio that has <0.1x active power inside main radio system, the NB-IoT radio system can track data from cell-tower more frequent with same power budget than conventional NB-IoT radios by enabling WRX to detect the wake-up signal from cell tower while no active network is present. The frame structure of WUS is shown in Figure 6.2. Each sub-carrier in a sub-frame of WUS is coded in Zadoff-Chu sequence that has relatively simple structure comparing to other NB-IoT sub-frames.

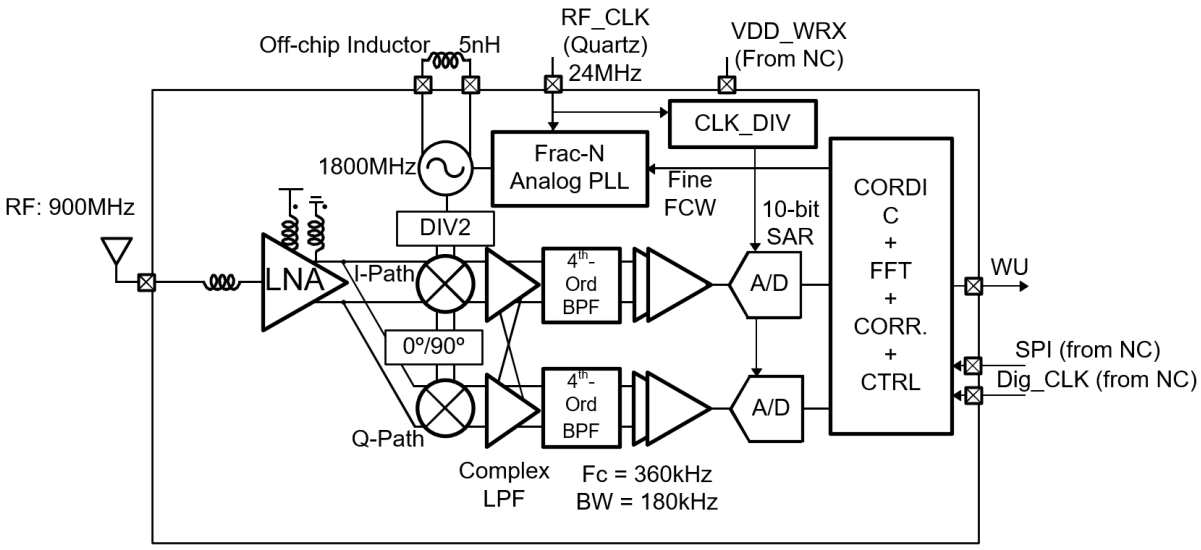


Figure 6.3 Conceptual system block diagram of low-power NB-IoT wake-up receiver.

The proposed NB-IoT WRX is shown in Figure 6.3. For the robustness of WUS detection feature in NB-IoT radios, the WRX has to meet ranging requirement of NB-IoT receiver. The receiver is looking for Zadoff-Chu sequence coded WUS data and detect it by using digital correlator that tracks the sequence of resource elements. According to the NB-IoT standard [61], the receiver has to support a 164dB link budget with +23dBm transmitter, and that leads us to implement WRX with NF of 3dB. The low active power, simplicity of design can be achieved by current efficient RF front-end with off-chip network for good RF blocker rejection, and collaboration of over-sampled DSP, analog based fractional-N PLL, and Low-IF baseband architecture for auto-channel correction. Unlike conventional direct down conversion, the WRX is low-IF architecture for several advantages such as improved NF, efficient RF gain requirement, and complexity of baseband architecture. Also, the architecture is less dependent on I/Q imbalance

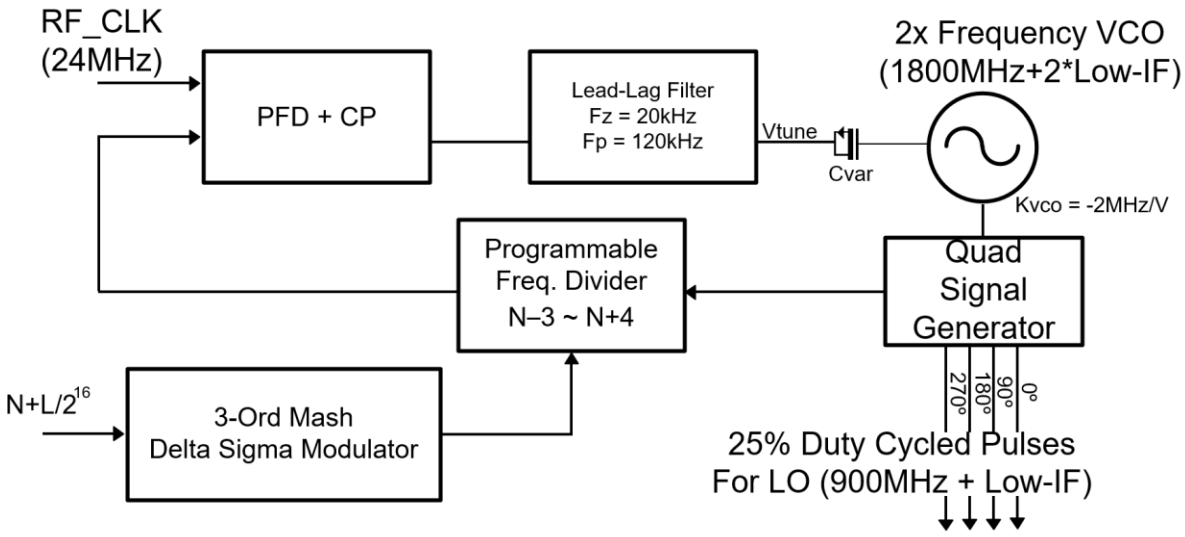


Figure 6.4 Analog fractional-N PLL that provides LO for low-IF down-conversion.

of the RF front-end for demodulation. Finally, the architecture is less insensitive to center frequency offsets that can be relieved further when demodulating the RF signal due to the nature of $\Delta f / f_c$. Oversampled DSP after ADC can auto-correct the fine LO offsets efficiently be the precise FFT profile of the sub-channels.

The NB-IoT WRX can be improved further in systemic perspective by implanting fast locking, high FoM PLL because conventional PLL in NB-IoT has very long locking time due to fine channel resolution.

Bibliography

[1] G. Bell, "Bell's Law for the Birth and Death of Computer Classes: A theory of the Computer's Evolution," *IEEE Solid-State Circuits Society Newsletter,* vol. 13, no. 4, pp. 8-19, Fall 2018.

[2] C. A. Mack, "Fifty Years of Moore's Law," *IEEE Transactions on Semiconductor Manufacturing,* vol. 24, no. 2, pp. 202-207, May 2011.

[3] Y. Lee, D. Sylvester and D. Blaauw, "Circuits for ultra-low power millimeter-scale sensor nodes," in *Conference Record of the Forty Sixth Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov. 2012.

[4] O. Khan, A. Niknejad and K. Pister, "Ultra low-power transceiver SoC designs for IoT, NB-IoT applications," in *IEEE Custom Integrated Circuits Conference (CICC)*, 2018.

[5] M. Rouse, Internot of Things (IoT), IOT Agenda, Aug. 2019.

[6] G. Schatz, "The Complete List of Wireless IoT Network Protocols," LinkedLabs, 08 Feb. 2016. [Online]. Available: https://www.link-labs.com/blog/complete-list-iot-network-protocols.

[7] A. Sai and e. al., "A 5.5 mW ADPLL-Based Receiver With a Hybrid Loop Interference Rejection for BLE Application in 65 nm CMOS," *IEEE J, Solid-State Citcuits,* vol. 51, no. 12, pp. 3125-3136, Dec. 2016.

[8] Z. Weng and e. al., "400-MHz/2.4-GHz Combo WPAN Transceiver IC for Simultaneous Dual-Band Communication With One Single Antenna," *IEEE Trans. Circuits Syst. I Regul. Pap.,* vol. 65, no. 2, pp. 745-757, Feb. 2018.

[9] D. Wenzloff, "Low Power Radio Survey," [Online]. Available: www.eecs.umich.edu/wics/low_power_radio_survey.html.

[10] A. M. Alghaihab, H. Kim and D. D. Wentzloff, "Analysis of Citcuit Noise and Non-Ideal Filtering Impact on Energy Detection Based Ultra-Low-Power Radios Performance," *IEEE Trans. Circuits Syst. II Express Briefs,* vol. 65, no. 12, pp. 1924-1928, Dec. 2018.

[11] N. E. Roberts and e. al., "26.8 A 236nW -56.5dBm-sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2016.

[12] J. Moody and e. al., "A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation," in *ISSCC Dig. Tech. Papers*, Feb. 2018.

[13] V. Mangal and P. R. Kinget, "28.1 A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator," in *ISSCC Dig. Tech. Papers*, Feb. 2019.

[14] J. Moody and e. al., "A -106dBm 33nW Bit-Level Duty-Cycled Tuned RF Wake-up Receivers," in *Symposium on VLSI Circuits*, June 2019.

[15] C. Bryant and H. Sjöland, "A 0.55 mW Saw-Less Receiver Front-End for Bluetooth Low Energy Applications," *IEEE j. Emerg. Sel. Top. Circuits Syst.,* vol. 4, no. 3, pp. 262-272, 2014.

[16] J. Im, H. Kim and D. Wentzloff, "A 217uW -82dBm IEEE 802.11 Wi-Fi LP-WUR using a 3rd-Harmonic Passive Mixer," in *IEEE RFIC Symp.*, June. 2018.

[17] M. Rahman and R. Harjani, "A Sub-1-V 194-uW 31-dB FOM 2.3-2.5-GHz Mixer-First Receiver Frontend for WBAN With Mutual Noise Cancellation," *IEEE Trans. Microw. Theory Tech.,* vol. 64, no. 4, pp. 1102-1109, Apr. 2016.

[18] J. Im, H. Kim and D. D. Wentzloff, "A 470uW -92.5dBm OOK/FSK Receiver for IEEE 802.11 WiFi LP-WUR," in *IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, 2018.

[19] A. Alghaihab, J. Breiholz, H. Kim and D. D. Wentzloff, "A 150 uW -57.5 dBm-Sensitivity Bluetooth Low-Energy Back-Channel Receiver with LO Frequency Hopping," in *IEEE RFIC Symp.*, June 2018.

[20] A. Alghaihab, Y. shi, J. Breiholz, H. Kim, B. H. Calhoun and D. D. Wentzloff, "Enhaced Interferenced Rejection Bluetooth Low-Energy Back-Channel Receiver With LO Frequency Hopping," *IEEE J. Solid-State Circuits,* vol. 54, no. 7, pp. 2019-2027, July 2019.

[21] C. Salazar, A. Cathelin, A. Kaiser and J. Rabaey, "A 2.4 GHz Interferer-Resilient Wake-Up Receiver Using A Dual-IF Multi-Stage N-Path Architecture," *IEEE J. Solid-State Circuits,* vol. 51, no. 9, pp. 2091-2105, Sep. 2016.

[22] N. E. Roberts, M. C. Kines and D. D. Wentzloff, "A 380uW Rx, 2.6mW Tx 433MHz FSK transceiver with a 102dB link budget and bit-level duty cycling," in *IEEE RFIC Symp.*, June 2015.

[23] W. Yu and e. al., "A 0.18V 382uW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2017.

[24] A. Selvakumar, M. Zargham and A. Liscidini, "13.6 A 600uW Bluetooth low-energy front-end receiver in 0.13um CMOS technology," in *ISSCC Dig. Tech. Papers*, 2015.

[25] M. Park, "Wake-Up Radio (WUR) Oeration," May 2016. [Online]. Available: www.ieee802.org/11/Reports/tgba_update.html.

[26] O. Liberg, M. Sundberg, Y.-P. E. Wang, J. Bergman and J. Sachs, Cellular Internet of Things: Technologies, Standards and Performance, Elsevier, Academic Press, 2018.

[27] LoRa Integration - Link Labs, LinkLabs, Feb. 2016.

[28] E. Nilson and C. Svensson, "Power Consumption of Integrated Low-Power Receivers," *IEEE J. Emerg. Sel. Top. Circuits Syst.,* vol. 4, no. 3, pp. 273-283, 2014.

[29] P. P. Wang and P. P. Mercier, "28.2 A 220uW -85dBm Sensitivity BLE-Compliant Wake-up Receiver Achieving -60dB SIR via Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimentional Wake-Up Signature," in *ISSCC Dig. Tech. Papers*, Feb. 2019.

[30] S. Sultan, T. Khan and S. Khatoon, "Implementation of HVAC System Through Wireless Sensor Network," in *2010 Second International Conference on Communication Software and Networks*, Singapore, 2010.

[31] F. Gutierrez, K. Parrish and T. S. Rappaport, "On-Chip Integrated Antenna Structures in CMOS for 60 GHz WPAN Systems," in *GLOBECOM IEEE Global Telecommunications Conference*, Honolulu, HI, 2009.

[32] D. Antonio, D. Zanette and D. Lopez, "Frequency stabilization in nonlinear micromechanical oscillator," *Nature Communication,* vol. 3, May 2012.

[33] "Crystal Oscillator," Murata, XTCHH52M000TJEA1P0, 2017.

[34] "Ceramic SMD Crystal Clock Oscillaor," Abracon, ABFM series, 2010.

[35] "Plastic Package Industrial Grade Ultra Miniature Pure SiliconTM Clock Oscillator," Abracon, ASDMB series, 2015.

[36] "SAW Basd Clock Oscillator," Crystek, CCS575S, 2017.

[37] L. Chuo, Y. Shi, Z. Luo, N. Chiotellis, Z. Foo, G. Kim, Y. Kim, A. Grbic, D. Wentzloff, H. Kim and D. Blaauw, "7.4 A 915MHz Asymmetric Radio using Q-Enhaced Amplifier for a Fully Integrated 3x3x3mm3 Wireless Sensor Node with 20m Non-Line-of-Sight Communication," in *ISSCC Dig. Tech. Papers*, Feb. 2017.

[38] G. Papotto, F. Carrara, A. Finocchiaro and G. Palmisano, "A 90nm CMOS 5Mbs Crystal-Less RF Transceiver for RF-Powered WSN Nodes," in *ISSCC Dig. Tech. Papers*, Feb. 2012.

[39] X. Huang, S. Rampu, X. Wang, G. Dolmans and H. d. Groot, "A 915 MHz, Ultra-Low Power 2-Tone Transceiver With Enhaced Interference Resilience," *IEEE J. Solid-State Circuits,* vol. 47, no. 12, pp. 3197-3207, Dec. 2012.

[40] J. Pandey, J. Shi and B. Otis, "A 120uW MICS/ISM Band FSK Rx with 44uW Low Power Mode Based on Injection Locking and 9X Frequency Multiplication," in *ISSCC Dig. Tech. Papers*, Feb. 2011.

[41] C. Salazar and e. al., "A -97dBm-Sensitivity Interferer-Resilient 2.4GHz Wake-Up Receiver Using Dual-IF Multi-N-Path Architecture in 65nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2015.

[42] H. Jiang and e. al., "A 4.5nW Wake-Up Radio with -69dBm Sensitivity," in *ISSCC Dig. Tech. Papers*, Feb. 2017.

[43] H. Kim and D. Wentzloff, "Back-Channel Wireless Communication Embedded in WiFi-Compliant OFDM Packets," *IEEE Journal on Selected Areas in Communications,* vol. 34, no. 12, pp. 3181-3194, Dec. 2016.

[44] J. Yin, P. Mak, F. Maloberti and R. Martins, "A 0.003mm2 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz 1/f3 Phase-Noise Corner, Extended

Tuning Range and Inherent Divided Output," *IEEE J. Solid-State Circuits,* vol. 51, no. 12, pp. 2979-2991, Dec. 2016.

[45] E. Alpman and e. al., "95uW 802.11g/n Compliant Fully-Integrated Wake-Up Receiver with -72dBm Sensitivity in 14nm FinFET CMOS," in *IEEE RFIC Symp.*, June. 2017.

[46] J. Im, H. Kim and D. Wentzloff, "A 335uW -72dBm Receiver for FSK Back-Channel Embedded in 5.8GHz Wi-Fi OFDM Packets," in *IEEE RFIC Symp.*, June. 2017.

[47] "IEEE P802.11ba/D1.0," TGba, [Online]. Available: http://www.ieee802.org/11/private/Draft_Standards/11ba/index.html.

[48] E. Alpman, A. Khairi, R. Dorrance, M. Park, V. Somayazulu, J. R. Foerster, A. Ravi, J. Paramesh and S. Pellerano, "802.11g/n Compliant Fully Integrated Wake-Up Receiver With -72-dBm Sensitivity in 14-nm FinFET CMOS," *IEEE J. Solid-State Circuits,* vol. 53, no. 5, pp. 1411-1422, May 2018.

[49] J. Cheng, N. Qi, P. Chiang and A. Natarajan, "A Low-Power, Low-Voltage WBAN-Compatible Sub-Sampling PSK Receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits,* vol. 49, no. 12, Dec. 2014.

[50] A. Homayoun and B. Razavi, "A Low-Power CMOS Receiver for 5 GHz WLAN," *IEEE J. Solid-State Circuits,* vol. 50, pp. 630-643, March 2015.

[51] C. Andrews and A. Molnar, "Implications of Passive Mixer Transparency for Impedance Matching and Noise Figure in Passive Mixer-First Receivers," *IEEE Transactions on Circuits and Systems,* pp. 3092-3103, Dec. 2010.

[52] N. Dalt and A. Sheikholeslami, Understanding Jitter and Phase Noise: a Circuits and Systems Perspective, Cambridge, United Kingdom; New York, NY: Cambridge University Press, Feb. 2018.

[53] "U.S. Energy Information Administration," AEO2015 Report, 2015. [Online]. Available: https://www.eia.gov/outlooks/archive/aeo15/.

[54] R. Liu and e. al., "An 802.11ba 495uW -92.6dBm-Sensitivity Blocker-Tolerant Wake-up Radio Receiver Fully Integrated with Wi-Fi Transceiver," in *IEEE RFIC Symp.*, June. 2019.

[55] F. Zhang and e. al., "A 1.6mW 300mV-Supply 2.4GHz Receiver with -94dBm Sensitivity for Energy-Harvesting Applications in 28nm CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2013.

[56] S. Blaakmeer and e. al., "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE J. Solid-State Circuits,* vol. 43, no. 6, pp. 1341-1349, June 2008.

[57] K. Huang and D. D. Wentzloff, "60 GHz on-chip patch antenna integrated in a 0.13-um CMOS technology," in *IEEE International Conference On Ultra Wideband (ICUWB)*, 2010.

[58] K. Huang and D. D. Wentzloff, "A 60 GHz Antenna-Referenced Frequency-Locked Loop in 0.13 uW CMOS for Wireless Sensor Networks," *IEEE J. Solid-State Circuits,* vol. 46, no. 12, pp. 2956-2965, Dec. 2011.

[59] Y. P. Zhang, M. Sun and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Transactions on Electronic Devices,* vol. 52, no. 7, pp. 1664-1668, July 2005.

[60] S. Glassman, "IoT and the four reasons why licensed spactrum technologies have been worth the wait," u-blox, 9 June 2016. [Online]. Available: https://www.u-blox.com/en/ublox-file-auth-redirection?destination=node/14610. [Accessed 26 2 2018].

[61] O. Liberg, M. Sundberg, E. Wang, J. Bergman, J. Sachs and G. Wikström, Cellular Internet of Things 2nd Edition: From Massive Deployments to Critical 5G Applications, London: Academic Press, 2019.

[62] N. Saputra and J. Long, "A Fully Integrated Wideband FM Transceiver for Low Data Rate Autonomous Systems," *IEEE J. Solid-State Circuits,* pp. 1165-1175, May 2015.

[63] X. Huang and e. al., "A 2.4GHz/915MHz 51uW Wake-Up Receiver with Offset and Noise Suppresion," in *ISSCC Dig. Tech. Papers*, Feb. 2010.

[64] S. Gambini and e. al., "A Fully Integrated, 290 pJ/bit UWB Dual-Mode Transceiver for cm-Range Wireless Interconnections," *IEEE J. Solid-State Circuits,* vol. 47, no. 3, pp. 586-598, Mar. 20112.

[65] J. Choi and e. al., "An Interference-Aware 5.8GHz Wake-Up Radio for ETCS," in *ISSCC Dig. Tech. Papers*, Feb. 2012.

[66] A. Shirane and e. al., "A 5.8GHz RF-Powered Transceiver with a 113uW 32-QAM Transmitter Employing the IF-based Quadrature Backscattering Technique," in *ISSCC Dig. Tech. Papers*, Feb. 2015.

[67] D. Shi and e. al., "A 5GHz Fully Integrated Super-regenerative Receiver with On-chip Slot Antenna in 0.13um CMOS," in *VLSI Circuits Digest of Technical Papers*, June. 2018.

[68] S. Ikeda and e. al., "A 0.5-V 5.8-GHz Ultra-Low-Power RF Transceiver for Wireless Sensor Network in 65 nm CMOS," in *IEEE RFIC Symp.*, June. 2014.

[69] K. Huang, J. Brown, E. Ansari, R. Rogel, Y. Lee, H. Kim and D. Wentzloff, "An Ultra-Low-Power 9.8 GHz Crystal-Less UWB Transceiver with Digital Baseband Integrated in 0.18 um BiCMOS," *IEEE J. Solid-State Circuits,* vol. 48, no. 12, pp. 3178-3189, Dec. 2013.

[70] C. Park and T. S. Rappaport, "Short-Range Wireless Communications for Next-Generation Networks: UWB, 60 GHz Millimeter-Wave WPAN, And ZigBee," *IEEE Wireless Communications,* vol. 14, no. 4, pp. 70-78, Aug. 2007.

[71] A. K. A. Natarajan, X. Guan, A. Babakhani and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas inSilicon: Transmitter and Local LO-Path Phase Shifting," *IEEE J. Solid-State Circuits,* vol. 41, no. 12, pp. 2807-2819, Dec. 2006.

[72] J. Im, H. Kim and D. D. Wentzloff, "A 220-uW -83-dBm 5.8-GHz Third-Harmonic Passive Mixer-First LP-WUR for IEEE 802.11ba," *IEEE Trans. Microw. Theory Tech.,* vol. 67, no. 7, pp. 2537-2545, 2019.

[73] J. Im, H. Kim and D. D. Wentzloff, "A 217uW -82dBm IEEE 802.11 Wi-Fi LP-WUR using a 3rd-Harmonic Passive Mixer," in *IEEE RFIC Symp.*, 2018.

[74] J. Moody and e. al., "Interference Robust Detector-First Near-Zero Power Wake-Up Receiver," *IEEE J. Solid-State Circuits,* vol. 54, no. 8, pp. 2149-2162, 2019.

[75] T. Chi, J. S. Park, S. Li and H. Wang, "A 64GHz full-duplex transceiver front-end with an on-chip multifeed self-interference-canceling antenna and an all-passive canceler supporting 4Gb/s modulation in one antenna footprint," in *ISSCC Dig. Tech. Papers*, Feb. 2018.