Crystal-Less RF Communication Integrated Circuits for Wireless Sensor Networks

by

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Table of Contents

List of Figures

List of Tables

Chapter 1
Introduction

1.1. The Evolution of Computing Devices

1.1.1. Background

The evolution of computing devices has changed our daily life significantly. Decades ago, it is the mainframe computers, which generally occupy large rooms with their substantial size, take care of the basic data computation for hundreds of employees in a company. Nowadays, smart-phone based devices have become the platform of personal computing, as predicted by Bell's Law [1]. Various applications such as sensing, wireless communication, digital identification, un-obtrusive surveillance, etc. have driven the computing devices to a more compact regime with mass production comparing to the previous computers.

According to Bell's Law, a new class of computers will dominate the market approximately every decade [1]. Bell defines a computer class as a set of computers with a similar cost, programming environment, network, and user interface, where each class undergoes a standard product life cycle of growth and decline. Fig. 1.1 shows the scaling and production trend of computing devices over years. From mainframe computers in the early 1950's, went through minicomputers, workstations, personal computers (PCs), laptops, and reached to the class of smart phones in the 2000's. Based on the trends, a new computer class comes into market approximately every decade, and each successive

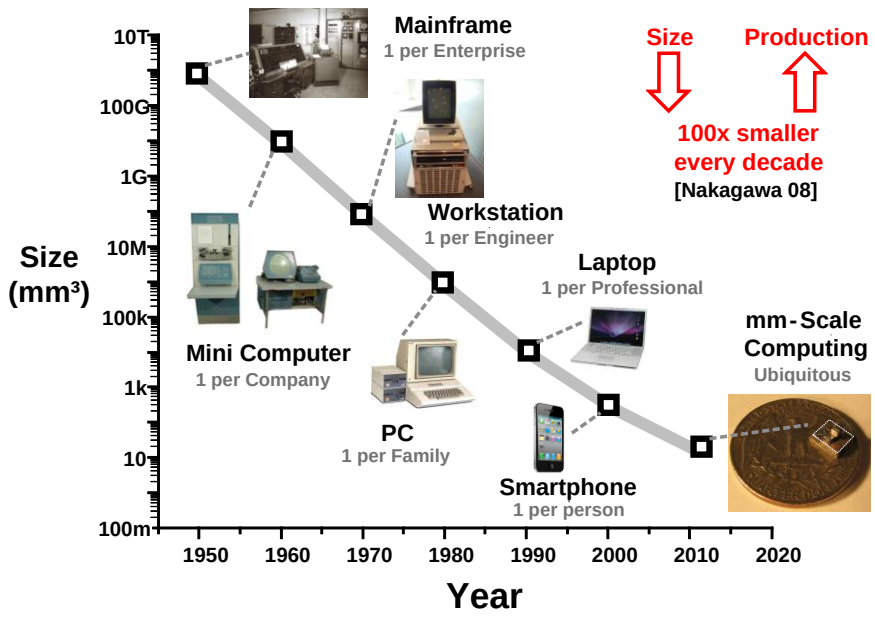


Fig. 1.1. Scaling and production trend of computing devices over years [1].

class has had a 100x reduction in volume. In addition, each successive class has resulted in a reduction in unit cost and an increase in volume of production [2].

With the trends in Bell's Law carry on, the next computer class is expected to be even smaller and more pervasive — the class of cubic-mm-scale devices. Ubiquitous sensing is projected to reach volumes of 1000 sensors per person by 2017 [3], considering that today we are surrounded by ~100 sensors at work, in the car, and at home. At cubic mm-scale, there is a growing demand for "smaller and smarter" devices in applications such as bio-medical implants and un-obtrusive monitoring.

1.2. Wireless Sensor Networks

1.2.1. Wireless Sensor Networks Overview

Based on Bell's Law, Wireless Sensor Networks (WSNs) are perceived as the next big step in the decades-long trend toward smaller, more ubiquitous computing. A WSN consists of distributed autonomous sensor nodes to monitor the environment conditions

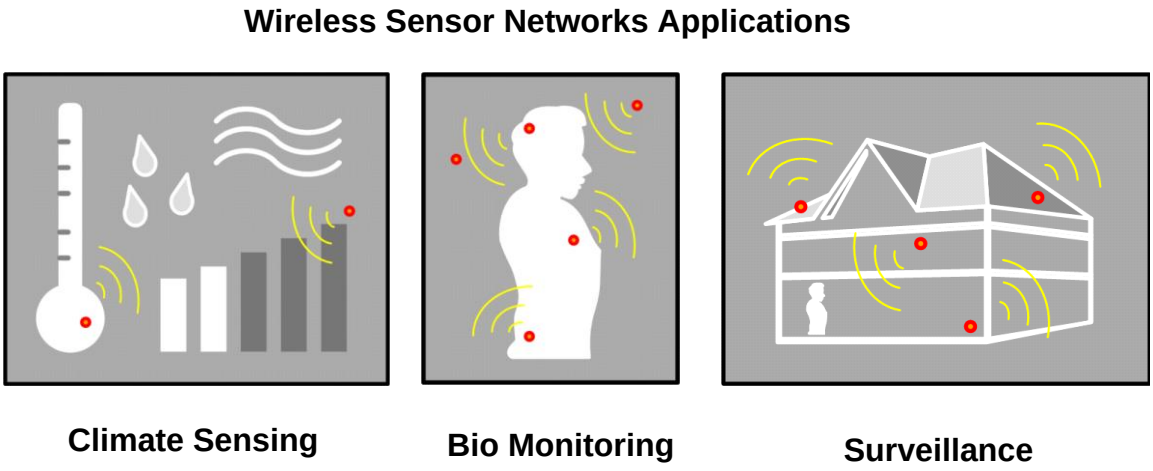


Fig. 1.2. Wireless Sensor Networks applications.

around them, such as temperature, vibration, imaging, and sound, etc. Each node is made up of components to process, sense, and communicate with other nodes in the network, and to cooperatively pass their data through the network to a main location. When deployed in the field, an ad hoc mesh network is created for relaying information to and from the gateway node [4]-[8]. This characteristic thus eliminates the need for costly and obtrusive wiring between nodes, allows nodes to be deployed in almost any location, which is promising for many applications (Fig. 1.2). Comparing WSNs with traditional wireless sensing technologies, it has the advantage of using the mesh networking scheme, therefore consumes less power than direct communication between node and base station which will be far away from each other. As a result, the sensing coverage of WSNs is better than conventional wireless sensing technologies using star topologies [7]-[8].

A variety of WSNs applications have been developed, demonstrating promising results for ubiquitous usages. A WSN platform is implemented for greenhouse microclimatic condition controlling in [10]. Climate monitoring is vitally important to the operation in

greenhouses, and the quality of the collected information has a great influence on the precision and accuracy of control results. For traditional climate monitoring and control systems, all sensors are distributed through the greenhouse and connected to the device performing the control tasks. These equipments use time-based data sampling techniques as a consequence of using time-based controllers. A more dynamic control algorithms and sampling techniques are implemented, realizing a WSN for each node to be programmed with different sampling and control algorithms. Therefore, overall performance of the greenhouse climate control is optimized.

Another example of WSNs application is monitoring the corrosion of steel rebar used in concrete bridges [11]. For this specific purpose, the design is completely wire-less for both data and power transmission because the nodes are embedded into the concrete. The control algorithm ensures minimum usage of energy source in each node for long life time. Hundreds of cost-effective nodes along a bridge provide the environmental data via interrogation units. The data is used to assist highway maintenance engineers in planning remediation and bridge deck repairs long before the need for total deck replacement.

Recently, many biomedical applications utilize WSNs for embedded monitoring. For example, an intraocular pressure (IOP) monitor was realized in [12] and [13], which measures the eye pressure for glaucoma diagnose. For implant and continuous monitoring purpose, the sensor node is completely integrated into a $1.5mm^3$ volume with a $1mm^2$ thin-film battery, showing a lifetime at least for weeks is feasible. This provides doctors with an accurate picture of the eye pressure during normal daily activities. It also allows customized medication to determine patient compliance with the prescribed medication regime.

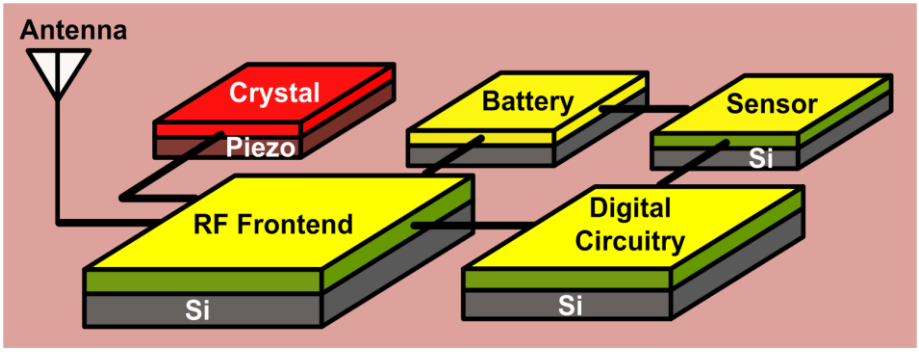


Fig. 1.3. Block diagram for a typical WSN node.

From the previous examples mentioned in the section, we know that WSNs applications vary widely in different fields. However, it is apparent that the hardware design plays an important role for specific purposes. Compact hardware size along with long lifetime is generally desirable, nonetheless, quite challenging. Next section will discuss the hardware design of WSNs.

1.2.2. Wireless Sensor Node

Fig. 1.3 shows the block diagram of a typical WSN node. An integrated WSN node generally has few sensors for multiple sensing functions, a digital processor for digital signal processing (DSP) and controlling, a radio frequency (RF) frontend and antennas for wireless communication, a battery as the energy source, and a crystal for frequency reference [4]. Fig. 1.4 summarizes the commercial integrated WSN node over past decade. We can see there is a clear trend of size reduction for the WSN nodes [14]. In the late 1990's, the WSN nodes are composed of multiple components on a printed circuit board (PCB) as shown in Fig. 1.4. The nodes consistently use commercial-off-the-shelf (COTS) components, and as a result, they are at tens of cubic centimeter scale. Assuming the trend in Fig. 1.4 continues, fully-integrated WSN nodes at mm^3 scale will be off-the-shelf in a very near future. Nonetheless, there are few bottlenecks in mm^3 WSN system

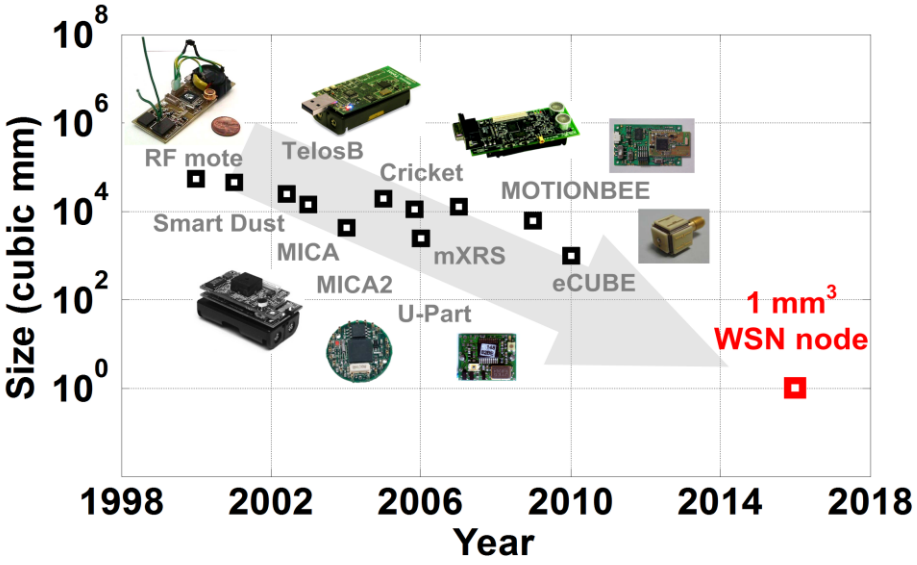


Fig. 1.4. Size reduction trend of integrated WSN nodes over years.

integration that need to be solved for simultaneous desire of long lifetimes and small volumes.

In general, the digital circuitry can be scaled down with advanced processes, and consume less power. Sensors can also be integrated onto the silicon substrate with the mainstream technologies to save area [1]. Moreover, size of RF front end and antennas can be shrunk by operating at a higher frequency. However, micro battery, crystal reference and antenna integration are the major issues for realizing integrated mm^3 WSN nodes. We will discuss those challenging issues in the following sections.

1.3. Micro-Battery

At mm^3 scale, micro-batteries have limited capacity and small peak current due to the direct relationship between capacity and volume [15]-[22]. For a 1.375 x 0.85 x 0.15mm custom lithium-ion (Li-ion) battery from Cymbet, the capacity is only 1µAh (Fig. 1.5) and the maximum discharge current is only 10µA [16]. The measured result presents

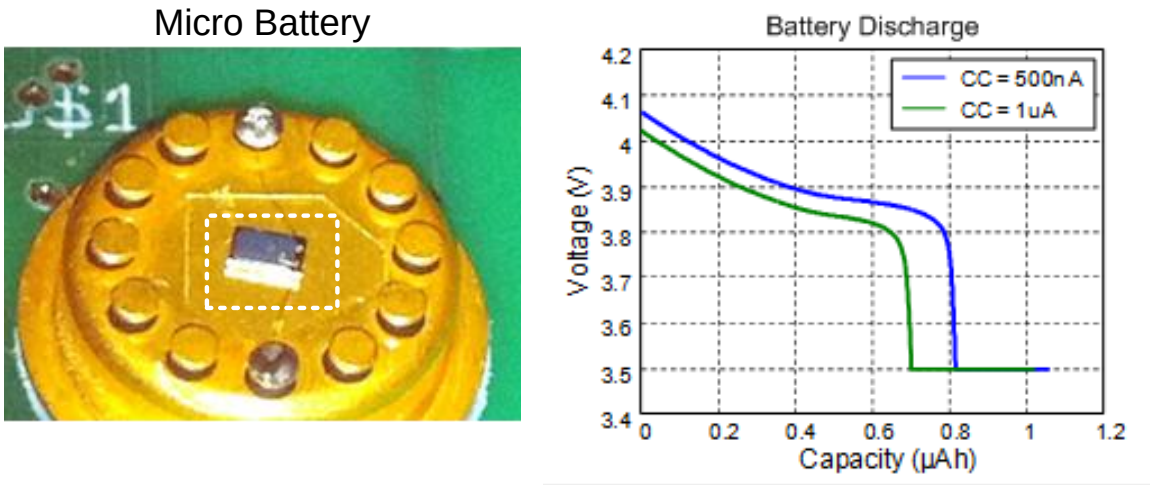


Fig. 1.5. Micrograph of the Cymbet micro-battery and its discharge curves.

direct challenges on the radio circuits, which typically consume > 100µW when active. As a result, for a node to survive longer, it either must be duty-cycled heavily, harvesting energy from other sources, or battery capacity must improve significantly. From a circuit design point of view, energy usage must be reduced by clever circuit techniques. The radio and oscillators easily dominate system energy usage if they are operated continuously to maintain synchronization for WSN nodes to communicate at the same frequency band [23], a phase-locked loop (PLL) with a crystal reference is usually necessary for the operation [24]. Thus, reducing the RF synchronization power consumption can greatly improve the WSN node lifetime; alleviate the burden of mm^3-scale micro-batteries.

1.4. Frequency References

A frequency reference provides a stable frequency over process, voltage and temperature (PVT) variations for synchronizations of a communication system. The accuracy depends on the system specifications [23], and can be implemented through different ways.

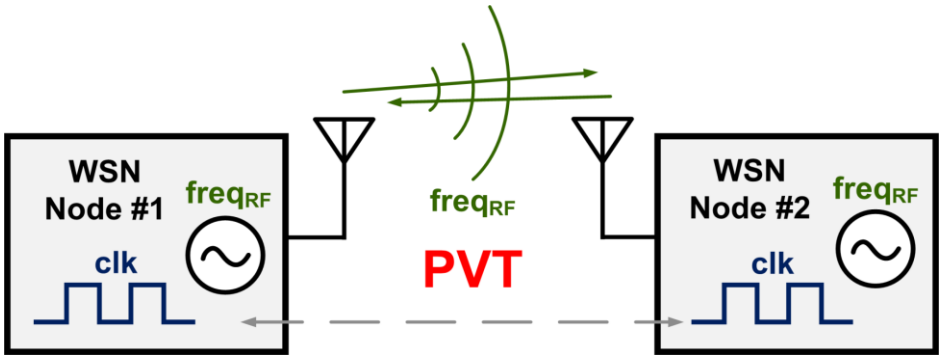


Fig. 1.6. Conceptual block diagram of synchronizations between two nodes in a WSN.

1.4.1. Synchronization in WSN Systems

Synchronization is critical to the overall functionality and power budget of a WSN [24]. There are two kinds of synchronizations need to be considered in the system: RF carrier synchronization, and baseband data synchronization. For RF synchronization, the WSN nodes must be able to talk to one another, which means, the RF center frequency band of each node should be close enough for the radios to receive and transmit signal properly. As mentioned earlier in Section 1.4, the synchronization accuracy depends on the system specification and modulation scheme. Non-coherent energy detection, which doesn't require a local oscillator, is a popular topology for receivers of WSN node because the severe energy constraint [14]. This topology also requires less accuracy on synchronization. We base on non-coherent energy detection topology, designed circuit with significant power reduction, meanwhile maintaining adequate frequency accuracy for synchronizations in WSNs.

1.4.2. Conventional Frequency References

Quartz crystal is the most common source for frequency reference. It provides excellent stability with PVT variations. However, it does not scale down with processes

	Crystal [26]	MEMS [27]	CMOS [28]
Manufacturer	Vectron International	SiTime	Silicon Labs
Volume	9.6 mm^3	4.5 mm^3	11.5 mm^3
Accuracy	25 ppm	50 ppm	150 ppm
Power	82.5 mW	72.6 mW	26.4 mW

Fig. 1.7. Comparison of compact frequency references.

nor frequency, and requires piezoelectric process which is incompatible with monolithic integration. In order to get stable oscillation out of crystals, certain amount of driving power is still necessary [25]. Therefore, the bulky size and cost of system integration become one of the bottlenecks for realizing mm^3-scale WSN nodes. Recently, MEMS and CMOS references are demonstrated with near-crystal accuracies [25]-[28]. Fig. 1.7 shows a comparison of compact frequency references made of crystal, MEMS and CMOS. All of their frequency accuracies are decent for WSN node specifications; however, none of their size is below $1mm^3$. Fig. 1.8 shows a COTS WSN node, TelosB [36]. A 32kHz crystal is highlighted in a red square, showing a significant volume out of the node. Note that the size does not scale because the resonance frequency of the crystal is fixed. The size ratio between crystal and the next generation WSN node will be worse once the node is miniaturized for future applications.

1.5. Antennas

Among the building blocks in a WSN node, the antenna plays a critical role because it is traditionally off-chip for better performance, and dominating the overall size of the

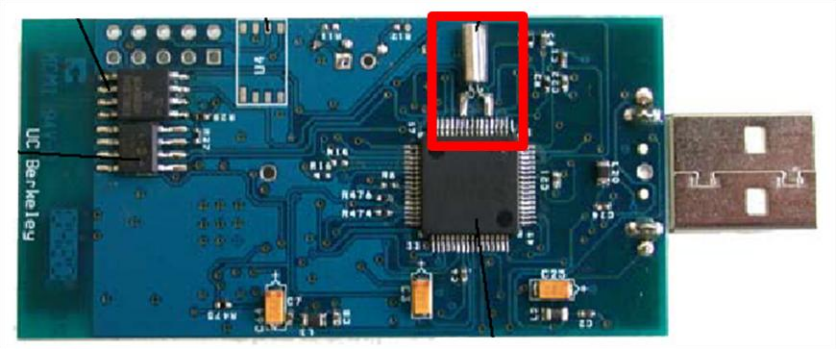


Fig. 1.8. A 32kHz crystal on WSN node, TelosB.

system. In this section, we will discuss about the integration of antenna and tradeoffs between antenna performance and center frequency.

1.5.1. Integrated Antennas

Integrated antennas have the size advantage over external packaged antennas. However, reducing antenna size results in reduced performance in general [46]. Antennas can be integrated directly on-chip, or at on-board level. At 1mm-scale, the operating frequencies need to be pushed up to 10GHz at least [14]. The parasitic loading of the package eliminates the possibility of using external antenna. Operating at higher frequency also creates important trade-offs. First, the path loss in the wireless channel increases [46]. As a result, more signal power is lost for a fixed communication distance. Second, the RF front end circuits that operate at these higher frequencies will consume more power. Therefore, reducing power consumption in RF front end components is critical from a system point of view. Fig. 1.9 shows a comparison table of the state-of-the-art antennas integrated with radio systems. Only on-chip antennas meet the mm^3 volume requirement. However, it is quite challenging to realize on-chip antennas with adequate performance. We will discuss about it in the next section.

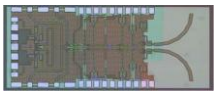
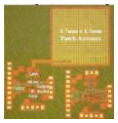
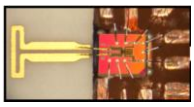
	On - Chip	On - Chip	Off - Chip
			
Reference	**[29]**	**[30]**	**[49]**
Frequency	**60 GHz**	**65 GHz**	**60 GHz**
Volume	**0.1 mm ^{3}**	**0.6mm ^{3}**	**4.5mm ^{3}**
Antenna Gain	**- 2.0dBi**	**- 8.5dBi**	**6.1dBi**

Fig. 1.9. Comparison of the state-of-the-art integrated antennas.

1.5.2. Challenges in CMOS Technology

CMOS technology is the mainstream nowadays due to its low cost, decent performance and ease of integration [1]. Nevertheless, there are several challenges for on-chip antenna integration. First, the area occupied by the antenna and the space for isolating the crosstalk between antenna and active circuits should be considered. Additionally, the lossy silicon P-substrate (~10Ω-cm) in a CMOS process degrades the antenna performance significantly because energy dissipates in the substrate instead of radiates into the air. Moreover, the design rules in CMOS technology such as metal slotting and density requirement also impact the antenna design. Fig. 1.10 shows a cross section of an on-chip CMOS patch antenna proposed in [45]. Space below the patch antenna is required for integrating custom circuits (e.g. DSP and memory) in a system-on-a-chip (SoC) application. Conventional digital circuits typically use 4 to 6 metal layers for wire routing; fewer metal layers of routing is feasible, but at the cost of lower circuit density. Consequently, the patch antenna is a good candidate for system

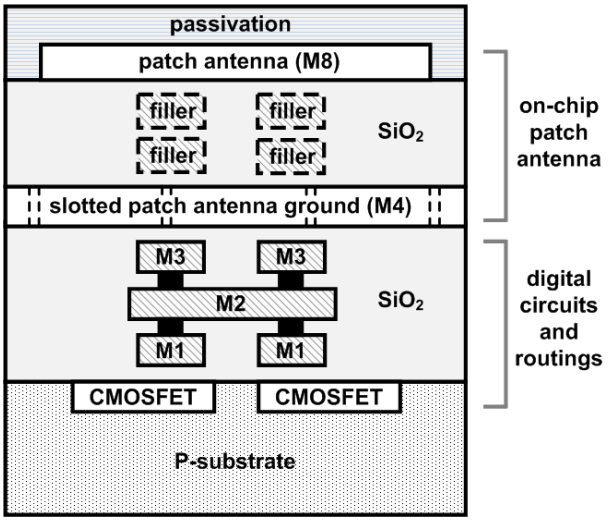


Fig. 1.10. Layout cross section of an on-chip patch antenna integrated in CMOS technology

integration in CMOS technology due to the better performance (ground shielding) and reusable area beneath the patch.

1.6. Goals and Contributions of this Work

For many WSNs applications, there is a desire for small volume and long lifetime simultaneously. Since RF front end easily dominates the whole volume and energy budget of a WSN node, both of its size and power consumption must be minimized. In addition, high power, bulky components like crystal oscillators and PLLs must be removed, which also helps to decrease node volume.

My research covers several aspects of the energy and integration challenges associated with mm^3-scale WSN nodes without crystal references. In particular, the goal of my research is to present several crystal-less frequency generation techniques for compact

and low-power RF radio systems. The research projects cover the RF synchronization and baseband data synchronization scope. The expected contributions are as follows:

1.6.1. 60GHz Antenna-Referenced Frequency-Locked Loop

I present the first Frequency-Locked Loop for WSNs using on-chip patch antenna as both the radiator and frequency reference. The proposed technique efficiently integrates the antenna, eliminates the need for a crystal reference, is FCC compliant, and ensures the node transmits at the antenna's peak efficiency. The substrate beneath the antenna is shielded by an intermediate metal layer ground plane, freeing up space for active circuits and routing beneath the patch. By integrating circuits in CMOS underneath the patch, and stacking the die on e.g., a thin-film battery, a fully integrated, cost-effective, mm^3-scale WSN node is feasible.

1.6.2. 10GHz IR-UWB Transmitter

I present an ultra-wideband transmitter (TX) optimized for cubic-mm sensor nodes. Unlike recently published UWB TXs, this TX operates at the voltage range of a lithium-ion micro-battery to save power. In addition, the entire TX, including bias currents, can be heavily duty-cycled at bit-level, so that the average current draw from the battery is less than 10μA. During transmission, the TX draws maximum on-current to generate the largest signal possible for the longest communication distance for efficient energy usage.

1.6.3. 1.2MHz Temperature-Compensated Relaxation Oscillator

I present a low-power; temperature-compensated relaxation oscillator for mm^3 WSN node clock generation. An RC network of the oscillator is proposed with a transmission zero for temperature compensation. It introduces an additional degree-of-freedom for relaxation oscillator design and maintains temperature compensation over a frequency

tuning range using conventional CMOS resistor and capacitor options. The oscillator offers a good balance between power, area, oscillation frequency, frequency stability and leakage power, which are all critical specifications for mm^3 WSN applications.

1.6.4. 60GHz T/R Switch-Less Antenna Front-End

I present a 60GHz transmit/receive (T/R) switch-less antenna front-end for the realization of mm^3 WSN nodes. With proper arrangement taking advantage of the linear polarization of the on-chip square patch antenna, there is an embedded T/R isolation without the need of a T/R switch, which is non-trivial at mm-wave range. The TX port and RX port of a square patch antenna either transmit or receive data at any given time from two orthogonal feeds. This location arrangement puts the RX port on the electrical null of the standing wave pattern when TX is transmitting, and vice versa. Thus, the T/R isolation is embedded (>30dB) and the loading effect of TX and RX can be minimized at operation frequency. The proposed technique eliminates the on-chip high frequency switch with decent isolation, loss, and linearity. As a result, the volume of the WSN radio system can be minimized toward mm^3-scale.

Chapter 2
On-Chip Patch Antenna and Standing Wave Pattern

This chapter presents the design considerations of a patch antenna and the fundamental theory of the patch antenna topology. Basics of the transmission line model are discussed as the preliminary study to understand the operation of a patch antenna. Furthermore, analysis of the standing wave pattern on the patch antenna is presented, and serves as the key characteristic for further applications in the next chapters.

2.1. Introduction

Microstrip patch antennas are popular for low-profile applications due to the fact that they are structurally compact and conformal [46]. One of the most common topologies is the rectangular patch. Fig. 2.1 shows a typical rectangular patch antenna with parameters

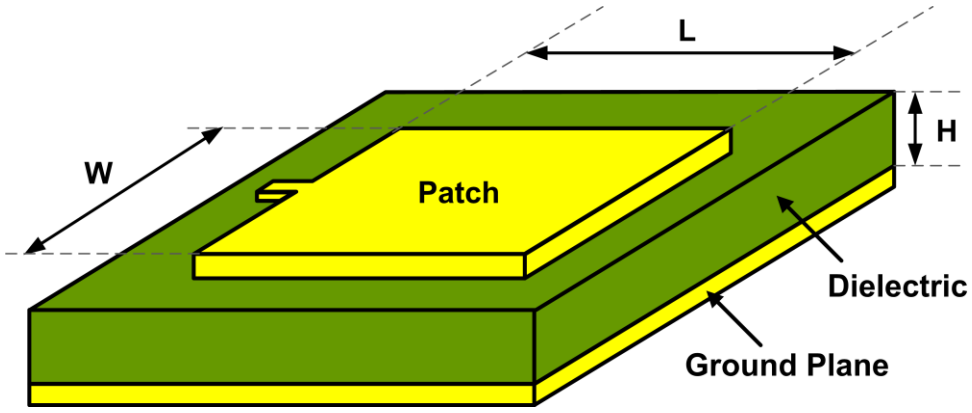


Fig. 2.1. A typical patch antenna with design parameters.

W as width, L as length, and H as height. The patch is generally made of conducting material and over a ground plane separated by a dielectric substrate; ideally a finite ground plane with perfect conductivity. For a rectangular patch, the length L of the patch is usually a little bit less than $\lambda/2$, where λ is the free-space wavelength of the operation frequency. The patch thickness is selected to be very thin such that it is much smaller than one λ. The height H of the dielectric substrate is usually $0.003\lambda < H < 0.05\lambda$ [46]. A microstrip patch antenna radiates primarily because of the discontinuity at the edge, basically the fringing fields between the patch edge and the ground plane. In general, a think dielectric substrate with a low dielectric constant is desirable for better antenna performance (radiation efficiency and bandwidth).

The microstrip patch antenna topology has a relatively high antenna quality factor (Q) [46]. Q represents the losses associated with the antenna and a large Q leads to narrow bandwidth and low efficiency. Q can be reduced by increasing the thickness of the dielectric substrate. But as the thickness increases, an increasing fraction of the total power delivered by the source goes into a surface wave [46]. This surface wave contribution can be counted as an unwanted power loss since it is ultimately scattered at the dielectric bends and causes degradation of the antenna characteristics.

Moreover, microstrip patch antennas can be fed by different methods. These methods can be classified into two categories: contacting and non-contacting. In the contacting method, the RF power is fed directly to the radiating patch using a connecting element such as a microstrip line. In the non-contacting scheme, electromagnetic field coupling is

done to transfer power between the microstrip line and the radiating patch. The four most popular feed techniques used are the microstrip line, coaxial probe (both contacting schemes), aperture coupling and proximity coupling (both non-contacting schemes). In the dissertation, microstrip line feeding from the edge will be the focus method of feeding as shown in Fig. 2.1. In this way, a conducting strip is connected directly to the edge of the microstrip patch. The conducting strip is smaller in width as compared to the patch and this feed arrangement has the advantage that the feed can be etched on the same substrate to provide a conformal planar structure, which fits well in CMOS technology.

2.2. Transmission Line Model

A microstrip patch antenna can be analyzed using a transmission line model. It basically treats the patch as a very wide microstrip transmission line with two slots at the source and load ends. The electric field varies sinusoidally under the patch along L, creating a standing wave pattern. The electric field is assumed to be invariant along the width W of the patch. Furthermore, it is assumed the radiation of the antenna comes from the fields leaking out along the width, which are the two slots serve as the radiating edges. As a result, most of the electric field lines reside in the dielectric substrate and parts of some lines in air. The transmission line cannot sustain a transverse-electric-magnetic (TEM) mode of propagation, because the phase velocities will be different in the substrate and in the air. The dominate mode is the quasi-TEM mode. Therefore, an

effective dielectric constant (ε_{eff}) needs to be obtained for further analysis ($f_{resonance}$, dimensions). The expression of ε_{reff} is [46] :

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{\frac{-1}{2}} \tag{1}$$

with the center frequency, f_0, dielectric constant of the silicon dioxide (SiO2), ε_r, and the height h, we can calculate the width, W, of the patch antenna by antenna theory for a better efficiency

$$W = \frac{c}{2 f_o \sqrt{\frac{(\varepsilon_r + 1)}{2}}} \tag{2}$$

where c is the speed of light. With the calculated W, It follows that the length of the patch antenna, L is

$$L = \frac{c}{2 f_o \sqrt{\varepsilon_{reff}}} - 0.824h\frac{(\varepsilon_{eff} + 0.3)(\frac{W}{h} + 0.264)}{(\varepsilon_{eff} - 0.258)(\frac{W}{h} + 0.8)} \tag{3}$$

Note that the size of the ground plane is greater than the patch dimensions by approximately six times the height all around the periphery to achieve results similar to that of an infinite ground plane [46]. As a result, the dimension of the on-chip patch antenna can be calculated given an operation frequency from the transmission line model.

In order to operate in the fundamental TM_{10} mode, the length of the patch is close but slightly less than $\lambda/2$. Also, the TM_{10} mode implies that the electric field varies one $\lambda/2$ cycle along the length L. In other words, the electric potential is at the maximum and the

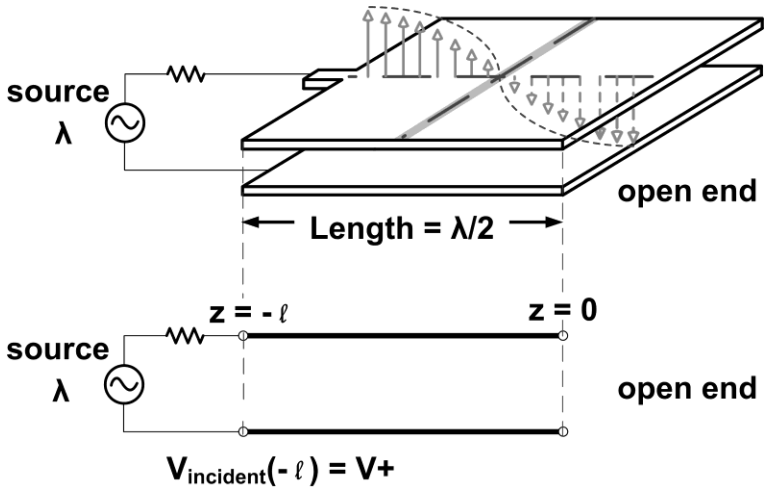


Fig. 2.2. Simplified lossless transmission line model of the patch antenna.

current is at a minimum at the two slots due to the open ends. Furthermore, a simplified lossless transmission line model is adopted for this analysis. Fig. 2.2 shows the transmission line model corresponding to the patch antenna along the length axis. The feed point serves as the source terminal, while the other edge behaves as the open end. When the source frequency is exactly at the resonant frequency, the length of the transmission line is equal to λ/2, and a standing wave pattern is generated by the superposition of the incident wave from the source and the reflected wave from the load. Under these conditions, the patch antenna radiates at its peak efficiency value. The source end and open end have the strongest electric fields, and those are the radiation edges. Note that there is an electrical null located in the center of the length axis (e.g. z = -l/2),

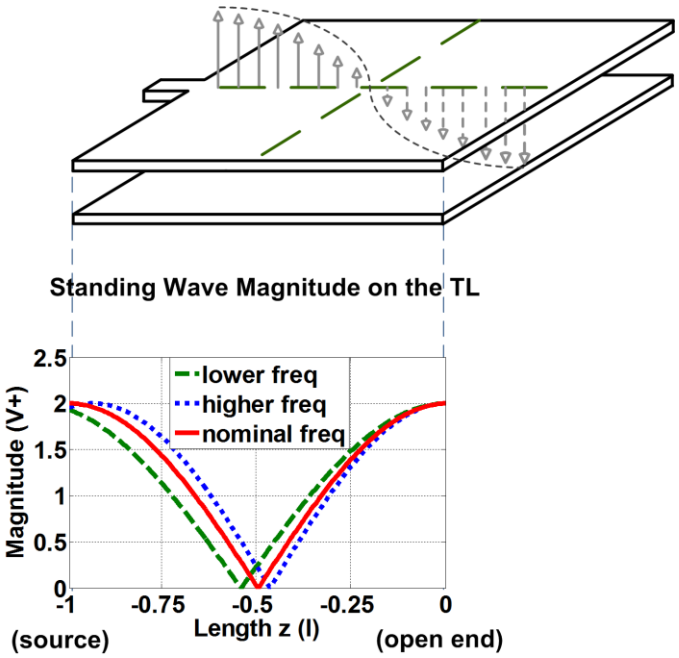


Fig. 2.3. Standing wave patterns at different frequencies.

shown as the solid shaded area in Fig. 2.2. The amplitude of the standing wave on the transmission line as a function of the length can be written in the general form [47]:

$$V(z) = V^{+}\left(e^{-j\beta z} + \Gamma e^{j\beta z}\right) \tag{4}$$

where V^{+} is the incident wave magnitude at z = 0, β is the propagation constant $2\pi/\lambda$, and Γ is the voltage reflection coefficient. When the load is open, Γ equals 1, thus the magnitude of the standing wave reduces to

$$\left|V(z)\right| = \left|V^{+}\right|\sqrt{\left[2 + 2\cos\left(2\beta z\right)\right]} \tag{5}$$

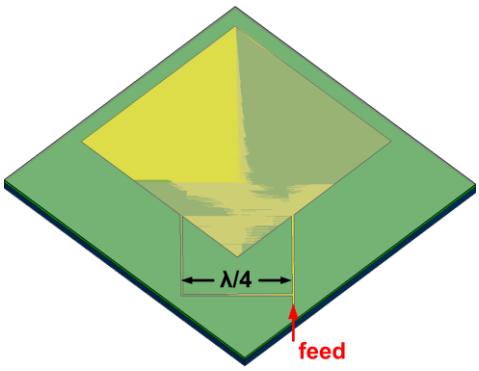


Fig. 2.4. Feeding with 90° difference to generate circular polarized radiation on the patch antenna.

Fig. 2.3 shows the magnitude plot of three standing wave patterns corresponding to three different source frequencies. Due to the open end boundary condition ($\Gamma = 1$ for an open load, the magnitude will remain the same at $z = 0$) and different λ according to different frequencies, the location of the electrical null moves along the transmission line length as frequency changes. When the source frequency is lower than the resonant frequency, the electrical null moves toward the source end. On the other hand, the electrical null will move toward the open end if the source frequency is higher than the resonant frequency as shown in Fig. 2.3. Also, at a given frequency, the source impedance would not change the null position, which is mainly determined by the geometry of the patch. However, it will affect the matching of total power delivered to this transmission line resonator, thus the absolute magnitude of the standing wave pattern.

2.3. Circular Polarized Patch Antenna

In the previous section, the linear polarized characteristics of a patch antenna are discussed based on the transmission line model. As a matter of fact, circular polarized

antennas are required for many wireless applications so as to maintain reliable communication regardless of antenna positioning [46]. A single square patch can support two degenerate modes at the same frequency with the radiated fields linearly polarized in orthogonal directions. Circular polarization can be accomplished by using a proper feed network with a 90° offset for the two feeding points on the patch antenna, as shown in Fig. 2.4. In this section, we do care about how the electrical field pattern will change as opposed to the linear polarized case. Moreover, we would like to know the location of the electric null as source frequency changes. Fig. 2.5 shows the electric field distribution in one cycle of a circular polarized patch antenna. The electric null line is rotating over time, which is consistent with the circular polarization effect. The only non-changed point of the electric null is the geometric center of the patch. However, as the source frequency changes, the non-changed point of the electric null does not move much compared to what we observed in the linear polarized case, as shown in Fig. 2.6 at 2.5% lower than the resonance frequency. This is an important observation for the applications in the following chapters.

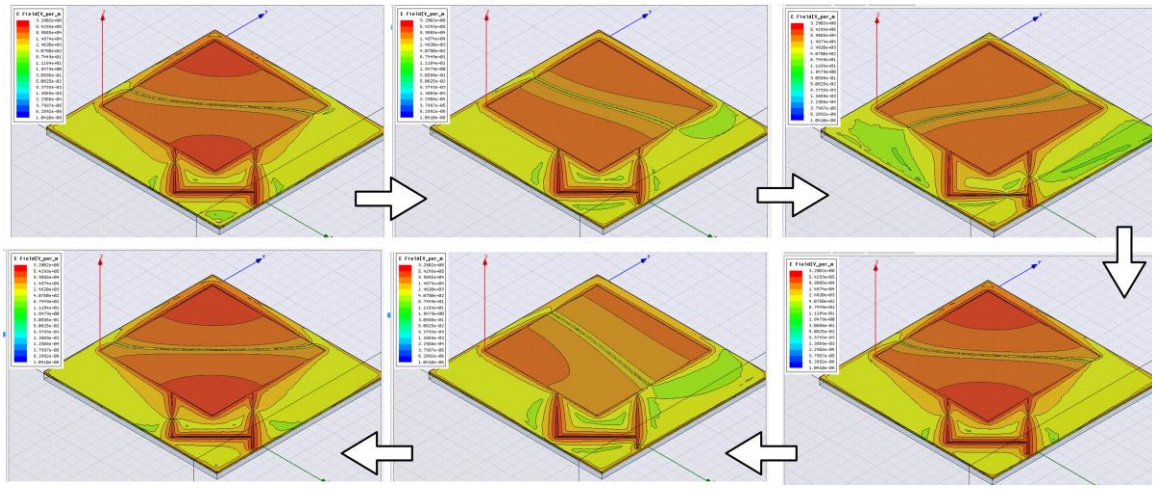


Fig. 2.5. Electric field distribution in one cycle of a circular polarized patch antenna at its resonance frequency.

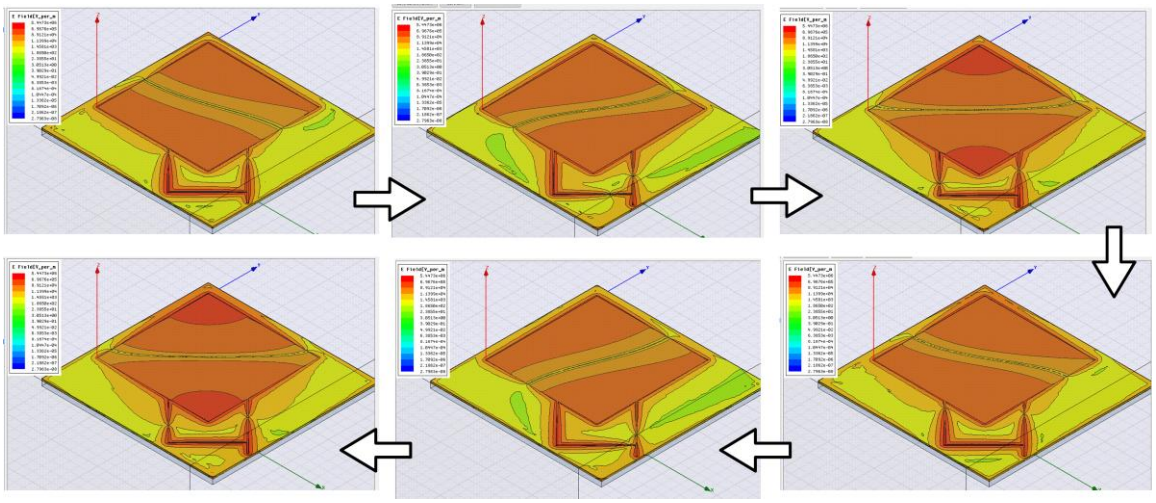


Fig. 2.6. Electric field distribution in one cycle of a circular polarized patch antenna 2.5% below its resonance frequency.

2.4. Limitations of the Patch Reference

As we discussed earlier in this chapter, the patch antenna can be analyzed through the transmission line model. The electric null position of its standing wave pattern will move according to the source frequency (due to the boundary condition at the open end and the changing wavelength). The characteristic is promising for resonance frequency detection of the patch antenna. In this section, we will discuss the limitations of the patch frequency detection. Finite metal conductivity is one of the main issues. The conduction loss will affect the standing wave pattern, causing the quality factor Q to reduce, and thus reduce the accuracy of frequency detection. We can start with the lossy transmission line model [47]

$$V(z) = V^{+}\left(e^{-\gamma z} + \Gamma e^{\gamma z}\right) \tag{6}$$

where λ is the propagation constant of the wave equation and it can be present as

$$\gamma = \alpha + j\beta = \sqrt{(R + jwL)(G + jwC)} \tag{7}$$

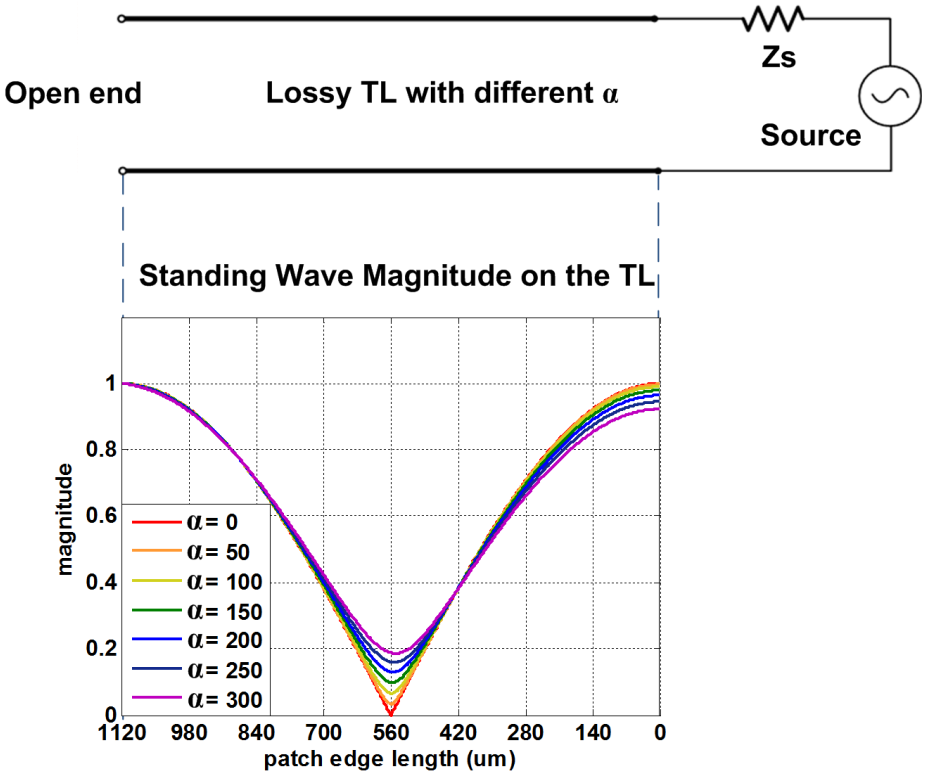


Fig. 2.7. Magnitude of standing wave pattern on a lossy transmission line with different attenuation constant α.

here α is the attenuation constant (Nepers/m) and β is the phase constant ($2\pi/\lambda$). The lumped R, L, G, C represents the unit length resistance (Ohms/m), inductance (Henries/m), conductance (Siemens/m) and capacitance (Farads/m) of the transmission line. In the following discussion, we will use the attenuation constant α in the analysis since it is a general expression for loss. Fig. 2.7 shows the magnitude plot versus the location on the transmission line model (patch edge) with different α (Γ=1 due to the

open end). Note that the electric null degrades as α increases and so does the Q of this transmission line resonator. The reason is because the standing wave pattern is constructed by the super position of the travelling and reflecting wave on the transmission line, and they will experience different attenuation as they propagate through the transmission line. The difference is larger with larger α, causing the null to disappear in the center of the length. In this case, the minimum of the standing wave pattern shifts and includes an asymmetry, causing a frequency shift from the nominal center frequency ($L=\lambda/2=C/2f_{nom}$). Note that when we sample the amplitude at two points along the length that they are equal distance away from the ideal null at resonance (ex: Fig. 2.7. when at patch length equal to 700μm and 420μm, they are symmetrical to the null at 560μm), the magnitude at the corresponding two points should be equal because the symmetry of the standing wave pattern at λ/2. In other words, if we take the difference in magnitude of these two points, the result should be zero. With the propagation constant with attenuation constant discussed in (7), we can further derive the difference in magnitude of the two points as (assuming they are 0.02λ apart from the null center) from the wave equation (6)

$$dV = V^{+}\left(e^{-(\alpha+j\beta)z_1} + \Gamma e^{(\alpha+j\beta)z_1}\right) - V^{+}\left(e^{-(\alpha+j\beta)z_2} + \Gamma e^{(\alpha+j\beta)z_2}\right) \qquad (8)$$

where the value of z_1 and z_2 are 0.23λ and 0.27 λ, respectively. Note that dV is a function of alpha and frequency, and the solution for resonance frequency is defined

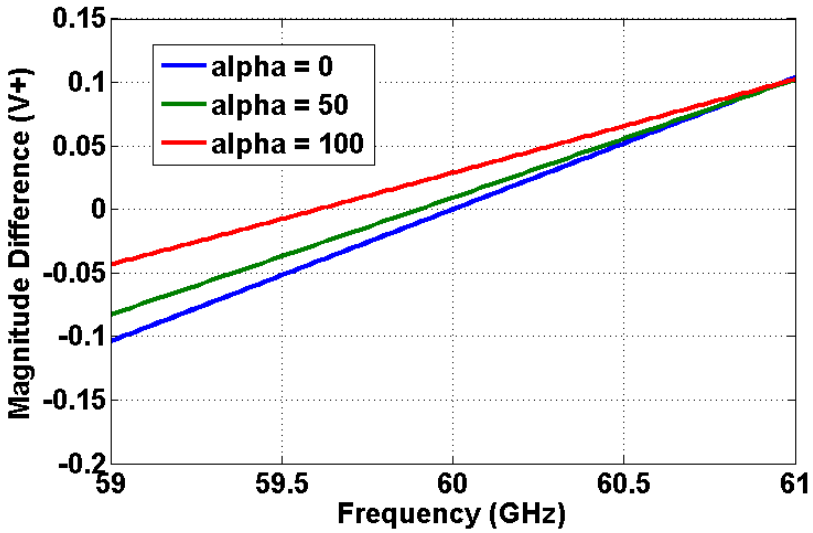


Fig. 2.8. Difference in magnitude on two points that are equal distanced away from the null center. Three cases with different alpha values are shown.

when dV equals to zero. Fig. 2.8 shows the difference in magnitude with three different values of alpha. When alpha is zero, this becomes the loss-less transmission line case, showing a difference of zero at nominal frequency (60GHz). When the loss gets larger, the center frequency needs to shift higher so as to compensate and make the magnitude difference equal to zero as shown in Fig. 2.7. As a result of putting this antenna in a frequency lock loop that tracks the frequency when this voltage difference equals zero, the loss causes the resulting center frequency to shift. Fig. 2.9 further shows the frequency shift versus α in the case where the distance of z_1 and z_2 is equals 0.02λ. Therefore, conductions losses increase the inaccuracy of resonant frequency detection.

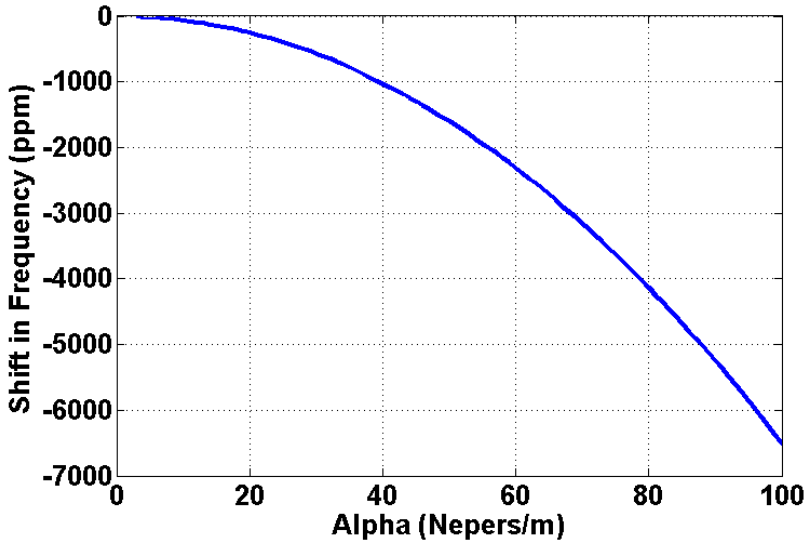


Fig. 2.9. Frequency shift versus α in the case where the distance of z_1 and z_2 is equals to 0.02λ.

A higher Q transmission line resonator is desirable because the loss is reduced, making the electrical null become more like an ideal notch in Fig. 2.7. In this case, there is less of an obscure region and less frequency shift for resonance frequency detection.

Another important issue when using the patch antenna as a frequency reference is the frequency detection range. From the previous discussion, we know that the differences in magnitude of two symmetry points along the length can potentially be used for frequency detection. If we plot the difference versus frequency like in Fig. 2.8, there is a monotonic curve passing through zero, where the resonance frequency is. However, the curve is not always monotonic, and a non-monotonic curve will cause the instability in a closed-loop frequency detection circuit. From the loss-less transmission

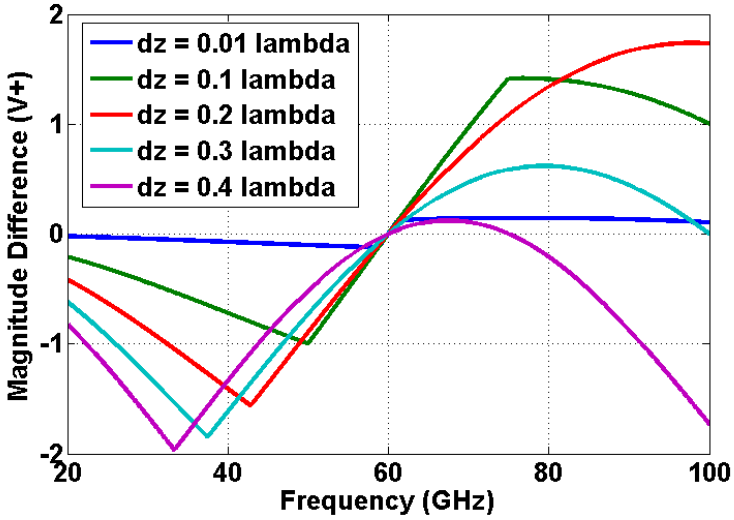


Fig. 2.10. Difference in magnitude on two points that are equal distanced away from the null center. Three cases with different dz values are shown.

line equation (5), we can derive the difference in magnitude expression in terms of frequency and the distance between the two points, dz as

$$dV = \left|V^{+}\right|\left[\sqrt{\left[2+2\cos\left(\frac{4\pi\left(\lambda_0/4+dz/2\right)f}{C}\right)\right]}-\sqrt{\left[2+2\cos\left(\frac{4\pi\left(\lambda_0/4-dz/2\right)f}{C}\right)\right]}\right] \quad (9)$$

where λ_0 is the wavelength at the nominal frequency, and C is the speed of light. From (9), we know that dz affects dV significantly. The frequency detection range is defined as the range over which (9) is monotonic. This can further be defined as the range between the frequencies which cause the derivative of (9) to equal zero. There is no closed-form expression of this range, however, we can use a numerical plot to find the extremes, tracing the difference in magnitude curves until they are no longer monotonic versus

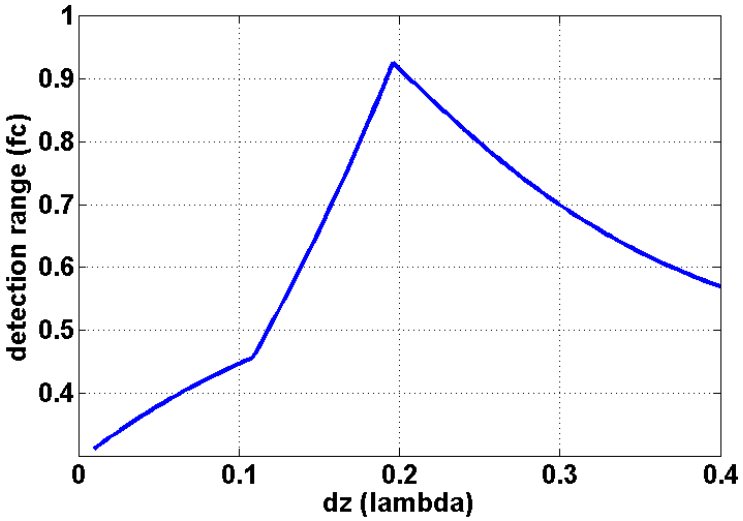


Fig. 2.11. Frequency detection range versus dz

frequency. Fig. 2.10 shows the curves for different values of dz, where the monotonic range of the curve defines the frequency detection range of each dz case. Furthermore, Fig. 2.11 shows the frequency detection range versus dz, showing that larger dz results in larger monotonic range. However, there is a peak around lambda/5 due to the interaction between the open-end and the source-end boundary conditions on the standing wave pattern. In conclusion, a wider separation between the two points provides a larger range of the monotonic curve for frequency detection by a lossless transmission line model. However, the matching condition of the transmission line needs to be considered (we assumed perfectly matched over the whole spectrum for previous case), and that will change the standing wave plot and thus the lock-in range. Nevertheless, the matching

condition should be negligible near the center frequency (±2% of fc). Practically, if dz is too wide for a target frequency range, the monotonic characteristic no longer applies, which could result in instability. We will further discuss the issue in the following chapter.

Chapter 3
60GHz Antenna-Referenced Frequency-Locked Loop

This chapter presents a 60GHz frequency-locked loop (FLL) for wireless sensor network applications. The FLL incorporates an on-chip patch antenna as both a radiator and a frequency reference, realizing a compact and low-cost solution for non-coherent energy detection radios. To further reduce the size of a wireless sensor node, the area beneath the patch antenna ground plane is utilized for analog and digital baseband circuitry integration. A sensor array was implemented beneath the antenna ground plane to measure the spatial coupling from the antenna to the circuitry beneath it. The FLL is fabricated in a 0.13μm CMOS technology. The operating frequency is locked to the maximum-efficiency point of the antenna with a mean of 59.34GHz and standard deviation of 195MHz over process variation. The circuit and antenna occupies 2.85mm^2 and consumes 29.6mW.

3.1. Introduction

The tendency towards smaller wireless sensor network (WSN) nodes has opened the possibilities of ubiquitous and unobtrusive sensing applications [31]-[33]. Over the past decade, researchers in both academia and industry have reduced the size of fully-integrated WSN systems by nearly two orders of magnitude. Fig. 3.1 summarizes the sizes of WSN node prototypes published in literature or commercially available versus year, showing the trend in size reduction of integrated WSNs [31]. Vanishingly-small, fully-integrated systems at the cubic millimeter scale represent the future of WSNs [31],

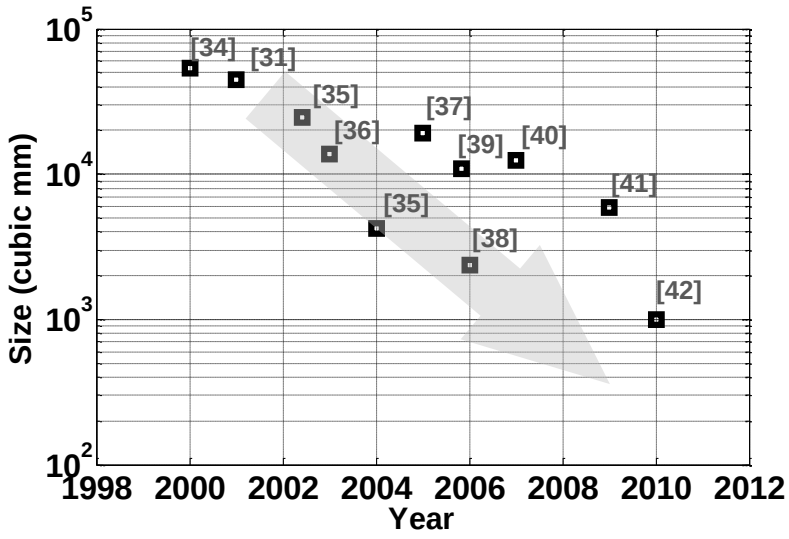


Fig. 3.1. Trend on size reduction of integrated WSN systems

[32], but present several integration challenges that may not be solved by CMOS scaling alone.

Conventionally, a WSN node is equipped with a radio transceiver, antenna, digital microcontroller, sensors, energy source such as a battery, and a crystal reference. Among all these building blocks, the RF front end and antenna could be scaled down in size by operating at a higher frequency due to the inverse proportional relationship to wave length. The digital circuitry could be scaled down in size by using advanced processes. Sensors for monitoring inertia, temperature, imaging, gravimetry, and chemical reactions can be integrated with CMOS technology on one silicon substrate [43]. The required battery volume could be reduced with the use of low-power or heavily duty-cycled circuit design [44], and thin film zinc/silver oxide batteries can be fabricated today that fit a $1mm^2$ form factor. However, there is currently no clear path to shrinking the size of the crystal reference oscillator and integrating it in a CMOS process with low power and low cost. Therefore, the crystal reference is one of the bottlenecks to realizing an extremely

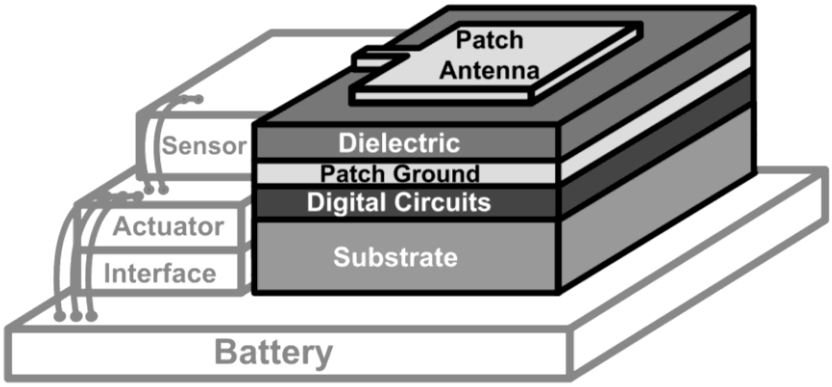


Fig. 3.2. Miniature, fully-integrated wireless sensor node system.

small WSN node, and crystal replacement with e.g. CMOS or MEMS oscillators is currently an active area of research. Additionally, an external antenna, requiring custom packaging, is an obstacle that prohibits scaling to $1mm^3$ volumes.

In order to eliminate the bulky off-chip components and further reduce the size of a fully-integrated WSN node, we present a solution of using a 60GHz on-chip patch antenna as both the radiator and frequency reference in this paper. The natural resonant frequency of the patch antenna serves as the frequency reference. At 60GHz, the guided wave length is around 2.5mm in silicon, which is comparable to the size of the active circuit blocks (e.g. radio, processor, and memory), and it operates in the 57-64GHz industrial, science and medical (ISM) band approved for unlicensed communication by Federal Communications Commission (FCC). The resonant frequency is mainly determined by the physical dimensions of the patch antenna, and the standard deviation, σ, due to process variation is around 1100ppm. This accuracy level is suitable for e.g. low-rate communication with a non-coherent energy-detection receiver. With the antenna reference, we fabricated a frequency-locked loop (FLL) circuit to track the reference frequency for RF synchronization. Furthermore, the area beneath the patch antenna

ground plane is investigated for containing additional circuits for higher integration. The mutual coupling between the antenna and the circuits beneath are tested by a coupling sensor array and a clock generator with a 16-node H-tree, showing that the 60GHz patch antenna and the digital clock switching circuitry routed beneath the patch antenna can functionally work with the antenna ground plane shielding. Fig. 3.2 depicts the concept of a miniature WSN node system. By integrating the antenna, frequency reference, RF front end, and digital circuitry onto the same die, a form factor of $1mm^3$ is feasible.

3.2. Antenna Reference

3.2.1. Patch Antenna Design

As an on-chip radiator, the patch antenna topology is chosen because its ground plane shields the patch antenna from the lossy substrate in standard CMOS processes, and thus provides higher radiation efficiency than non-shielded integrated antennas. Moreover, the patch antenna is also a good candidate for system integration due to the reusable area beneath the ground plane for high noise margin digital circuits. In our design, we first determine how many metal layers are typically needed for digital circuit routings. The distance between the patch metal layer (top-metal M8) and the ground metal layer determines the height of the patch antenna. The tradeoff between radiation efficiency and height are discussed in [45]. The analysis suggests that lower antenna height (or a higher metal layer ground plane) results in lower radiation efficiency. In this design, Metal 4 is used as the ground plane, resulting in an antenna height of 14.1 μm. Based on simulations, using Metal 4 for the ground plane instead of Metal 1 reduces the radiation efficiency by 15%, but frees up three metal layers for routing of circuits beneath the

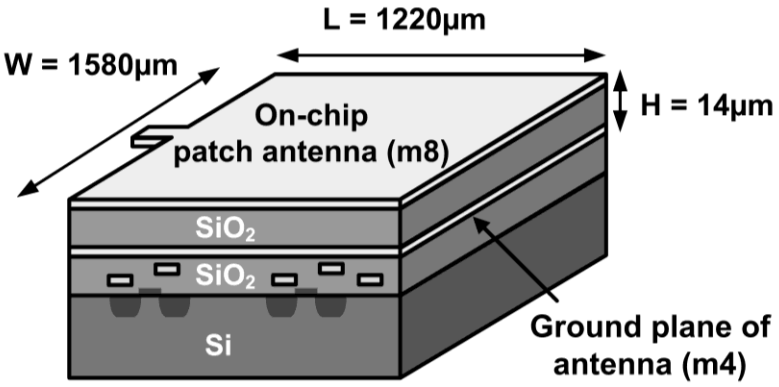


Fig. 3.3. Dimensions of the 60 GHz patch antenna.

antenna. With the knowledge developed in Chap. 2, Fig. 3.3 illustrates the final dimensions of the patch antenna. The resonant frequency is mainly determined by the width and length which can be verified by back calculating for f_0 from (1)-(3) when W and L are known. The 3σ process variation parameters on length and width of the top metal layer are on the order of 400 ppm of the antenna parameters, resulting in the same order of accuracy of the resonant frequency of the patch antenna, determined by the first-order antenna theory. The simulated antenna radiation pattern is shown in Fig. 3.4. The simulation results include the effects of required dummy filling for meeting local metal density requirements, dielectric loss of the SiO_2 insulator (loss tangent = 0.001), and show the center frequency is 60.54 GHz with a bandwidth of 920 MHz. The peak antenna gain is -3 dB while the efficiency at resonance is 15.6%. As a resonator, the quality factor Q is approximately equal to 66 at resonance.

3.2.2. Resonant Frequency Detection

To detect the resonant frequency of the antenna reference, we will need to understand the physical phenomena on the patch antenna when it is resonating. Recalling from Chap.

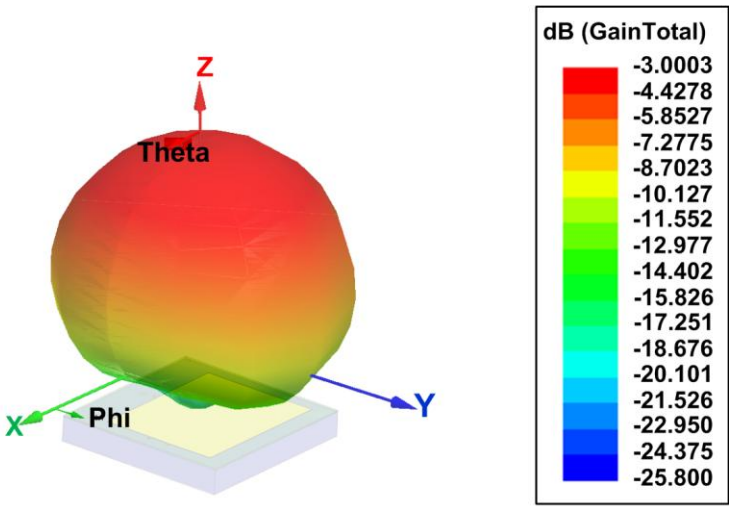


Fig. 3.4. Radiation pattern of the on-chip patch antenna.

2, a simplified lossless transmission line model is adopted for this analysis. Fig. 3.5 shows the transmission line model corresponding to the patch antenna along the length axis. We may consider the patch antenna a very wide transmission line, with the feed point being the source terminal, while the other edge behaves as the open end. When the source frequency is exactly at the resonant frequency, the length of the transmission line is equal to λ/2, and a standing wave pattern is generated by the superposition of the incident wave from the source and the reflected wave from the load. Under these conditions, the patch antenna radiates at its peak efficiency value. The source end and open end have the strongest electric fields, and those are the radiation edges. Note that there is an electrical null located in the center of the length axis (e.g. z = -l/2), shown as the solid shaded area in Fig. 3.5. The amplitude of the standing wave on the transmission line as a function of the length can be written in the general form [47]:

$$V(z) = V^{+}\left(e^{-j\beta z} + \Gamma e^{j\beta z}\right) \tag{4}$$

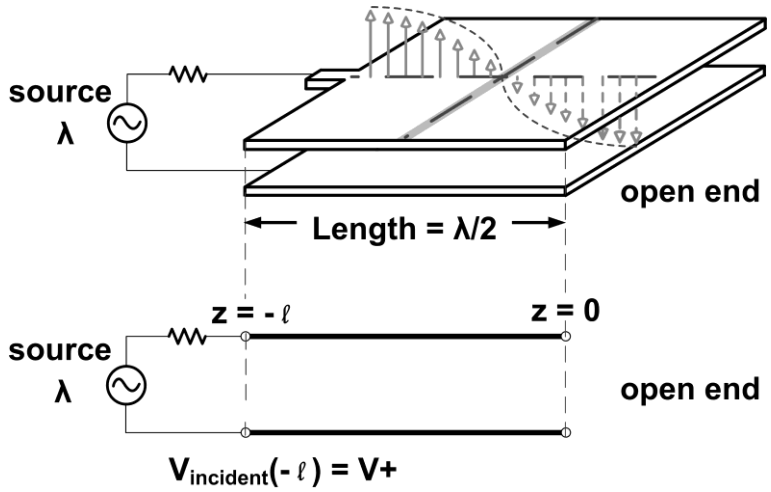


Fig. 3.5. Simplified lossless transmission line model of the patch antenna.

where V^+ is the incident wave magnitude at z = 0, β is the propagation constant $2\pi/\lambda$, and Γ is the voltage reflection coefficient. When the load is open, Γ equals 1, thus the magnitude of the standing wave reduces to

$$|V(z)| = |V^+|\sqrt{[2 + 2\cos(2\beta z)]} \tag{5}$$

Fig. 3.6(a) shows the magnitude plot of three standing wave patterns corresponding to three different source frequencies. Due to the open end boundary condition and different λ according to frequencies, the location of the electrical null moves along the transmission line length as frequency changes. When the source frequency is lower than the resonant frequency, the electrical null moves toward the source end. On the other hand, the electrical null will move toward the open end if the source frequency is higher than the resonant frequency. By monitoring the difference in voltage magnitudes at two taps ZA and ZB on the patch antenna that are equally spaced away from the center, a monotonic curve passing through zero can be traced out for resonance detection. Fig. 3.6(b) shows three monotonic curves, the solid line is derived from the lossless

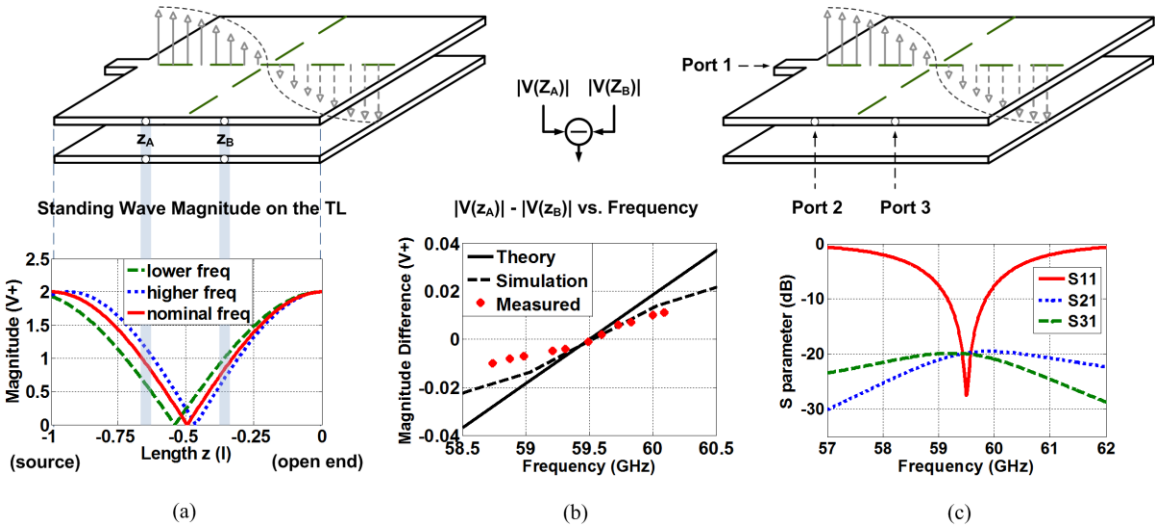


Fig. 3.6. Center frequency detection of the antenna reference: (a) standing wave magnitudes along the length for three frequencies at source, (b) the difference in magnitude of two taps Z_A and Z_B versus frequency, (c) S-parameter analysis of the 3-port antenna reference.

transmission line model, assuming perfect matching over the frequency band. The dashed line is obtained from Ansoft HFSS full-EM simulations of the three port antenna reference setup in Fig. 3.6(c), showing the discrepancy due to the limited bandwidth of the patch antenna. Measured results are shown as dots in Fig. 3.6(b), which follow the same trend as the simulation. Fig. 3.6(c) also shows the S-parameter analysis. S21 and S31 represent the ratio of power delivered onto ZA and ZB from the antenna feed point at Port 1. The two tap nodes are designed to be high impedance nodes, so that they do not load the patch antenna significantly, but provide enough voltage swing for the following envelope detectors to measure the standing wave magnitude. Simulation results show only 2% of the power delivered onto the patch antenna is lost on the two tap nodes. The locations of the two taps are also important. A wider separation between the two taps provides a larger range of the monotonic curve, thus a larger lock-in range of the FLL, as discussed in Chap. 2. However, the matching condition of the patch antenna also needs to

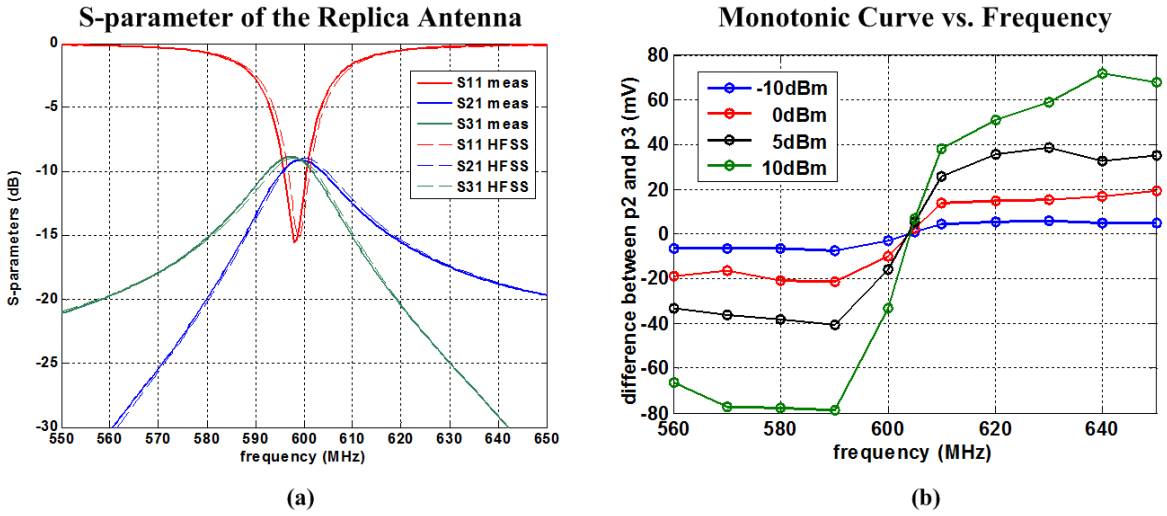


Fig. 3.7. Measured results: (a) S-parameter of the replica antenna, (b) difference in magnitude of Port 2 and Port 3 versus frequency under different input (Port 1) power level.

be concerned, which will change the monotonic range of the magnitude diffrerence plot. Therefore, if the separation is too wide for a target frequency range, the monotonic characteristic no longer applies, which could result in instability in the FLL. Furthermore, the two envelope detectors would be placed far away from each other on the chip, causing mismatch from separation within the single wafer [48], and thus affecting the accuracy of tracking the resonant frequency. In the final layout of the antenna reference, the two taps are equally spaced 110μm (~0.1λ) away from the length center, resulting in a calculated locking range of 8.5GHz. Another factor that will affect the locking range of the antenna reference is the antenna bandwidth. A larger bandwidth implies a wider locking range. In this case, the antenna bandwidth is around 1 GHz, which provides sufficient range for covering process variation of the patch antennas.

3.2.3. Replica Antenna at Low Frequency

In order to characterize the concept of antenna reference, we built a replica prototype at 600MHz ($freq_{target}$/100) before we implemented it on CMOS. The center frequency is chosen because of the precision of our milling equipment. The prototype is realized using Rogers RO4003 substrate. The dimension of the patch antenna reference design is shown in Fig. 3.7. Full EM simulation from Ansoft HFSS shows that the standing wave pattern characteristic also applies to the replica prototype, so that the center frequency detection scheme is still valid. Fig. 3.8(a) shows the measured and simulated S-parameters of the prototype antenna, which has the similar behavior of the 60GHz design. Fig. 3.8(b) shows the difference in magnitude of Port 2 and Port 3 versus frequency under different

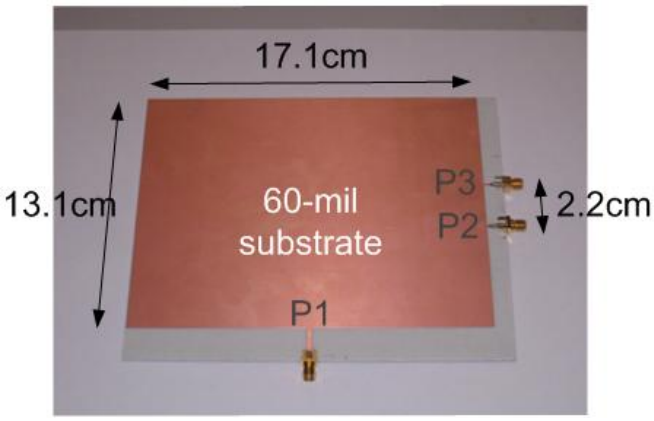


Fig. 3.8. Replica patch antenna prototype at 600MHz.

input (Port 1) power level. The monotonic curves from 590MHz to 620MHz demonstrated the feasibility of center frequency detection, therefore utilizing the patch antenna as a frequency reference.

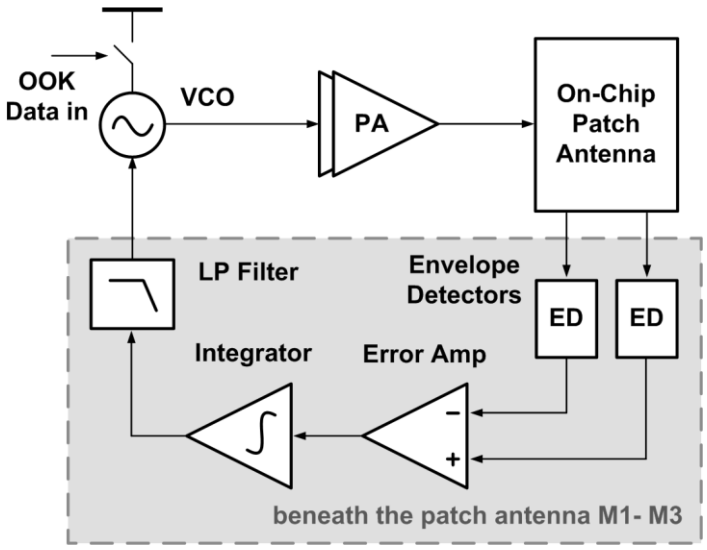
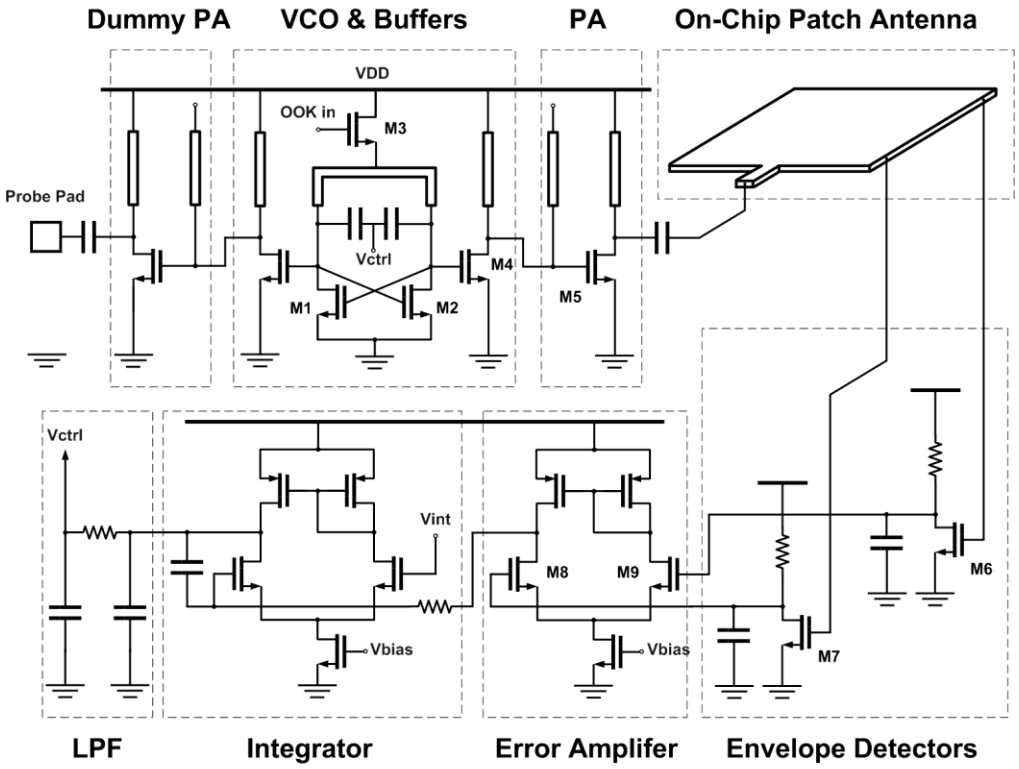


Fig. 3.9. Block diagram of the 60GHz FLL.

3.3. Frequency-Locked Loop Circuit Design

Fig. 3.9 shows the block diagram of the 60 GHz FLL. The FLL mainly consists of two parts; a feed-forward RF part and a feedback baseband part. The RF part comprises a differential VCO, a buffered output of the VCO, a power amplifier (PA), and the on-chip patch antenna reference. The baseband part functions as a PI controller, and has two envelope detectors, an error amplifier, an integrator, and a loop filter. The VCO signal is amplified by the PA, and radiated through the antenna. The frequency of the VCO is regulated by the feedback baseband part. The VCO is designed to be on-off keying (OOK) modulated by power gating with header device, so that the FLL can serve as a simple low-rate OOK transmitter. Note that the baseband circuits highlighted in Fig. 3.9 are placed beneath the patch antenna ground plane using Metal 1 to Metal 3 routing layers. The optimal placement and routing to reduce crosstalk between the RF and baseband components will be discussed in Session 3.4.



M1	M2	M3	M4	M5	M6	M7	M8	M9
12.8 / 0.12	12.8 / 0.12	50.0 / 0.12	6.4 / 0.12	26.0 / 0.12	50.0 / 0.48	50.0 / 0.48	18.0 / 1.00	18.0 / 1.00

Fig. 3.10. Schematic of the 60GHz FLL.

3.3.1. VCO, Buffers, and PA

Fig. 3.10 shows the schematic of the 60GHz FLL. The VCO uses a cross-coupled pair topology with an LC resonator. The resonator is realized by a half-wavelength transmission line at the top metal layer, and the simulated Q-factor of the resonator is 15 at 60GHz. The frequency tuning is achieved by a pair of thin oxide NMOS varactors. One of the differential VCO outputs feeds the signal onto the patch antenna through a common source stage buffer and a PA. The PA is designed for maximum power delivery, using the top metal layer for high-Q transmission lines for matching. Ideally, we want to probe the signal at the antenna input, where the FLL output is. However, the pad and

probing might destroy the matching condition between the PA and the antenna, so the secondary output of the differential VCO is used for testing, and is connected to an RF probe pad through a dummy PA. In this way, we can monitor the FLL output frequency. However, the absolute output power is not available through direct measurement due to an extra 500μm routing that is necessary for the on-chip probing pads setup. The simulated FLL output frequency and power are 60.12GHz and -3.6dBm, respectively. The measured power consumption of the VCO core, buffers, and PA are 8.8mW, 2.6mW, and 16.0mW, respectively.

3.3.2. Envelope Detector

The envelope detectors sense the magnitude of the standing wave on the antenna, and down-convert the signal from 60GHz to DC. An active envelope detector topology is used for larger output voltage levels, which is a class-AB biased amplifier with parallel RC load at the output [49]. The bias of the two envelope detectors is critical, and the connection through the patch antenna ensures the DC voltage at both gates of the envelope detectors are the same. The setup also makes sure the patch antenna is not DC floating when it is operating. Moreover, large devices are used and they are laid out in close proximity to lower the mismatch between the two envelope detectors [48]. The simulated offset voltage of the envelope detector inputs due to process variation is 190μV, corresponding to a frequency offset of roughly 6MHz. By changing the bias gate voltage and the drain current, the input node of the envelope detectors can be designed as high impedance nodes, so that the two taps on the edge of the patch antenna do not significantly affect the standing wave pattern. The measured power consumption of one envelope detector is 670μW.

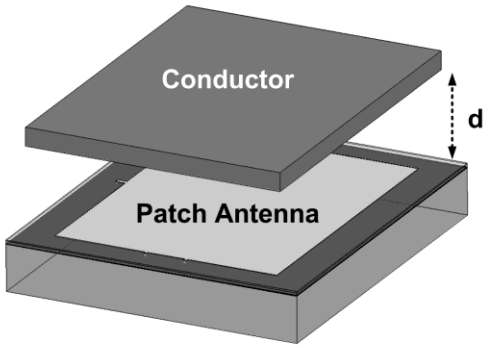


Fig. 3.11. Proximity effect setup of the patch antenna.

3.3.3. Error Amplifier, Integrator, and Loop Filter

The error amplifier provides the difference and controller gain for the FLL. It is an amplifier with a differential input and an active load for single-ended output. 20dB of gain and 300MHz bandwidth is obtained from this stage. The simulated offset voltage at the input of the error amplifier is 52μV, corresponding to a frequency offset of roughly 11MHz. The integrator introduces a pole at DC, minimizing the steady state error between the FLL output and the natural resonant frequency of the patch antenna. Bias conditions of the error amplifier, envelope detectors and the integrator must be considered together for the proper input voltage range and gain margin. The loop filter stabilizes the FLL and is realized by a distributed resistive transmission line with metal comb capacitor units with a self-resonant frequency above 60GHz. The cutoff frequency of the loop filter is designed to be 100MHz.

3.3.4. Proximity Effect on the Patch Antenna

In practical applications, the properties of the antenna will be affected by application-

specific scenarios in which objects are placed near the radiating element. This will affect communication in two ways; 1) similar to any radio, the transmitted signal will be attenuated by the interfering object, and 2) specific to this antenna-referenced FLL, the resonant frequency of the antenna will shift and the FLL will track the shift. In the latter case, the transmission line theory still applies, but the center frequency and the bandwidth will change. Fig. 3.11 shows a simulation setup for characterizing the proximity effect when a conductor appears in close proximity to the antenna. Full-EM simulations show that when a copper patch of the same size of the patch antenna is placed directly in front of the antenna at a distance of 500μm, the center frequency shifts by 67.6MHz (0.1%). This value is equivalent to the 1σ standard deviation on center frequency due to process variation alone, and is not enough to compromise FCC compliance in the 60GHz ISM band. The bandwidth is also impacted by the metal in front of the antenna, and it reduces by 17%. The frequency shifts caused by nearby metal and by process variation are uncorrelated, so the center frequency of a blocked antenna has the same distribution due to process variation as the unblocked one, but with a shifted mean. Therefore, including worst-case 3σ process variation and the effects of interfering metal 500μm away, two patch antennas can still communicate with each other.

Moreover, the case when a strong interfering signal is incident on the antenna should be considered. An interfering signal with random phase could cause constructive or destructive interference to the standing wave pattern on the patch antenna. A patch antenna is a relatively narrow band filter, so the interference which is close to the center frequency is most likely to be picked up by the antenna. Simulation results show that when we introduce an interference tone that is 1% lower in frequency and 50% lower in

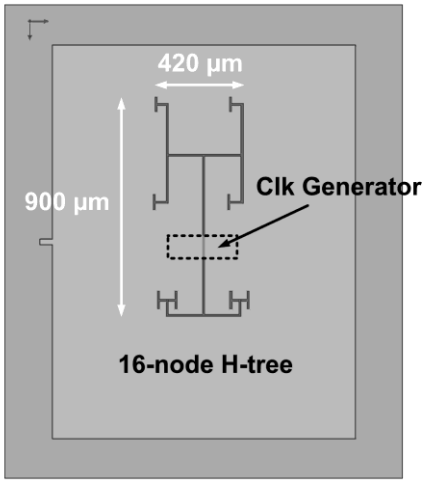


Fig. 3.12. A 16-node clock H-tree beneath the antenna ground plane.

power level than the VCO output but with different phases, the transmitter output shifts -5% away from the nominal value. While this high of power typically would not be seen in a WSN of these nodes, this does place limitations of the proximity of this transmitter to other high-power 60GHz radiators.

3.4. Circuitry beneath the Patch Antenna

Because the patch antenna and the baseband circuits beneath are working simultaneously in the FLL, the crosstalk between them is important, and it is a general issue for system integration as well. Coupling can happen in two directions. A digital signal operating beneath the ground plane could be picked up by the patch antenna, and then radiated, causing the chip to exceed the FCC noise emission mask. On the other hand, the 60GHz RF signal on the patch may couple to the baseband circuits causing malfunction of the feedback loop, digital logic, or memory. We know the patch ground plane helps with shielding. However, a more detailed discussion and experiments on spatial placement and routing are presented in this section.

3.4.1. Coupling from Circuits beneath to the Antenna

The digital clock and full-Vdd logic switching are considered low frequency noise sources to the RF signal on the patch antenna. In order to verify the shielding ability of the antenna ground plane, we fabricated a replica patch antenna over a clock generator with a 16-node clock distribution tree on a separate die, which is shown in Fig. 3.12. The clock generator is a 5-stage ring oscillator with a center frequency around 400MHz. The H-tree is located in the middle of the patch antenna, using Metal 3 as the routing layer. There are repeaters every 100µm along the tree, and it occupies an area of 420µm x 900µm. The experimental result shows that, when a $1.2V_{pp,}$ full-swing, 322MHz clock signal is running on the H-tree, we are able to detect the presence of the clock signal using a RF probe pad connected to a Metal 1 trace that capacitively couples to the clock H-tree. This step is to make sure the clock is running. Then we move the probe a port on the replica patch antenna at Metal 8. With 10kHz resolution bandwidth and a noise floor level of -98.2dBm, we did not observe the 322MHz clock signal or its harmonics on the patch antenna. The -98.2dBm noise floor is far below the -41.3dBm/MHz noise emission mask allowed by the FCC. The experiment shows that the low-frequency noise coupled from the circuit beneath onto the patch antenna is negligible due to the ground plane shielding.

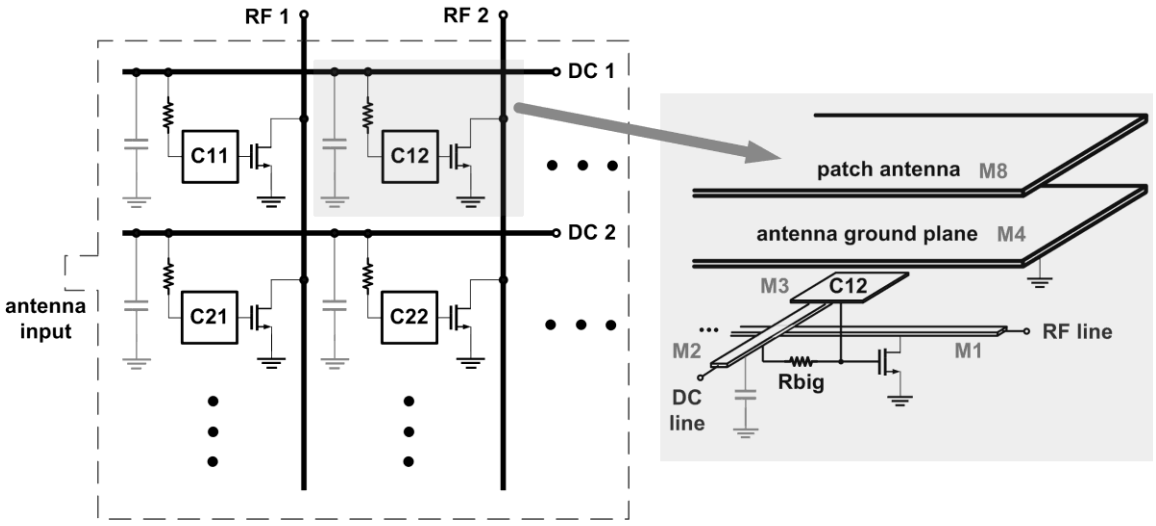


Fig. 3.13. 60GHz coupling sensor array.

3.4.2. Coupling from the Antenna to the Circuit beneath

The circuits beneath the antenna ground plane need good isolation to function correctly. At 60GHz, it is assumed that the electric field distribution on the antenna dominates the coupling between the patch and substrate; in other words, the magnitude of coupling will follow the standing wave pattern along different locations beneath the antenna. In order to verify this, we fabricated a coupling sensor array under the replica patch antenna to measure the coupling magnitude at different locations beneath the antenna. Fig. 3.13 shows a schematic of 4 sensor cells of the coupling sensor array (not drawn to scale). In the test chip, there are 8 by 7 cells, a total number of 56 sensors, spread over half of the antenna-covered area.

Each sensor cell has a 60µm x 60µm sensor pad at Metal 3 (directly below the Metal 4 ground plane) and an amplifying transistor, with the drain of the transistors connect to a RF line at Metal 1 and the gate of the transistors connect to a DC line through a large resistor. The goal of the circuit is to sense the coupling signal individually at each sensor

pad. The pads are drawn at the Metal 3 layer so that the strongest coupling is sensed. The RF line, the most sensitive signal trace, is on the Metal 1 layer, reducing the global coupling directly from the antenna to the RF line. The RF output is connected to Port 2 of an Agilent E8361A vector network analyzer (VNA), while providing a DC bias through a bias tee, and with Port 1 connected to the replica antenna input shown in Fig. 3.13 through on-chip probing. The DC lines are orthogonal to the RF lines for probing purposes, and there are large capacitors connecting from the DC lines to ground to reduce global coupling onto the DC lines and then onto the RF lines. There is also a column of dummy sensors that contains one RF line and 8 DC lines providing different sensor cell gain numbers for calibration. Because we use the same bias voltage for all of the sensor cells, the gain differences mainly come from different load impedances according to the locations where the sensor cells connect their drain terminals to the RF line. We use the dummy sensors to characterize the impact of the different load impedances.

When measuring sensor cell C11 (see Fig. 3.13), we first probe RF line 1 and measure the S21 when the whole array is turned off, and then measure the S21 again when RF line 1 and DC line 1 are providing the bias for cell C11. The latter S21 is denoted as S21' and there is a general relationship

$$S21_{xy} + C_{xy} \times G_y = S21'_{xy} \tag{10}$$

Where $S21_{xy}$ is the S21 when cell C_{xy} is selected but the DC bias is off, and C_{xy} is the coupling signal that corresponds to that sensor cell, which is the desired result. G_y is the gain of the y^{th} sensor cell from the dummy sensor cell column. $S21'_{xy}$ is the S21 when cell C_{xy} is selected and the DC bias of the cell is also on. By (10), we can measure and calibrate out the coupling noise from other locations to obtain the small coupling signal

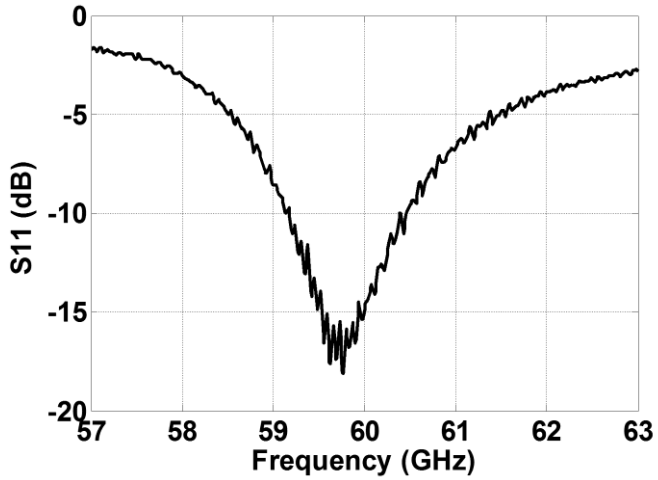


Fig. 3.14. Measured S11 of the replica patch antenna.

C_{xy}. The algorithm relies on the sensitivity of the VNA, because the coupling signal C_{xy} is predicted to be on the order of at least -50dB [45]. Moreover, the gain of the dummy sensor is not high at 60GHz without proper matching. So the magnitude difference of $S21_{xy}$ and $S21'_{xy}$ may be small. The Agilent E8361A network analyzer has a dynamic range of 94dB and a trace noise smaller than 0.006dB from 10MHz to 67GHz [50]. The measurement results are shown in the next section.

3.5. Measurement Results

3.5.1. Antenna Reference

In order to test the antenna resonant frequency and bandwidth, we fabricated a second chip in the same 0.13μm CMOS process that has a replica patch antenna with the same dimensions as the one in the FLL. Twenty of the replica antennas were tested, and Fig. 3.14 shows one of the measured S11 plots of the antenna with a frequency span of 6GHz. The center frequency is around 59.8GHz with a bandwidth of 1.2GHz. Fig. 3.15 shows the distribution on measured resonant frequency and bandwidth over 20 replica patch

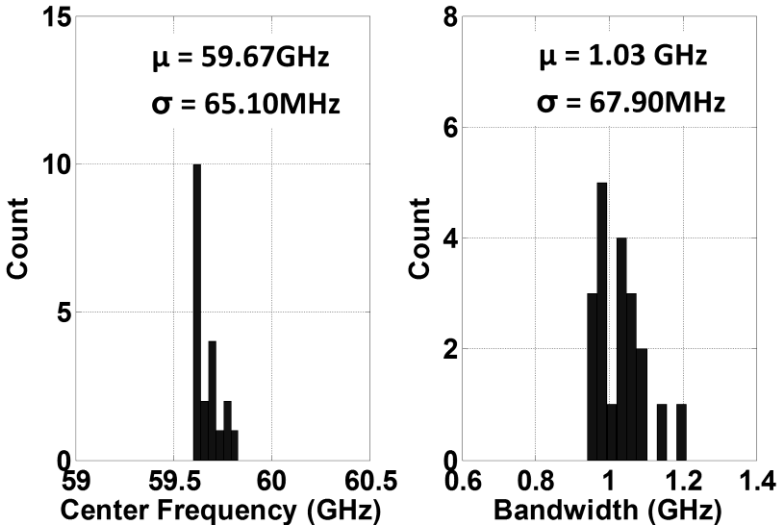


Fig. 3.15. Antenna resonant frequency and bandwidth distribution over 20 replicas.

antennas. The mean and standard deviation of the center frequency is 59.7GHz and 65.1MHz, respectively. The mean and standard deviation of the bandwidth is 1.03GHz and 67.9MHz, respectively. This results in a 3σ variation in center frequency of 3270ppm, ensuring it is FCC compliant in the 60GHz ISM band. In order for the transmitter to reliably communicate with e.g. an energy-detection receiver with an identical patch antenna (not included in this work), process variation should not cause the transmitter frequency to fall outside the bandwidth of the receiving antenna. Assuming a worst-case 3σ variation on all parameters from process variation, the frequency response of two patch antennas would overlap. Based on the measured S11 of 20 dies from a single wafer, no missed alignment between two antennas was observed.

3.5.2. Coupling Sensor Array

Fig. 3.16 shows the surface plot of the attenuation of a 60GHz signal coupled to the area beneath the antenna ground plane measured by the sensor array described in section 2.4.2. The x- and y-axis correspond to the coordinates of the physical locations under the

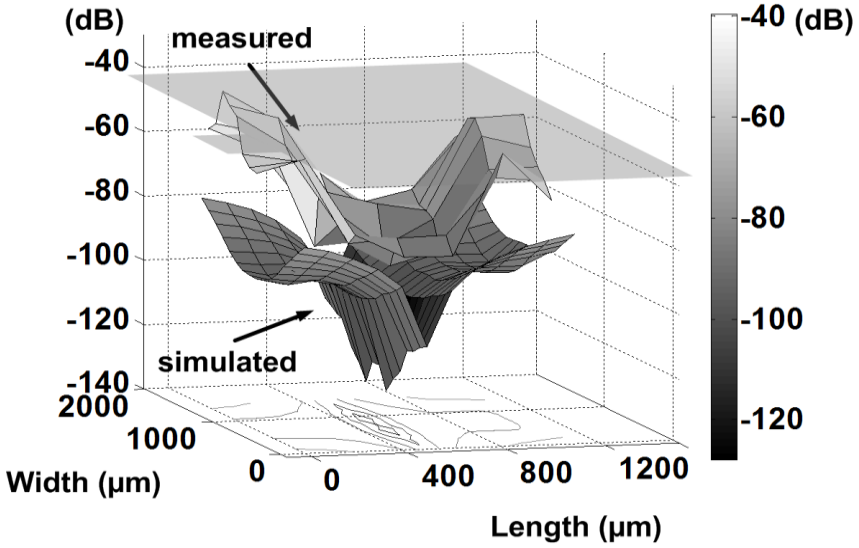


Fig. 3.16. Surface plot and contour of 60 GHz signal coupled from M8 patch antenna to M1 and the white mesh is the mirrored plot from the measured half.

antenna. The measured results from the 56 coupling sensors covers half of the antenna, and we mirror the results and plot them in a white mesh format because of the perfect symmetry for the antenna. Compared with the simulated results, the measurement has a general 20 to 25dB increase in magnitude. This is likely due to the measurement accuracy of a very small coupling ratio. Even with calibration, a small difference on S21 or the gain of the dummy sensor cell measurement will cause large offsets in the coupling calculation from (6). However, the measured result has a similar coupling shape and contour to the simulated result. It not only verifies the impact of the standing wave pattern on the coupling effect, but also provides a guideline for placing and routing the circuits beneath the ground plane for minimum coupling. Fig. 3.17 shows the micrograph of the die used for characterization. It has the replica patch antenna, 60GHz coupling sensor array, clock generator, and the 16-node H-tree. The sensor array occupies an area of 800μm x 1200μm.

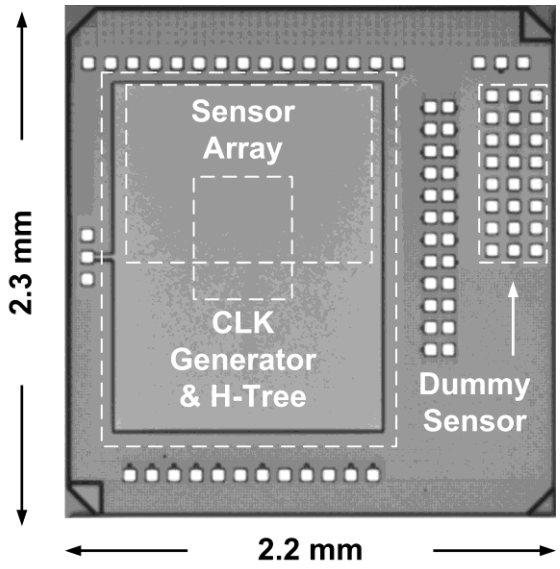


Fig. 3.17. Micrograph of the die for characterization.

3.5.3. Frequency-Locked Loop

The FLL is fabricated in a 0.13μm CMOS process and the power consumption (excluding the dummy PA to test pads) is 29.6mW. Fig. 3.18 illustrates the test setup for characterizing the 60GHz FLL. The output spectrum measured with a 10MHz span while the FLL is locked is shown in Fig. 3.19. The locked frequency is at 59.27GHz, which is within the variation of the replica antenna. There are no reference spurs in the output spectrum, which would typically appear in a frequency synthesizer with a crystal reference multiplied by a PLL [44]. Fifteen FLLs from a single wafer were tested, and

Fig. 3.20 compares the frequency distribution of the free-running VCO when the feedback loop is off, and when operating in locked mode. The mean center frequency is 59.34GHz, with a standard deviation of 195MHz. Compared to the 503MHz standard deviation of the free-running VCO; the FLL provides an improvement in frequency variation, while eliminating the need for an external reference and tracking the peak-efficiency frequency of the integrated antenna. We can compare this antenna reference

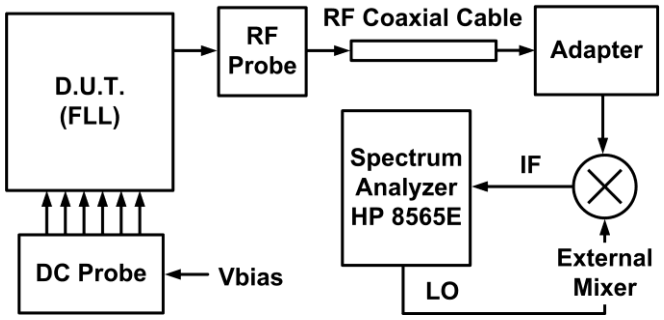


Fig. 3.18. Test setup for the 60GHz FLL.

technique to using an open-loop fixed LC oscillator, which would have benefits of simplicity and lower power consumption than the FLL approach. However, some extent of post-process calibration will be required with the fixed LC oscillator to account for process variation (even though CAD tools can provide accurate predictions of the resonant frequency for both an LC tank and a patch antenna). In the fixed LC oscillator case, calibration of the center frequency requires 60 GHz measurements, which is not cost-effective (e.g. 60GHz divider) and is time consuming (e.g. RF testing). The antenna reference therefore provides a cost-effective method for closed-loop regulation of the transmitting frequency to the peak efficiency point of the antenna.

Fig. 3.21 shows the power breakdown table of the FLL blocks. Furthermore, a pie chart that summarized power breakdown in terms of RF and baseband parts is also shown. Showing the major power consumption (94%) are dissipated in the RF blocks, and the additional baseband circuitry for frequency locking consumes only 6% of the total power. Fig. 3.22 shows the FLL TX signal when the VCO is being OOK modulated at 1kbps. The signal amplitude is small because it is down-converted through a passive harmonic mixer which has an uncalibrated attenuation; therefore, this plot simply verifies the OOK functionality. Fig. 3.23 shows the two envelope detector output signals when the FLL is

OOK modulated and the difference of the two envelope detector outputs as the error signal. The settling time is around 3μs once the loop is turned on; therefore, the VCO can be powered on and FLL locked during every bit transmission for data rates less than 200kbps. The measured results of the FLL are summarized in Table 3.1 and compared with a state-of-the-art PLL, frequency synthesizer and OOK transmitter. While a frequency synthesizer requires a crystal reference, this antenna-referenced FLL performs closed-loop frequency regulation without any off-chip components. A die micrograph of the FLL is shown in Fig. 3.24. The FLL occupies 1.60 x 1.78 mm^2 without pads.

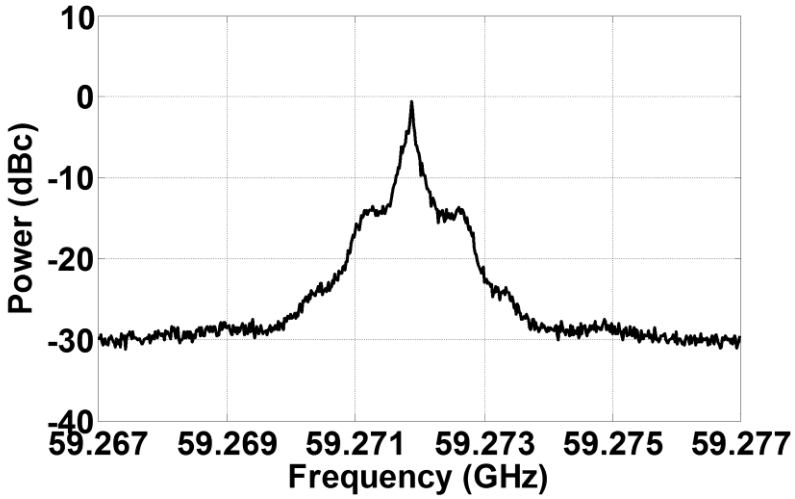


Fig. 3.19. Output spectrum of the FLL in 10MHz span.

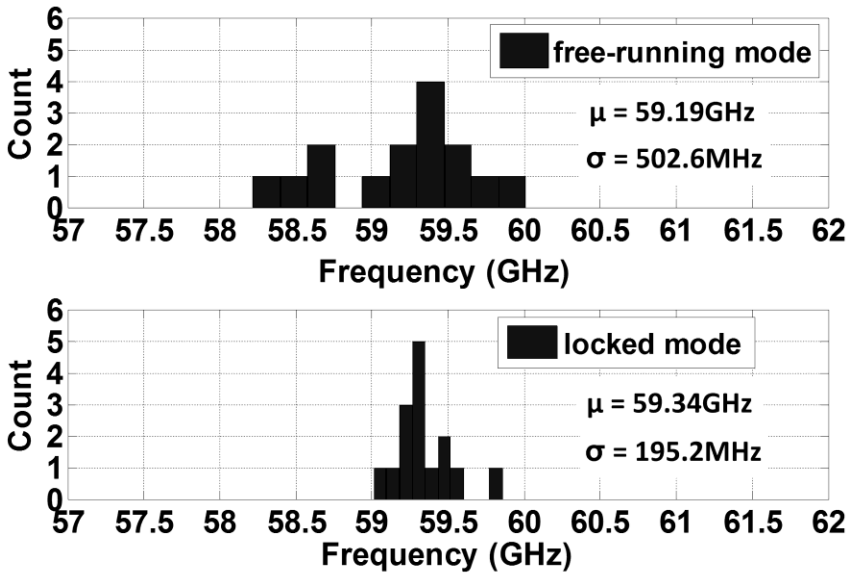


Fig. 3.20. Frequency distribution of the FLL in different modes.

VCO	8.8mW
VCO buffer	1.3mW
PA	16.0mW
ED	0.7mW
Err Amp	0.5mW
Integrator	0.4mW

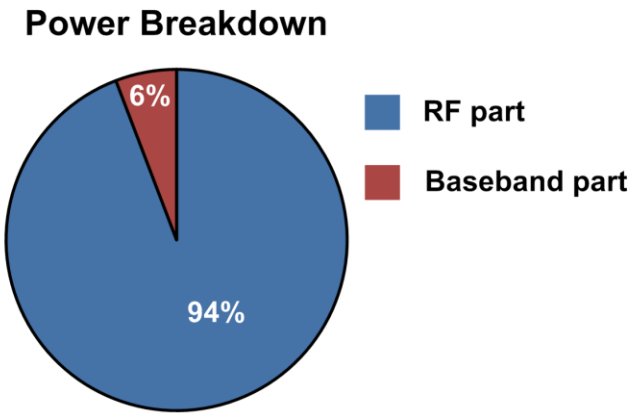


Fig. 3.21. Power breakdown of the FLL.

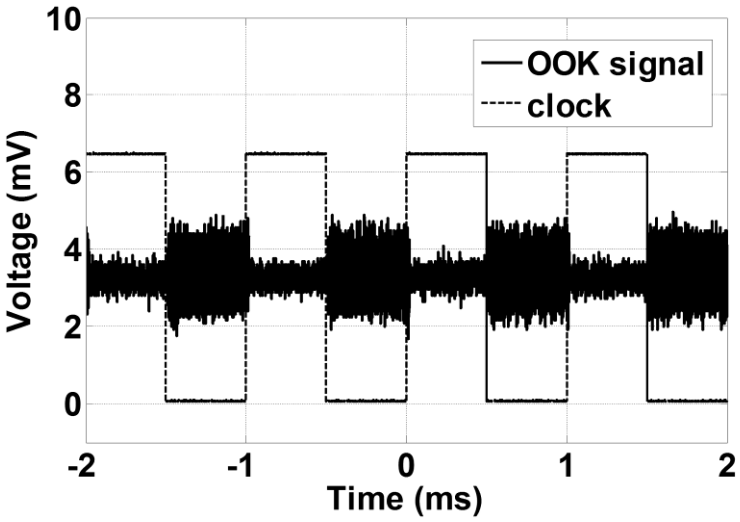


Fig. 3.22. OOK modulating the VCO at 1kbps.

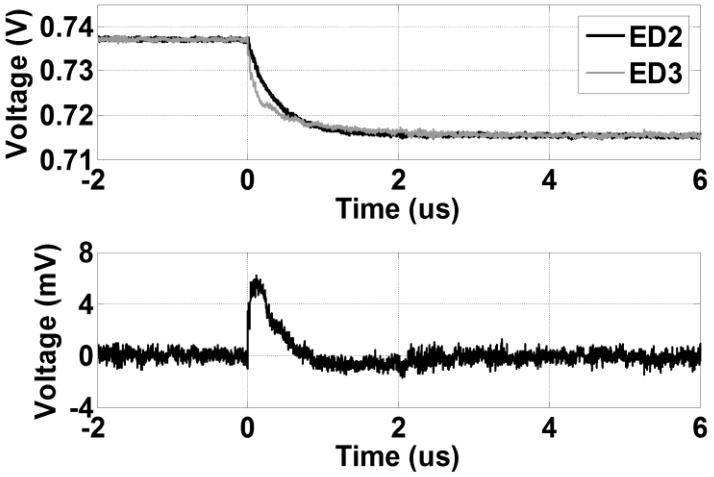


Fig. 3.23. Transient response of the two envelope detector outputs when turning the FLL on and the envelope outputs difference for settling time characterization.

Table 3.1. FLL Performance Summary

	[51]	[52]	[53]	This Work
Type	PLL	Frequency Synthesizer	OOK TX	FLL
Technology	90nm CMOS	90nm CMOS	90nm CMOS	0.13μm CMOS
Power	88.0mW	80.0mW	183.0mW	29.6mW
Frequency	75GHz	60GHz	60GHz	60GHz
Antenna	N/A	N/A	Off-Chip	On-Chip
Area	0.80mm^2	0.95mm^2	0.43mm^2	2.85mm^2
Active Circuit Area	0.80mm^2	0.95mm^2	0.43mm^2	0.64mm^2

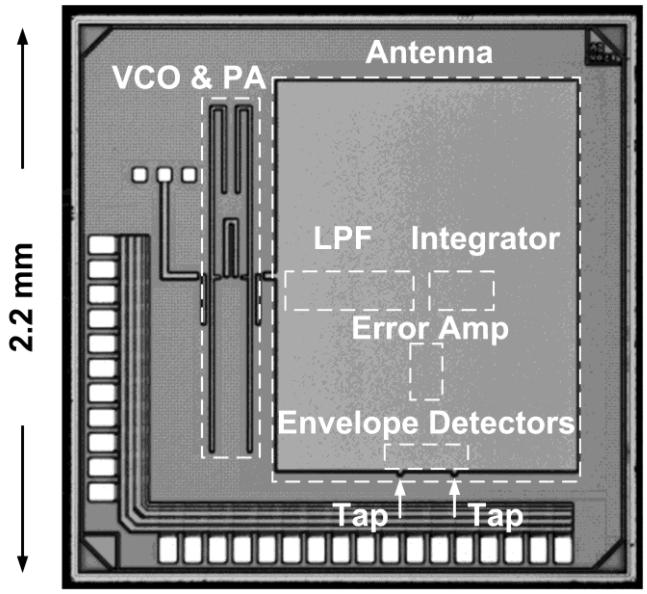


Fig. 3.24. Die micrograph of the 60GHz FLL.

3.6. Conclusion

A FLL in a 0.13μm CMOS process using an on-chip patch antenna as both the radiator and the frequency reference has been demonstrated. The proposed technique efficiently

integrates the antenna, eliminates the need for a crystal reference, is FCC compliant, and ensures the node transmits at the antenna's peak efficiency. The substrate beneath the antenna is shielded by an intermediate metal layer ground plane, freeing up space for active circuits and routing beneath the patch. By integrating circuits in CMOS underneath the patch, and stacking the die on e.g. a thin-film battery, a fully integrated, cost-effective, mm^3-scale WSN node is feasible.

Chapter 4
10GHz IR-UWB Transmitter

This chapter presents an IR-UWB transmitter for heavily duty-cycled mm^3-scale wireless sensor nodes. At these scales, micro-batteries have severely limited capacity and discharge current. Therefore, this transmitter is designed to operate off a local 1.5nF decoupling capacitance during each pulse that is recharged from the battery between pulses. A 30% frequency tuning range ensures RF synchronization between WSN nodes without using crystals. The measured center frequency is 10GHz, while consuming 7.5μW average power at a 10-kHz data rate, and 170pW in sleep mode. The output swing is $700mV_{pp}$ (50Ω).

4.1. Introduction

As discussed in Chapter 1, size reduction towards mm^3-scale WSN nodes leads to severe performance degradation of the battery [13]. At this scale, a micro-battery has limited capacity (1μAh) and small peak current (< 10μA) [13], which presents new challenges on the radio circuits, which typically consume > 100μW when active. Thus, a duty-cycled radio is necessary, along with a large on-chip local decoupling capacitor (decap). However, duty-cycling at the bit-level is required when using only on-chip decap, otherwise a full packet could not be sustained without fully depleting the decap. Recently, impulse-radio ultra-wideband (IR-UWB) transmitters have shown low-power consumption and high efficiency, with fast turn-on/off times [54]-[57]. In this chapter, an IR-UWB TX is proposed targeting mm^3 WSN node operation in a heterogeneous die

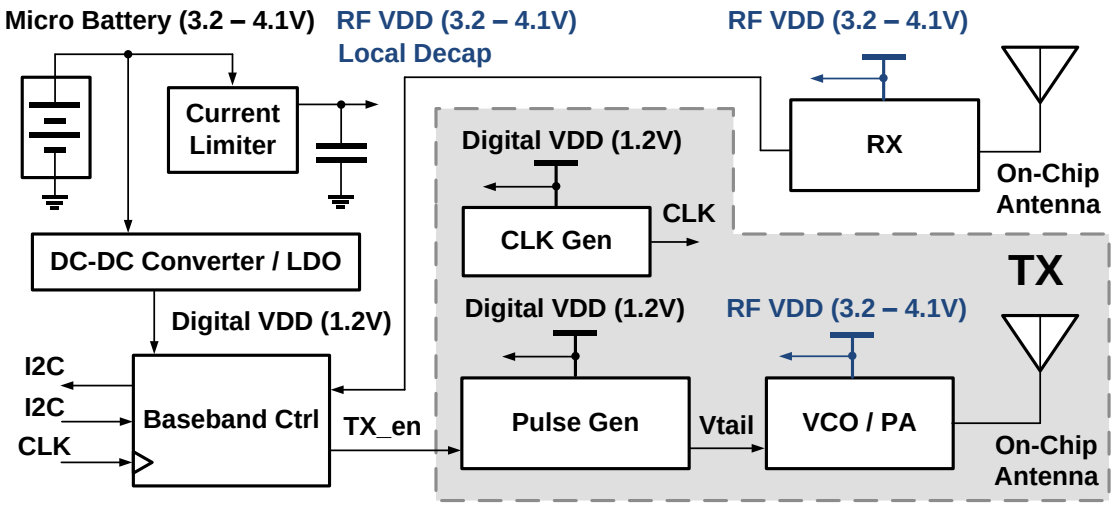


Fig. 4.1. Block diagram of the proposed IR-UWB TX in a typical mm^3 WSN node

stacking platform. It operates over the supply voltage range of a micro-battery, generates tunable pulse durations and center frequencies, and relies on an on-chip local decoupling capacitor only when pulsing. During a pulse, the TX draws maximum on-current to generate the largest signal possible for the longest communication distance. The decap recharges between pulses from the current-limited battery; therefore the maximum pulse repetition frequency (PRF) is set by the battery current limit.

4.2. System Overview

Fig. 4.1 shows the block diagram of the proposed IR-UWB TX in a typical mm^3 WSN node. The TX and RX share one local decoupling capacitor and either transmit or receive at one time. The RF V_{DD} is equal to the voltage of the micro-battery with a current limiter (CL) providing over-current battery protection. Digital baseband controller operates from a 1.2V V_{DD} to reduce power consumption. To survive on the limited resources of the micro-battery, all blocks on the radio have a low-power sleep state. RF and other analog blocks are duty-cycled at the bit-level by the baseband controller, while baseband blocks

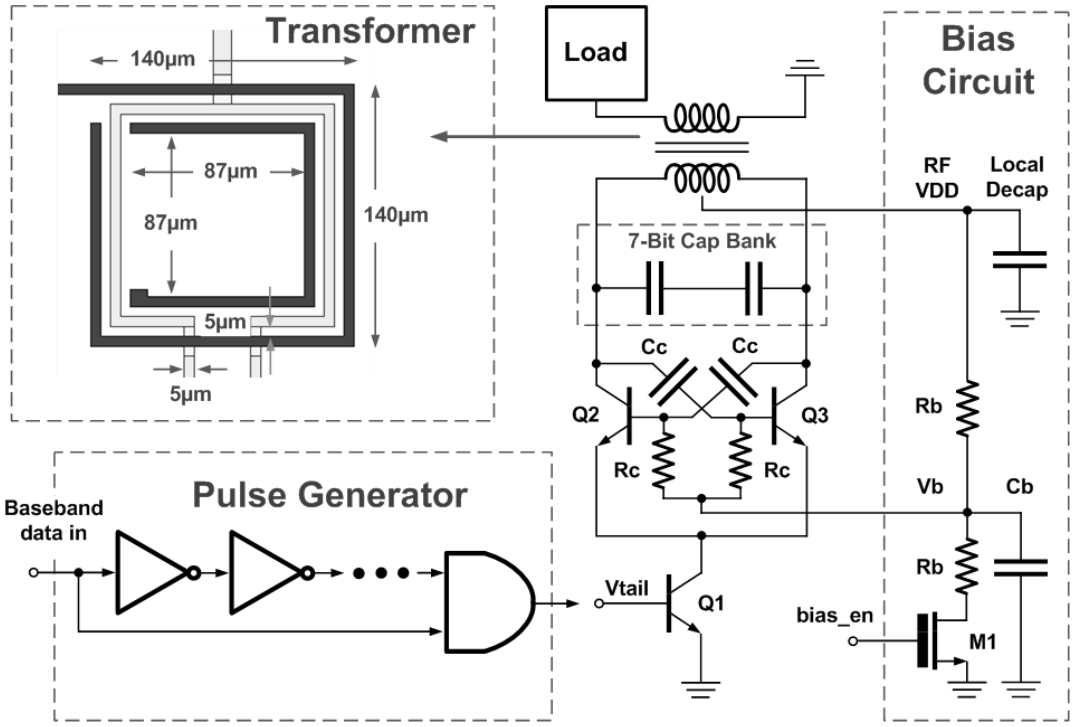


Fig. 4.2. Schematic of the VCO/PA block along with baseband pulse generation in the IR-UWB TX

are duty-cycled at the packet-level by a separate sleep controller. The sleep controller remains on-continuously unless an under-voltage condition occurs. The sleep controller begins and ends the wake-up procedure for each packet via I2C communication, modified to eliminate pull-up resistors. The I2C controller then provides the remaining bidirectional communication with other stacked die in a sensor node. The baseband controller sends a positive edge-triggered TX_en signal to trigger the TX. The baseband pulse generator enables the RF oscillator, and has a 4-bit tuning range of 1.2ns to 6.0ns. The VCO/PA block of the TX is designed to operate at the RF V_{DD} for higher output power during the short period of on-time. An on-chip antenna is preferred for an mm^3 system because of its compact size. Thus, the upper end of the UWB spectrum is chosen

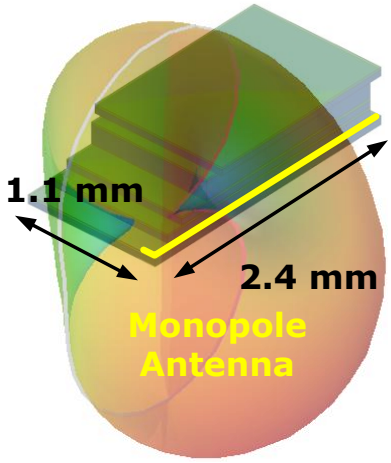
to maximize the antenna gain and minimize the size of an integrated antenna. Nonetheless, we still keep the option of wire-bonding to an off-chip antenna for longer communication distance.

4.3. Circuit Design

The circuits in this IR-UWB TX have two major blocks: VCO/PA, and on-chip antenna.

4.3.1. VCO/PA

Fig. 4.2 shows the schematic of the VCO/PA block in the TX. The LC cross-coupled topology is chosen for fast turn-on time in order to have heavily duty-cycle at bit level, and the transformer coupled scheme boosts the signal swing delivered to the antenna. The area of the internal matching network between the VCO and PA is reduced by direct transformer coupling. The dimensions of the transformer are specified in Fig. 4.2. The inductances and coupling coefficient for the primary and secondary are 270pH, 900pH, and 0.66 respectively, from HFSS simulations. In order for the baseband controller to calibrate the center frequency, a capacitor bank with 3-bits coarse tuning and 4-bits fine tuning is implemented and shown in Fig. 4.2, targeting a ±10% tuning range. The capacitor, C_c, controls the oscillating signal magnitude on the base terminals, and it is designed so that the voltage swing will never exceed the breakdown voltage of Q_1 and Q_2 at RF V_{DD}. The bias circuit sets the base voltage and current of the cross-coupled pair Q_2 and Q_3. While the TX is generating a pulse, the voltages on the local decap and base, V_b, will drop. While the recharge current of the decap is set by the battery, the charging time for V_b is set by R_c and R_b. The tail device Q_1 is chosen to be large, such that it enters the saturation region fast once the V_{tail} signal is high. 60mA of current is drawn from Q_1



	[58]	[59]	This Work
Technology	180nm CMOS	180nm CMOS	180nm BiCMOS
Antenna Type	On-chip monopole	On- chip loop- dipole	On- chip monopole
Frequency	9.0 GHz	5.8 GHz	10.0 GHz
Efficiency	0.6 % (- 22.2 dB)	N/A	1.8 % (- 17.4 dB)
Peak Gain	- 16.8 dBi	- 29.5 dBi	- 26.2 dBi
Area	3.4mm x 1.3mm	3.0mm x 1.5mm	2.4mm x 0.1mm

Fig. 4.3. On-chip monopole antenna in a heterogeneous die-stacking setup with comparison table with other integrated UWB antennas

when the VCO begins oscillating. However, the high on-to-off current ratio of the bipolar transistor (>10^8) is favorable for mm^3 WSN nodes so that leakage power is minimized when the TX enters the sleep mode.

4.3.2. On-Chip Monopole Antenna

In order to accomplish a fully-integrated WSN node, the radio die is stacked with other chips like processor, battery, and image sensors. Fig. 4.3 shows the on-chip monopole antenna in a heterogeneous stacked-die simulation setup. A comparison table with other integrated UWB antenna is also shown in Fig. 4.3. With the limited mm^3 size budget, the antenna operates in short monopole region (< $\lambda/2$), delivers a peak gain of -26.2dB at 10GHz with the dies above the radio. The center frequency of the IR-UWB TX is a tradeoff between antenna gain and circuit power consumption.

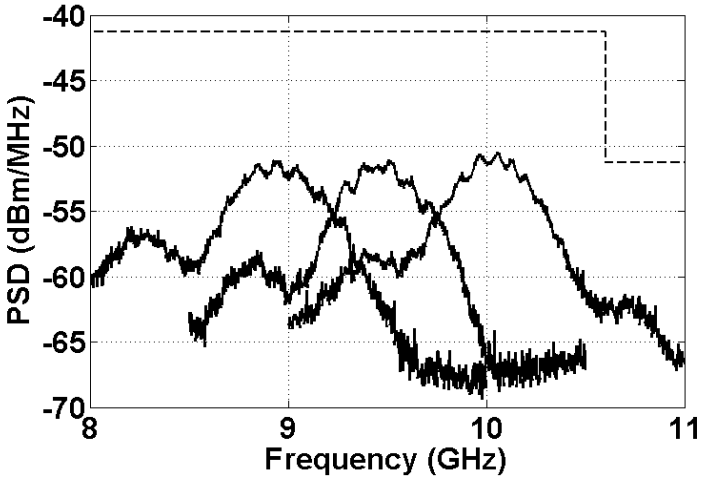


Fig. 4.4. Measured power spectral density of the tunable TX output

4.4. Measurement Results

The proposed UWB TX is fabricated in a standard 180nm BiCMOS technology. Fig. 4.4 shows the measured power spectral density of the tunable TX output with an overlaid FCC emission mask. The nominal center frequency and bandwidth are 10GHz and 900MHz, and the TX consumes 7.46μW of power at a 10kHz PRF. The TX operates over a voltage range of 3.2V-4.2V. Fig. 4.5 shows the output pulse, Vtail, Tx_en and RF VDD in the time domain. The magnitude of the UWB pulse is 700mVpp when delivered to a 50Ω load. However, the TX is designed for an on-chip antenna with higher impedance, and therefore higher voltage on-chip. The turn-on/off times are 800ps and 2ns, respectively.

Fig. 4.6 is a transient plot of RF VDD between pulses, the RF VDD drops by 0.2V during every pulse but recharges from the micro-battery before the next pulse arrives, showing that the TX can fully operate on the on-chip local decap. The peak output power is 0.9 dBm at a 10kHz PRF. Fig. 4.7 shows the center frequencies of TX output with

corresponded digital tuning codes. The tuning mechanism plus UWB signaling ensure RF synchronization over PVT variations without crystals. The measured leakage power of the TX is 170pW, and a die photo is shown in Fig. 4.8 with an active area of 0.11mm^2. All the measured performance of the proposed TX is summarized and compared with other state-of-the art UWB TXs in Table 4.1. The proposed IR-UWB TX, surviving on the local decoupling capacitor, offers a high output power solution for cubic-mm WSN node systems limited by micro-batteries.

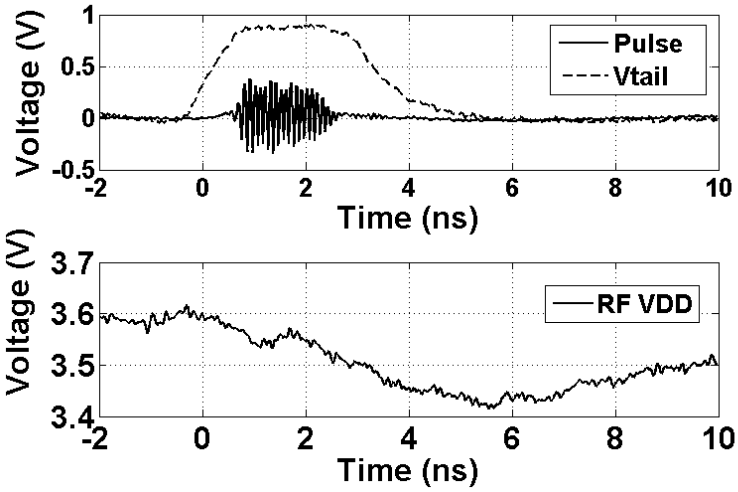


Fig. 4.5. Transient response of the TX output and RF VDD during pulsing.

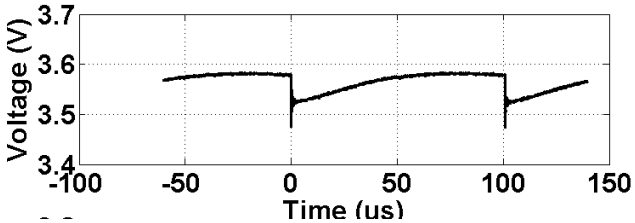


Fig. 4.6. Transient response of RF VDD between pulses.

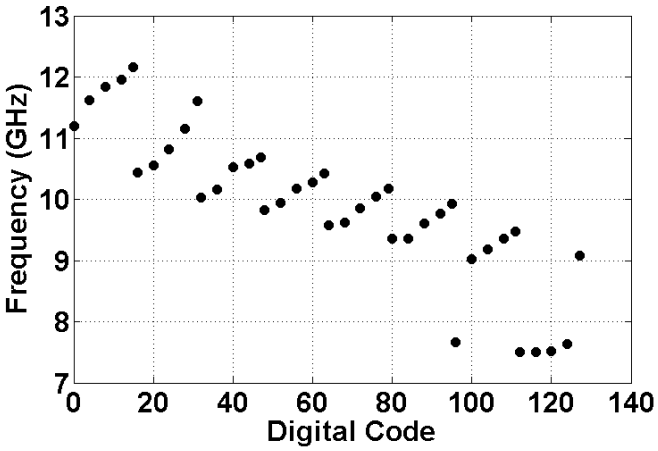


Fig. 4.7. Center frequencies of TX output versus digital tuning codes.

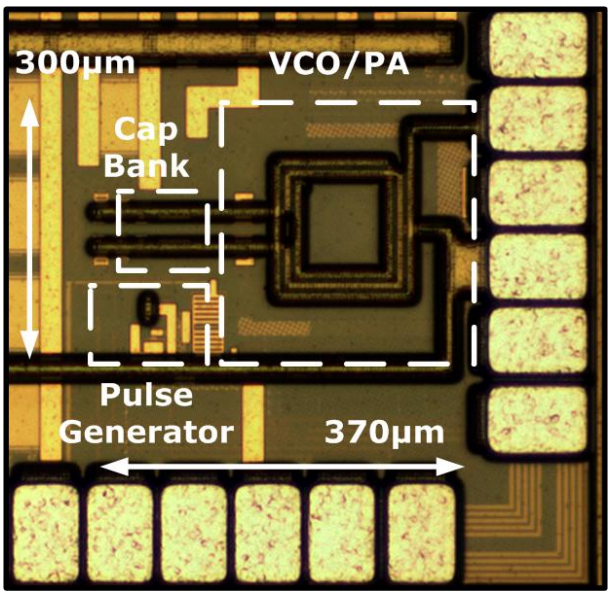


Fig. 4.8. Die photo of the IR-UWB TX.

Table 4.1. Measured IR-UWB TX Performance and Comparison.

	[54]	**[55]**	**[56]**	**[57]**	**This Work**
Technology	90nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm BiCMOS
Center Frequency(GHz)	10	6.85	8	3.4 – 4.4	9-12
Modulation	BPSK	BPSK	N/A	PPM	PPM
Supply (V)	1	N/A	2.1	N/A	3.2-4.2
Avg. Power (μW)	1400	N/A	1380	2000	7.46@3.6V
Output Power (dBm)	-10	N/A	N/A	-10	0.9
Leakage Power (pW)	N/A	N/A	N/A	N/A	170
Output Swing (mVpp)	N/A	506	673	200	700
PRF (Hz)	1M	100M	50M	40M	10k
Pulse Width (s)	N/A	394p	500p	1.1n – 4.5n	1.2n – 6.0n
Energy/Pulse (pJ/pulse)	40	70.8	27.6	50	746
Area (mm^2)	0.066	0.250	0.110	0.030	0.111

4.5. Conclusion

A 10GHz IR-UWB TX in an 180nm BiCMOS process with an on-chip monopole antenna has been demonstrated. It operates over the supply voltage range of a micro battery, generate tunable pulse durations and center frequencies, and lives on an on-chip local decoupling capacitor (decap) only. When the TX is active, it draws maximum on-current to generate the largest signal possible for the longest communication distance. The TX is designed for heavily duty-cycled operations, showing promising results for the integration of a complete mm^3 WSN node system.

Chapter 5
1.2MHz Temperature-Compensated Relaxation Oscillator

This chapter presents a low-power, temperature-compensated relaxation oscillator in 130nm CMOS for mm^3 WSN node on-chip clock generation, therefore baseband data synchronization. An RC network is proposed for the oscillator which introduces a zero in the transfer function, creating an additional degree-of-freedom in the step response used for frequency temperature compensation. This approach uses conventional CMOS resistor and capacitor options and is fully integrated. The oscillator has a measured nominal frequency of 1.24MHz with 1.0% variation from -20°C to 60°C. It occupies an area of $0.02mm^2$, and consumes 5.8μW of active power with a leakage power of 440pW.

5.1. Introduction

Wireless sensor networks (WSN) today are comprised of cm-scale devices that, at a basic level, include a battery, sensor, processor, memory, radio, and some form of timing reference – typically a crystal oscillator. The scaling trend of WSNs suggests mm^3 sensors nodes are on a near-term horizon, and nodes of this form-factor have been recently demonstrated [60]. These vanishingly small devices will enable ubiquitous sensing platforms for environmental, biomedical, military and industrial applications [60], [13], and [31]-[33]. To achieve this, the nodes must be designed for long-term unobtrusive deployment over large temperature variations.

Power consumption, size and frequency stability of the timing reference for wireless communication are major concerns in a cubic-mm WSN node. At the mm-scale, micro-

batteries have limited capacity (1μAh) and peak discharge current (< 10μA) [13]. This leads to severe challenges on the cubic-mm WSN circuit design. While crystal-based oscillators are typically used as a timing reference due to their immunity to PVT variation, the size of off-chip crystals is an obstacle for cubic mm-scale system integration, and frequency robustness of crystals comes at the expense of power [61]. As an alternative, monolithic crystal-less oscillators recently have been reported for WSN applications [61]-[62]. With low power consumption and small silicon area, these fully-integrated frequency references maintain temperature compensation over a wide range, without relying on a bulky off-chip crystal.

A low-power CMOS relaxation oscillator is presented with a modified RC network and a single-ended hysteresis comparator. The RC network proposed in this paper adds one additional zero in the transfer function of a conventional relaxation oscillator. This additional degree of freedom allows for temperature compensation of the step response, with a demonstrated variation of 1%. This accuracy is specifically targeting wireless communication using non-coherent energy detection radios, which are common for WSN node systems, and this accuracy is sufficient for a receiver to track during demodulation. The oscillator design is primarily focused on reducing the power consumption and the area while providing sufficient accuracy, both of which are factors in mm^3 WSN nodes.

5.2. RC Network of the Oscillator

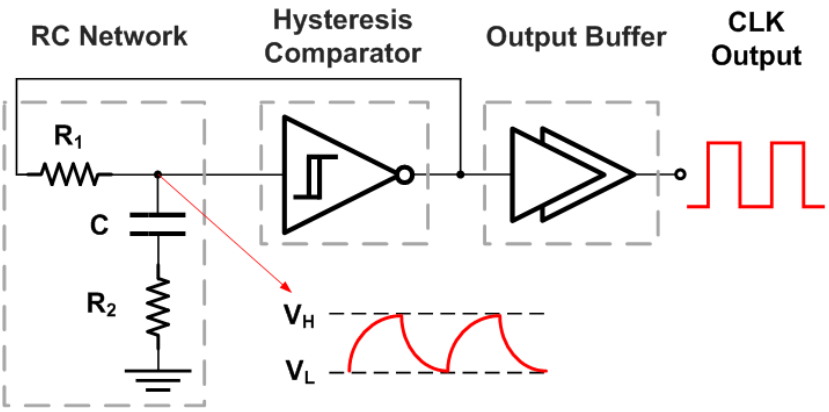


Fig. 5.1. Block diagram of the proposed temperature-compensated relaxation oscillator.

Fig. 5.1 shows the block diagram of the proposed oscillator. Like conventional relaxation oscillators, this one employs an inverting hysteresis comparator with switching thresholds of V_H and V_L, which define the charging and discharging levels of the RC network. When the output of the hysteresis comparator is high, capacitor C of the RC network is being charged until the voltage becomes larger than V_H. Then the output of the comparator flips to the low state and discharges C until the voltage reaches V_L. Oscillation is achieved through back and forth charging and discharging processes, and the frequency is determined by the resistance and the capacitance of the RC network. Fig. 5.2(a) shows the step response of the conventional RC network which consists of R_1 and C only. The transfer function is

$$T_{convention}(s) = \frac{1}{1+s(R_1C)} \tag{11}$$

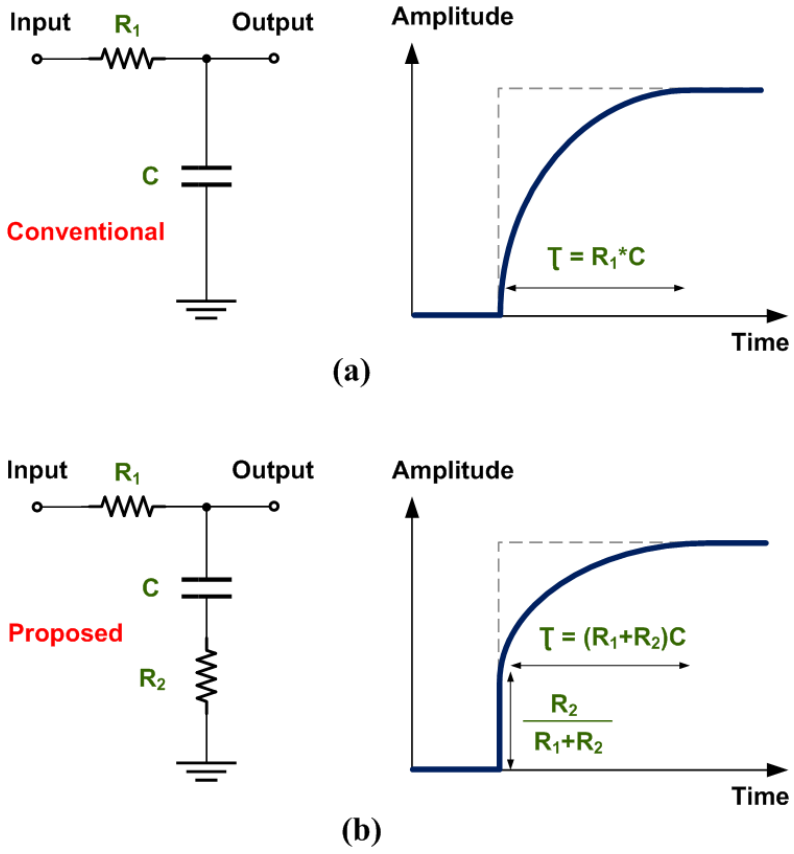


Fig. 5.2. Step response of the (a) conventional RC network and (b) the proposed RC network.

The time constant τ (R_1C) and therefore the frequency vary depending on the temperature coefficients of the resistor and the capacitor. The network proposed in this paper adds an additional resistor, R_2, as shown in Fig. 5.2(b), and the transfer function becomes

$$T_{proposed}(s) = \frac{1+sR_2C}{1+s(R_1+R_2)C} \tag{12}$$

introducing a zero in the transfer function. By the initial-value theorem of a Laplace transform [63], the step response when t = 0 is

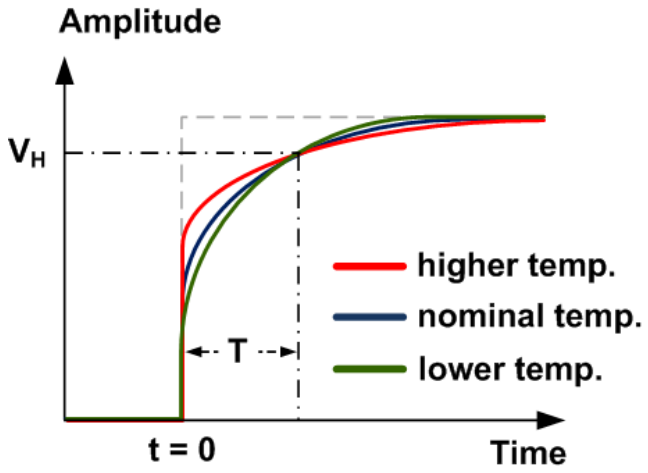


Fig. 5.3. Step response of the RC network at different temperatures.

$$\lim_{t\to 0} f(t) = \lim_{s\to\infty} s \cdot T_{proposed}(s) \cdot \frac{1}{s} = \frac{R_2}{(R_1 + R_2)} \tag{13}$$

In other words, the step response of the proposed RC network has two segments, the step at t = 0 followed by the exponential transient, before the voltage reaches steady-state. Assuming the magnitude of input step is one, the magnitude of the output step is $R_2/(R_1+R_2)$ at t = 0, and the time constant of the exponential transient is $(R_1+R_2)C$.

In CMOS technologies, resistors and capacitors typically have monotonic temperature coefficients with the same polarity. The temperature coefficient of capacitors (MIM and metal comb capacitors), however, is often small compared to resistors. With the proposed RC network, the two segments in the step response have different temperature dependencies if different resistor types are used for R_1 and R_2. As a result, the temperature dependence of the relaxation oscillator can be decreased by selecting resistors with different temperature coefficients so that the two step response segments are offsetting. Specifically, R_1 is chosen to have a smaller temperature coefficient and R_2

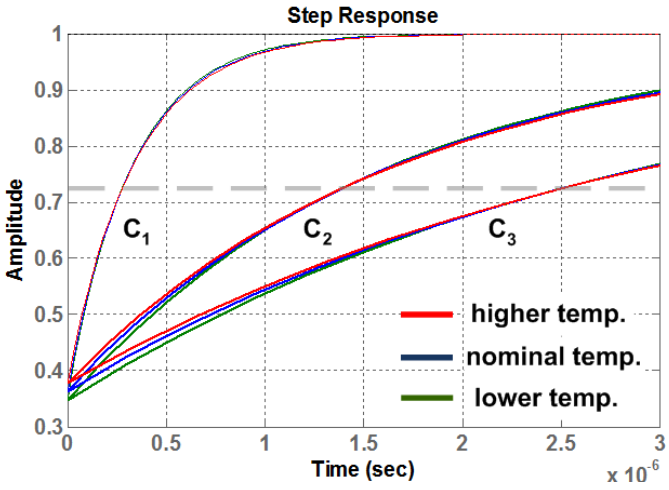


Fig. 5.4. Step response of the RC network with three capacitances at three temperatures.

to have a larger temperature coefficient. Fig. 5.3 shows the step response of the proposed RC network at different temperatures. As temperature increases, the initial step at t = 0 increases, but the time constant of the exponential decay also increases, offsetting the step increase and resulting in a constant time, T, to trigger the switching threshold V_H. The same trend applies as temperature decreases; the initial step decreases while the time constant also decreases, so that the overall period remains unchanged. Thus, by tuning the combination of R_1, R_2, C, V_H and V_L, the period of the proposed RC network will remain constant over a wide temperature range.

According to the step response analysis, we can change C for frequency tuning without losing the temperature-compensated character because C only appears in the exponential transient segment of the step response and will not change the offset over temperature. Fig. 5.4 shows the step responses for three C values C_1, C_2, and C_3 at different temperatures. The time constant of the exponential segment changes, thus the oscillation frequency changes. However, the switching threshold at which temperature

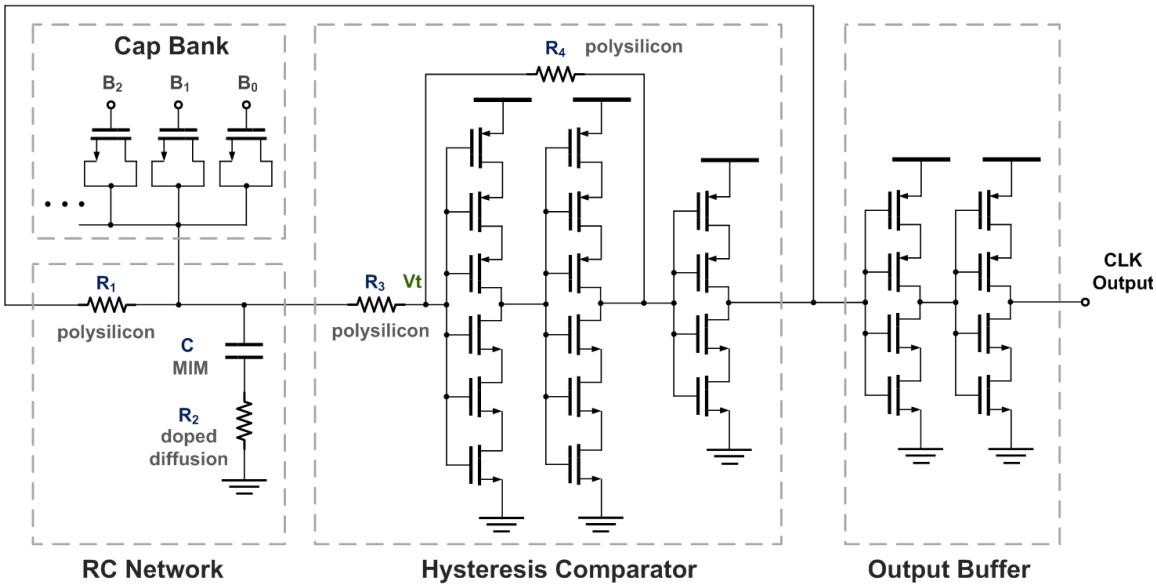


Fig. 5.5. Schematic of the proposed oscillator.

variation is compensated is always the same, maintaining compensation with the ability to tune frequency.

5.3. Oscillator Circuit Design

The schematic of the proposed oscillator is shown in Fig. 5.5. R_1 is a P+ polysilicon 24KΩ resistor while R_2 is an N+ doped diffusion resistor of 28KΩ, and C is a MIM capacitor. The modeled temperature coefficients are 77ppm/°C, 1810ppm/°C and 15ppm/°C, respectively. A 5-bit capacitor bank is added to the oscillator for one-time process calibration of frequency. Note that the capacitor bank will not severely load the RC network since its capacitance is small relative to C, so the temperature compensation scheme still dominates within the frequency tuning range. The single-ended hysteresis comparator is realized with three stacked inverters and two resistors. The stacked transistors help minimize the leakage power while the oscillator is in sleep mode, which is important for mm^3 WSN node applications [60]. The first two stacked inverters with R_3

and R_4 serve as a high gain amplifier with resistive feedback, providing a sharp transition for the step response and the proper value of V_H and V_L. Assume the output of the hysteresis comparator is at ground and the input of the last inverter is V_{DD}, then the voltage *Vt* between R_3 and R_4 can be described in terms of comparator input *Vin* as

$$Vt = Vin + (\frac{R_3}{R_3 + R_4})(V_{DD} - Vin) \tag{14}$$

When *Vt* equals to $V_{DD}/2$, which is the switching threshold of the stacked inverters, we can solve for the V_L

$$Vin = V_L = (\frac{R_4 - R_3}{2R_4})V_{DD} \tag{15}$$

Similarly, when the comparator output is V_{DD}, *Vt* then becomes

$$Vt = (\frac{R_4}{R_3 + R_4})Vin \tag{16}$$

And V_H can be solved by applying *Vt* equals $V_{DD}/2$

$$Vin = V_H = (\frac{R_4 + R_3}{2R_4})V_{DD} \tag{17}$$

In this design, R_4 is twice the value of R_3, so that V_H is around $3/4V_{DD}$ and V_L is around $1/4V_{DD}$ no matter the supply voltage. This gives the oscillator immunity to V_{DD} variation. The last inverter flips the polarity for charging and discharging the RC network to create the oscillation. The single-ended oscillator topology tends to be more vulnerable to supply variation and temperature, mostly from V_L and V_H tripping at the hysteresis comparator. The simulated results show 3.5% and 0.5% on V_L and V_H tripping at 10% supply variation, with -0.9% and 0.7% variation for V_L and V_H at 60°C and -20°C, respectively. However, the single-ended topology significantly reduces the power

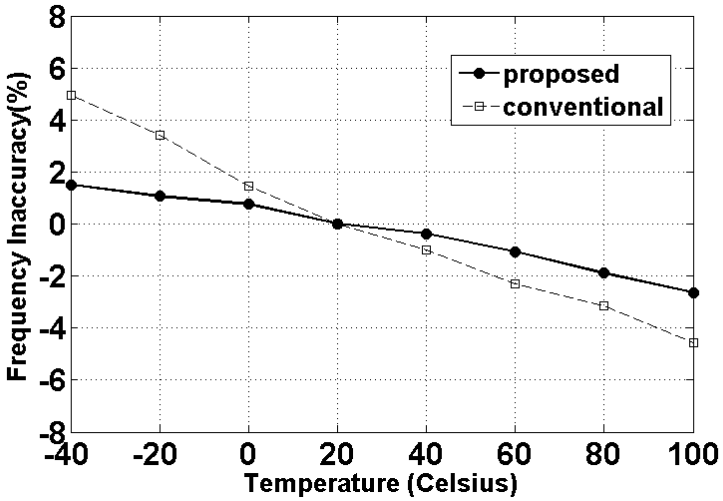


Fig. 5.7. Measured oscillation frequency inaccuracies over temperature.

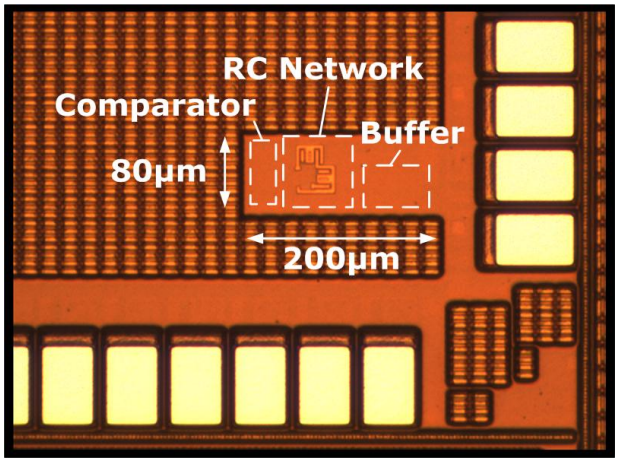


Fig. 5.6. Die photo of the proposed oscillator.

consumption from differential hysteresis comparators. Finally, the output buffer drives the clock output.

5.4. Measurement Results

The proposed oscillator is fabricated in a standard 130nm CMOS technology. The nominal clock frequency is 1.24MHz while consuming only 5.8μW of power from a 1V supply voltage. The frequency variation is 1.8% with a 1% change in supply voltage. The

Table 5.1. Performance Summary and Comparison

	[61]	[62]	[64]	[65]	This Work
Technology	130nm CMOS	65nm CMOS	65nm CMOS	90nm CMOS	130nm CMOS
Frequency (MHz)	3.2	0.15	6	100KHz	1.2
Power (μW)	38.0	51.0	66.0	0.28	5.8
Area (mm^2)	0.073	0.200	0.030	0.12	0.016
Freq. Variation (%) with Temp.	±0.25 @ 20 to 60°C	±0.5 @ -55 to 125°C	±0.43 @ 0 to 100°C	±0.68 @ -40 to 125°C	±1.8 @ -40 to 80°C
Temp. Coefficient	125 ppm/°C	-18 ppm/°C	86 ppm/°C	82 ppm/°C	-296 ppm/°C
Supply Sensitivity (%)	±0.4 @ 1.4 to 1.6V	1.2/V	N/A	±0.82 @ 0.725 to 0.9V	±1.8 @ 1.01 to 0.99V
RMS Jitter	1456 ppm	N/A	N/A	N/A	2781 ppm
Freq. Tuning Range (%)	±40	N/A	N/A	N/A	±12
Leakage Power (pW)	N/A	N/A	N/A	N/A	440

RMS jitter is 2781ppm at 20°C, and the leakage power is 440pW when the oscillator is in sleep mode. Fig. 5.7 compares the frequency stability of the proposed oscillator with an oscillator using the conventional RC network over the temperature range of -40°C to 100°C, showing roughly twice inaccuracy improvements. Over a range of -20°C to 60°C, the oscillator has only 1% variation in frequency, corresponding to a temperature coefficient of -296 ppm/°C. Before the relaxation oscillators are being deployed for cubic-mm WSN applications, they need a one-time frequency calibration over process variation so that they are aligned. With the 5-bit capacitor bank, the frequency tuning range is ±12% or 1.06MHz to 1.32MHz, which is enough for the calibration over process variation. Note that the temperature compensation still applies over the frequency tuning range. The die photo is shown in Fig. 5.6. The relaxation oscillator occupies an area of 80μm x 200μm without pads. The measured performance of the proposed relaxation oscillator is summarized and compared with other state-of-the art oscillators in Table 5.1.

5.5. Conclusion

A low-power, temperature-compensated relaxation oscillator for mm^3 WSN applications is designed and fabricated in a standard 130nm CMOS process. An RC network of the oscillator is proposed with a transmission zero for temperature compensation. It introduces an additional degree-of-freedom for relaxation oscillator design and maintains temperature compensation over a frequency tuning range using conventional CMOS resistor and capacitor options. The oscillator offers a good balance between power, area, oscillation frequency, frequency stability and leakage power, which are all critical specifications for cubic-mm WSN applications.

Chapter 6
60GHz T/R Switch-Less Antenna Front-End

With the knowledge from the preliminary research, this chapter further proposes a 60GHz transmit/receive (T/R) switch-less antenna front-end for the realization of mm^3 WSN nodes. T/R switches are not trivial to implement in the mm-wave range of frequencies. In order to achieve decent T/R isolation (>32dB) at high frequency, resonant circuitry are commonly used [66]-[70], thus increase the area of the system. In this chapter we describe a technique for providing T/R isolation by arranging T/R ports on orthogonal sides of a patch antenna. The proposed technique eliminates the on-chip high frequency T/R switch with decent isolation, loss, and linearity. As a result, the volume of the WSN radio system can be minimized toward mm^3-scale.

6.1. Introduction

Following the continual trend toward smaller and more pervasive computing devices [1], radios are required to be more compact, including antennas, which are usually implemented off-chip for the radio front-end [45]. Integrated antennas have a size advantage over external packaged antennas. However, reducing antenna size results in reduced performance in general [46]. Antennas can be integrated directly on-chip, or at the PCB level. At mm-scale, the operating frequencies need to be pushed up to 10GHz at least [14]. The parasitic loading of the package eliminates the possibility of using external antenna. On-chip antennas seem to be the candidate to meet the mm^3 volume requirement.

Recently, several highly-integrated CMOS radio systems with on-chip antennas operating at the mm-wave range have been reported [14], [71]-[73], showing promising

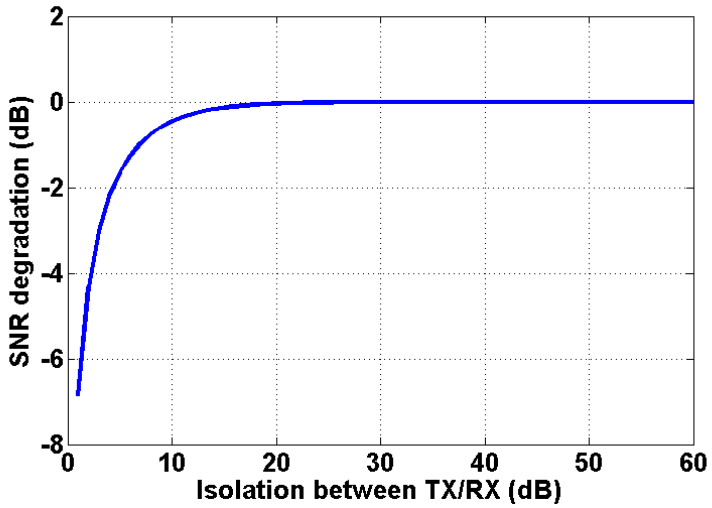


Fig. 6.1. SNR degradation versus isolation between TX/RX.

opportunities for complete SoC integration at a vanishingly small scale. A patch antenna topology with a shielding ground plane shows better performance over other topologies like the monopole, dipole or loop [45]. However, it requires a mm-wave T/R switch [66]-[70], typically required when only one antenna is shared for TX and RX. In general, the isolation between TX and RX is an important metric for the T/R switch in a radio system. In reality, T/R isolation needs to be large enough for RX to be shielded from large TX swing. Furthermore, it has to be large enough to minimize the power lost from the receiving signal leaked into the TX path, so as to maximize the signal-to-noise ratio (SNR) at the RX input. Fig. 6.1 shows the SNR degradation versus isolation between TX/RX. Practically, more than 20dB of isolation is desirable due to the fact that the SNR degradation is less than 0.1dB (98% of nominal power). At mm-waves, decent TX/RX switch performance of isolation, insertion loss, return loss and linearity are approached by matching and resonant components, which occupy significant silicon area [68]-[70].

Table 6.1. Comparison of CMOS On-Chip Antenna Topologies

Type	Area	Gain	Efficiency	Directivity
Dipole	Δ	Δ	Δ	X
Monopole	O	X	X	X
Loop	X	Δ	Δ	X
Patch	X	O	O	Δ

In this chapter, a 60GHz T/R switch-less antenna front-end using an on-chip patch antenna is presented, which has an in-band isolation (>30dB) inherited from the standing wave pattern on the patch antenna at resonance [14]. The TX port and RX port of a square patch antenna either transmit or receive data at any given time from two orthogonal feeds. This location arrangement puts the RX port on the electrical null of the standing wave pattern when transmitting, and vice versa. As a result, the T/R isolation is embedded and the loading effect of TX and RX can be minimized at the operation frequency. The antenna front-end doesn't require spare area for a T/R switch since it is a co-design with the antenna; therefore, no additional insertion loss is incurred. Moreover, the linearity of the front-end system is better than the ones with FETs-based switches [68]-[70] because it is purely passive, so that it can handle large power at the TX output without nonlinear distortion, showing promising results for the realization of mm^3-scale radio system.

6.2. T/R Switch-Less Antenna Front-End

6.2.1. CMOS On-Chip Antennas at 60GHz

In a standard CMOS process, the resistivity of the silicon substrate is approximately 10Ω-cm, and the dielectric constant is around 11 [45]. On-chip antennas suffer from the

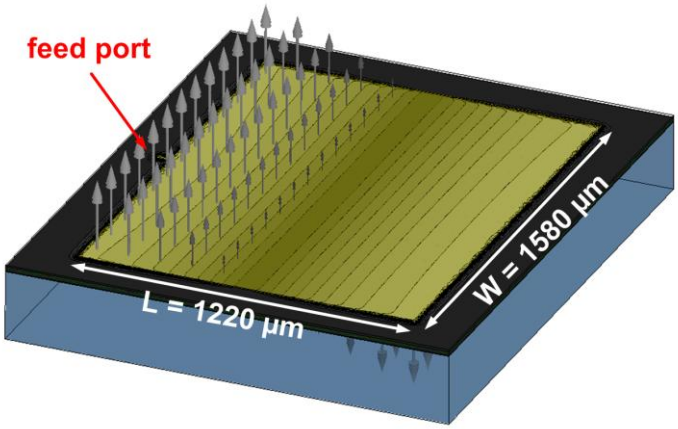


Fig. 6.2. Standing wave pattern on a 60GHz CMOS patch antenna design [45].

low resistivity and the high dielectric constant of Silicon, causing energy dissipated in the substrate instead of radiated into the air. Therefore, most of the antenna topologies without shielding from the lossy substrate have low radiation efficiency numbers, thus low antenna gains. Different types of on-chip antenna have been reported at 60 GHz bands [71]-[73]. Table 6.1 compares four common topologies of CMOS on-chip antennas. The patch antenna has the highest radiation efficiency and antenna gain due to the ground shielding the antenna from the lossy substrate, as shown in Fig. 1.10. Furthermore, the space below the patch antenna can potentially be used for integrating custom circuits (e.g. DSP and memory) in a SoC application. The patch antenna might occupy a relatively larger area compared to other types of antennas; however, if the reusable area beneath patch ground plane and the possibility of using patch antenna as frequency reference [14] are considered from a system point-of-view, the patch antenna is a good candidate for on-chip radio integration. In the next section, we will further discuss how to use patch antenna to realize a T/R switch-less antenna front-end.

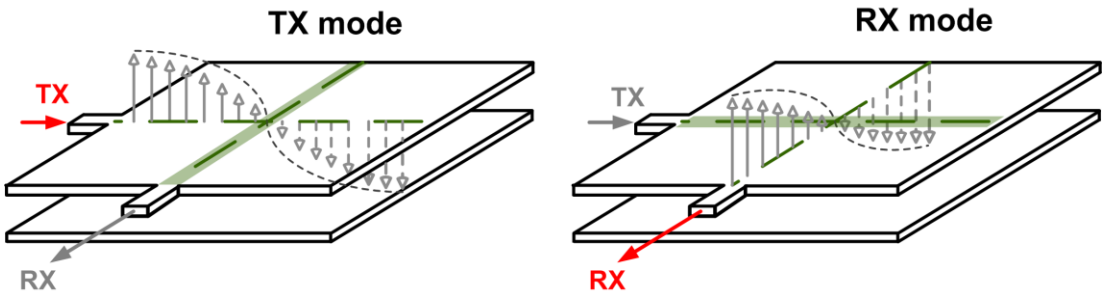


Fig. 6.3. T/R switch-less antenna front-end at its TX mode and RX mode with their corresponding standing wave patterns and electrical nulls (shaded area).

6.2.2. 60GHz Square Patch Antenna Design in CMOS

Microstrip patch antenna theory is well developed [46]. The width and the length of the patch are roughly half of the operation wavelength. The patch needs a ground plane to shield the substrate, which can be drawn in a lower metal layer in the CMOS process. The distance between the patch (top-metal) and the ground metal layer (intermediate metal layer) determines the height of the patch antenna. Fig. 6.2 shows the electric field distribution and vector plot of a simulated 60GHz CMOS patch antenna design [45]. It basically shows the standing wave pattern on the patch with its feeding port on the left, and the darker area represents a weaker electric field distribution. The electrical null represents a low-potential area, and it can either be un-connected or grounded with little effect on the antenna's operation. Therefore, the isolation between the feeding port and the electrical null is intrinsically high based on these fundamental characteristics of the patch antenna.

Fig. 6.3 shows the concept of the T/R switch-less antenna front-end. The TX feeding port and RX feeding port are placed in an orthogonal manner to share one antenna for transmission and reception with decent isolation between them. The TX and RX ports are

located at the center of the patch radiation edges, as a general feeding topology of patch antennas [46]. The patch needs to be square so that the structure is fully symmetrical, ensures TX and RX both operate at the same frequency for RF synchronization of the system. The TX port and RX port of a square patch antenna either transmit or receive data at any given time from the two orthogonal feeds. This location arrangement puts the RX port on the electrical null of the standing wave pattern when TX is transmitting, and vice versa. As a result, the T/R isolation is embedded and the mutual loading effect of the TX port and RX port can be minimized at the operation frequency. When the front-end is receiving data, the TX will be turned off, however leaving finite output impedance still connected to the TX port. However, it will not affect the RX since the TX port located at the null of the RX standing wave, equivalently connected to AC-ground. No receiving data will leak out to the TX port and there is no additional insertion loss (IL) caused by the T/R switch, thus maximizing the received signal power. Similarly, due to reciprocity, when the front-end is transmitting data, the RX port is protected by the intrinsic isolation. The TX output power is also exempt from the degradation of the IL of a T/R switch. Moreover, the linearity of the T/R switch-less antenna front-end is high because the structure is purely passive. It can handle high output power without distortion.

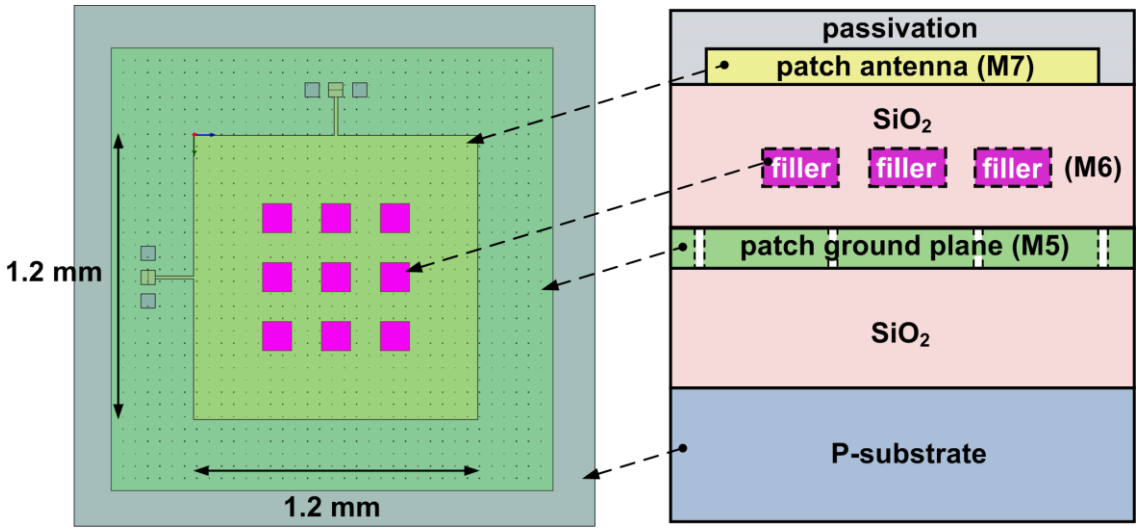


Fig. 6.4. The T/R switch-less antenna front-end design in CMOS 0.13μm technology.

Fig. 6.4 shows the T/R switch-less antenna front-end design in a standard CMOS 0.13μm technology with the layer mapping. The width and the length of the patch for the frequency of interest can be determined by the transmission line model [72]. In this case, a square patch is necessary. Let us recall the patch antenna design procedure at Chap. 2. With the center frequency, f_0, dielectric constant of the silicon dioxide (SiO_2), ε_r, and the height h, we can calculate the width, W, of the patch antenna by antenna theory [46]

$$W = \frac{c}{2 f_o \sqrt{\frac{(\varepsilon_r + 1)}{2}}} \tag{1}$$

where c is the speed of light. With the calculated W, we can find the effective dielectric constant, ε_{reff}

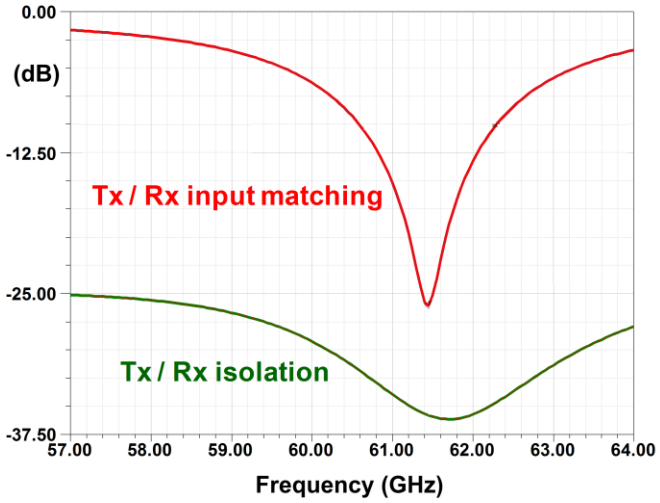
$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{\frac{-1}{2}} \tag{2}$$

It follows that the length of the patch antenna, L is

$$L = \frac{c}{2 f_o \sqrt{\varepsilon_{reff}}} - 0.824h \frac{(\varepsilon_{eff} + 0.3)(\frac{W}{h} + 0.264)}{(\varepsilon_{eff} - 0.258)(\frac{W}{h} + 0.8)} \quad (3)$$

The calculate *L* is the common length of the square patch. In addition, the dummy metal filling and slotting are also considered for fabrication in CMOS technology [45]. Dummy metal filler structures are therefore placed under the patch to meet this local density rule on M6 (Fig. 6.4). When placing fillers between the patch and the ground plane, it decreases the gain and varies the center frequency. Therefore, the fillers are carefully placed to minimize the performance degradation in a symmetrical pattern around the geometric center of the square patch. In this design, the height is 9.25μm, reserves 4 metal layers for possible circuit routing beneath the ground plane. The common length of the patch is 1200μm with two feeding lines (13μm x 163μm) connected to the probing pad that designed for 50Ω loadings.

Fig. 6.5 plots the simulated S-parameters and the antenna performance of the T/R switch-less antenna front-end (with fillers and slotted ground plane), showing isolation for at least 33dB throughout the entire bandwidth of the antenna. The RX matching doesn't change with the impedance loaded at the TX port. In practical applications, the properties of the antenna will be affected by application-specific scenarios in which objects are placed near the radiating element as we discussed in Chap. 3. Fig. 6.6 shows a simulation setup for characterizing the proximity effect when a conductor appears in close proximity to the antenna front-end. With a distance of 500 μm, where it causes 1σ standard deviation on center frequency (Chap. 2), the full-EM simulation shows that the isolation variation is less than 3dB throughout the pass band, showing a decent immunity against proximity conductor effect.



Technology	0.13μm BiCMOS
Center Frequency	61.4GHz
Efficiency	6% @ 61.4GHz
Peak Gain	-6.2dBi
Bandwidth	1.6GHz
Area	1.2mm x 1.2mm

Fig. 6.5. Simulated S-parameters and the antenna performance of the T/R switch-less antenna front-end.

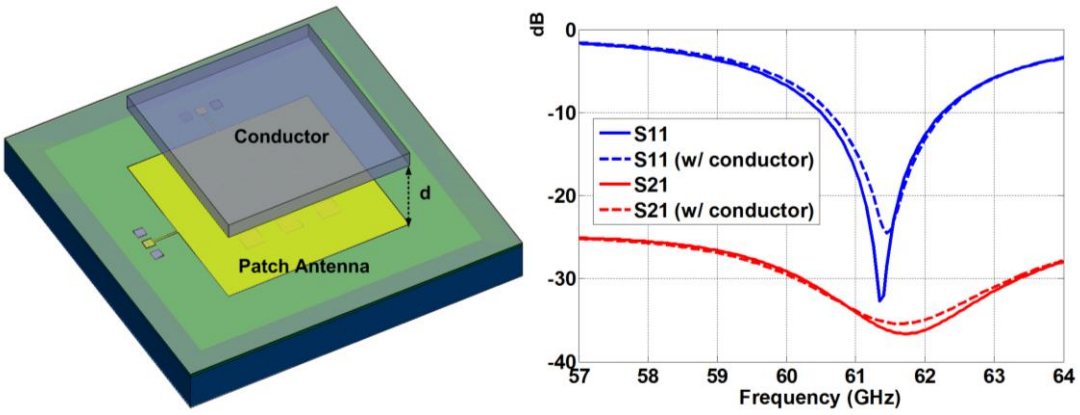


Fig. 6.6. Simulated proximity effect on matching and isolation of the antenna front-end.

6.3. Measurement Results

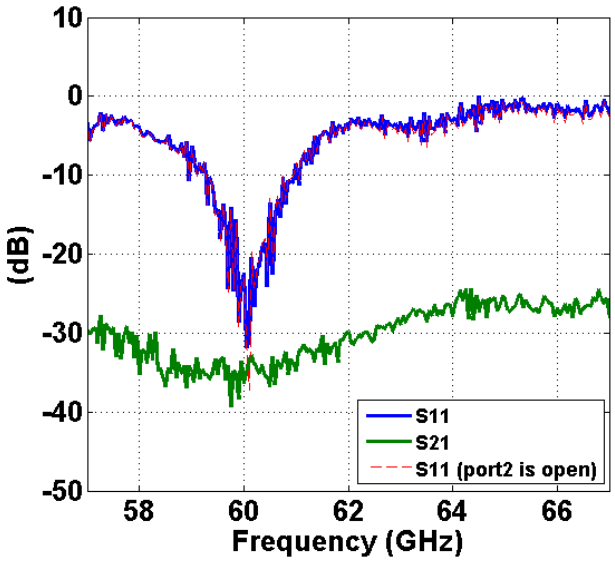


Fig. 6.7. Measured S-parameters of the T/R switch-less antenna front-end.

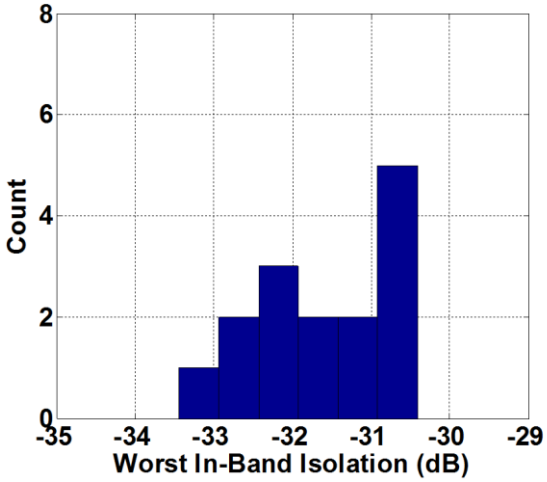


Fig. 6.8. Worst in-band isolation distribution measured from 15 dies.

Fig. 6.7 shows the measured S-parameters of the T/R switch-less antenna front-end from a high-speed probe station, showing consistent results with the simulation. The in-

	[66]	[67]	[68]	[69]	[70]	This Work
Technology	65nm CMOS	90nm CMOS	130nm CMOS	130nm CMOS	90nm CMOS	130nm BiCMOS
Frequency (GHz)	57-66	50-94	57-66	50-70	57-64	57-63
Insertion Loss (dB)	3.6	3.3	5.8	3	3.5	0
Return Loss (dB)	10	20	9.2	10	24	> 25
Isolation(dB)	26	27	24	25	34	> 30
P_{1dB} (dBm)	12	15	4.1	14	6.9	> 20
Area (μm^2)	240000	240000	221000	265500	324900	0

Fig. 6.9. Summary and comparison of the mm-wave T/R switches.

band isolation is always greater than 32dB, and the bandwidth is 1.68GHz. The input matching condition at the RX port doesn't change with the loading at the TX port, and vice versa. The measured center frequency is shifted by 2% from the simulation due to the limitation on simulating all of the micro slots on the ground plane and the fillers. However, the trend of having the largest isolation at resonance is identical for both measured and simulated cases. Fig. 6.8 shows the distribution of the worst in-band isolation measured from 15 dies. The mean is -31.6dB with an σ of 0.93dB, showing robust result over process variation. Fig. 6.9 summarizes the performance as if a built-in T/R switch within the patch antenna and compares it with other T/R switches at mm-wave range. Finally, a die photo of the design is shown in Fig. 6.10.

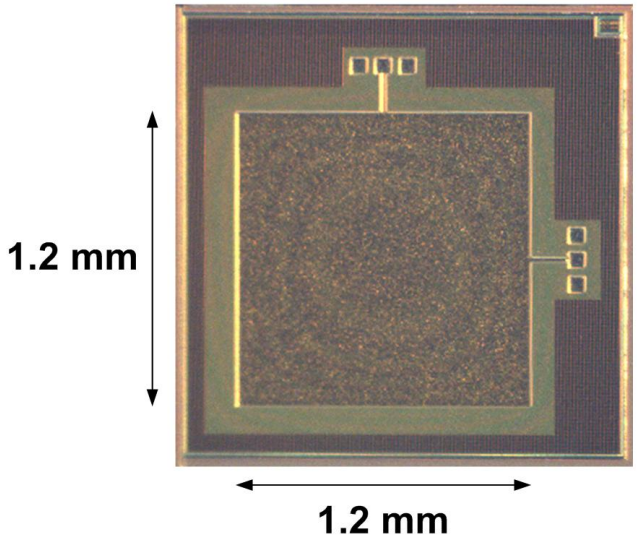


Fig. 6.10 Die photo of the T/R switch-less antenna front-end.

6.4. Conclusion

A 60GHz T/R switch-less antenna front-end using an on-chip patch antenna is presented, which has an in-band isolation (>32dB) inherited from the standing wave pattern on the patch antenna at resonance. The TX port and RX port of a square patch antenna either transmit or receive data at any given time from two orthogonal feeds. This location arrangement puts the RX port on the electrical null of the standing wave pattern when TX is transmitting, and vice versa. As a result, the T/R isolation is embedded and the loading effect of TX and RX can be minimized at the operation frequency. The antenna front-end doesn't require spare area for a T/R switch. Therefore, no additional insertion loss is incurred. Moreover, the linearity of the front-end system is better than the ones with FETs-based switches because it is purely passive, so that it can handle large power at the TX output without nonlinear distortion. The performance along with its area efficiency show promising results for the realization of mm^3-scale radio system.

Chapter 7
Conclusion

The continual evolution of computing devices has changed daily life significantly over the past several decades, and it is still advancing towards pervasive and ubiquitous networks. Reducing size and cost are the key factors for achieving this goal. Bell's Law has continued to hold from mainframes to smartphones, continuing into wireless sensor networks being the next big step along the journey. In general, a cubic-mm scale WSN node system is foreseen on the roadmap. However, compact hardware design at this unobtrusive scale is quite challenging, and that is the reason why there is no cubic-mm WSN node yet. The first issue is there are non-scaling components in the device like the crystal. Its resonance frequency is fixed and it cannot be integrated onto silicon. Another obstacle is the reduced energy source as the size shrinks. Unfortunately, energy sources, such as the battery and solar cell, have been slow to improve relative to the CMOS scaling trend. As a result, energy must be conserved in the WSN node by reducing the power consumption of the circuit components. The antenna is another issue when integrating with silicon towards smaller profile. The loss of antenna gain needs higher power to compensate for communication over the same distance. Having a higher operation frequency is also helpful for size reduction, however, the path loss is increased, and the circuits need to consume more power to achieve required performance. Showing trade-offs between energy source and system size. All of the issues are bundled together, and need to be optimized as a whole. Therefore, this thesis has investigated new methods to eliminate the bulky crystal reference for the miniaturization of the WSN node from a

system perspective, while reducing the overall power consumption for longer lifecycle of operation.

A frequency-locked loop (FLL) in a 0.13µm CMOS process using an on-chip patch antenna as both the radiator and the frequency reference has been demonstrated. The proposed technique efficiently integrates the antenna, eliminates the need for a crystal reference, is FCC compliant, and ensures the node transmits at the antenna's peak efficiency. The substrate beneath the antenna is shielded by an intermediate metal layer ground plane, freeing up space for active circuits and routing beneath the patch. By integrating circuits in CMOS underneath the patch, and stacking the die on e.g. a thin-film battery, a fully integrated, cost-effective, mm^3-scale WSN node is feasible.

A 10GHz IR-UWB crystal-less TX in an 180nm BiCMOS process with an on-chip monopole antenna has been demonstrated. It operates over the supply voltage range of a micro battery, generate tunable pulse durations and center frequencies, and lives on an on-chip local decoupling capacitor (decap) only. The PVT variations are calibrated out by the one-time frequency tuning mechanism and wide-band communication technique. When the TX is active, it draws maximum on-current to generate the largest signal possible for the longest communication distance. The TX is designed for heavily duty-cycled operations, showing the way to cope with limited micro battery performance.

A low-power, temperature-compensated relaxation oscillator for mm^3 WSN applications is designed and fabricated in a standard 130nm CMOS process. An RC network of the oscillator is proposed with a transmission zero for temperature compensation. It introduces an additional degree-of-freedom for relaxation oscillator design and maintains temperature compensation over a frequency tuning range using

conventional CMOS resistor and capacitor options. The oscillator offers a good balance between power, area, oscillation frequency, frequency stability and leakage power, showing a good candidate for crystal oscillator replacement.

A 60GHz T/R switch-less antenna front-end using an on-chip patch antenna is presented, which has an in-band isolation (>32dB) inherited from the standing wave pattern on the patch antenna at resonance. The TX port and RX port of a square patch antenna either transmit or receive data at any given time from two orthogonal feeds. This location arrangement puts the RX port on the electrical null of the standing wave pattern when the TX is transmitting, and vice versa. As a result, the T/R isolation is embedded and the loading effect of TX and RX can be minimized at the operation frequency. The antenna front-end doesn't require spare area for a T/R switch. Therefore, no additional insertion loss is incurred. Moreover, the linearity of the front-end system is better than the ones with FETs-based switches because it is purely passive, so that it can handle large power at the TX output without nonlinear distortion. The performance along with its area efficiency show promising results for the realization of mm^3-scale WSN system.

References

[1] G. Bell, "Bell's Law for the Birth and Death of Computer Classes," *Commun. ACM*, vol. 51, no. 1, pp 86-94, Jan. 2008

[2] T. Nakagawa *et al.*, "1-cc Computer: Cross-Layer Integration with UWB-IR Communication and Locationing," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 964-973, Apr. 2008.

[3] J. Bryzek, "Emergence of a $Trillion MEMS Sensor Market", *SensorsCon*, March 2012.

[4] I.F. Akyildiz *et al.*, "A Survey on Sensor Networks," *IEEE Commun. Mag.*, pp. 102-114, Aug. 2002.

[5] K. Romer and F. Mattern, "The Design Space of Wireless Sensor Networks," *IEEE Wireless Commun.*, vol. 11, no. 6, pp. 54-61, Dec. 2004.

[6] D. Puccinelli and M. Haenggi, "Wireless Sensor Networks: Applications and Challenges of Ubiquitous Sensing," *IEEE Circuits Syst. Mag.*, vol. 5, no. 3, pp. 19-31, 2005.

[7] J. Yick, B. Mukherjee, and D. Ghosal, "Wireless Sensor Networks Survey," *J. Comput. Networks*, vol. 52, no. 12, pp. 2292-2330, Apr. 2008.

[8] P. Corke *et al.*, "Environmental Wireless Sensor Networks," *in Proc. IEEE*, vol. 98, no. 11, pp. 1903-1917, Nov. 2010.

[9] B.H. Calhoun *et. al.*, "Body Sensor Networks: A Holistic Approach from Silicon to Users," *in Proc. IEEE,* vol. 100, no. 1, pp. 91-106, Jan. 2012.

[10] I. Matijevics, J. Simon, Control of the Greenhouse's Microclimatic Condition using Wireless Sensor Network, IPSI Journal, TIR, Vol. 6, No. 2, pp. 35-38, 2010.

[11] B. Carkhuff and R. Cain, "Corrosion Sensors for Concrete Bridges," *IEEE Instr. Meas. Mag.*, vol. 6, no. 2, Jun. 2003.

[12] G. Chen, S. Hanson, D. Blaauw, and D. Sylvester, "Circuit Design Advances for Wireless Sensing Applications," *in Proc. IEEE,* vol. 98, no. 11, pp. 1808-1827, Nov. 2010.

[13] G. Chen *et al.*, "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *ISSCC Dig. Tech. Papers*, pp. 310-311, Feb. 2011.

[14] K. -K. Huang, and D. D. Wentzloff, "A 60 GHz Antenna-Referenced Frequency-Locked Loop in 0.13μm CMOS for Wireless Sensor Networks," *in IEEE J .Solid-State Circuits*, Vol. 46, No. 12, Dec. 2011, pp. 2956-2965.

[15] G. Chen *et al.*, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," *ISSCC Dig. Tech. Papers*, pp. 288-289, Feb. 2010.

[16] Cymbet Corp., *EnerChip Smart Solid State Batteries*, (2012, Feb. 6) [Online]. Available: http://www.cymbet.com/products/enerchip-solid-state-batteries.php.

[17] Samsung SDI, *Prismatic Rechargeable Battery*, (2012, Feb. 6) [Online]. Available: http://samsungsdi.com/battery/prismatic-rechargeable-battery.jsp.

[18] Y. Nishi, "Lithium Ion Secondary Batteries; Past 10 Years and the Future," *J. Power Sources*, vol. 100, no. 1-2, pp. 101-106, Nov. 2001.

[19] A.H. Zimmermann and M.V. Quinzio, “Performance of SONY 18650-HC Lithium-Ion Cells for Various Cycling Rates,” Aerospace Corp., El Segundo, CA, Tech. Rep. TR-2010(8550)-5, Jan. 2010.

[20] S. Hossain *et al.*, “Lithium-Ion Cells for Aerospace Applications,” *in Proc. 32nd Intersociety Energy Conversion Eng. Conf.*, vol. 1, pp. 35-38, Aug. 1997.

[21] “CGR18650D: Cylindrical Model,” Panasonic Corp., Product Spec., CGR18650D, Jun. 2005.

[22] “Panasonic Batteries Energy Catalog,” Panasonic Corp., Rolling Meadows, IL, Product Spec., PIC-PanBat-FY11-PanaEnergyCatalog, 2011.

[23] S. Hanson, M. Seok, Y.-S. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, “A low-voltage processor for sensing applications with picowatt standby mode,” *IEEE J. Solid-State Circuits*, vol. 44, no. 4, Apr. 2009, pp. 1145-1155.

[24] H.-J. Lee, A.M. Kerns, S. Hyvonen, and I.A. Young, “A Scalable Sub-1.2mW 300MHz-to-1.5GHz Host-Clock PLL for System-on-Chip in 32nm CMOS,” *ISSCC Dig. Tech. Papers*, pp. 96-97, Feb. 2011.

[25] Sundaresan, K., Ho, G.K., Pourkamali, S., Ayazi, F., "Electronically Temperature Compensated Silicon Bulk Acoustic Resonator Reference Oscillators", *Solid-State Circuits, IEEE Journal of,* On page(s): 1425 - 1434 Volume: 42, Issue: 6, June 2007

[26] “Temperature Compensated Crystal Oscillators (TCXO),” Vectron Corp., Product Spec., VT820 Series, 2009.

[27] “Standard Frequency Hugh Performance MEMs VCTCXO,” SiTime, Product Spec., SiT5000, 2012.

[28] “Single-Ended Output Silicon Oscillator,” Silicon Labs, Product Spec., Si500S, 2011.

[29] C. Wang , Y. Cho , C. Lin , H. Wang , C. Chen , D. Niu , J. Yeh , C. Lee and J. Chern "A 60 GHz transmitter with integrated antenna in 0.18 µm SiGe BiCMOS Technology", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 2006 .

[30] T. Yao , L. Tchoketch-Kebir , O. Yuryevich , M. Q. Gordon and S. P. Voinigescu "65 GHz Doppler sensor with on-chip antenna in 0.18 µm SiGe BiCMOS", *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 2006 .

[31] B. W. Cook, S. Lanzisera and K. S. J. Pister, “SoC Issues for RF Smart Dust,” in *Proc. IEEE*, vol. 94, pp. 1177-1196, Jul. 2006.

[32] B. Warneke, M. Last, B. Liebowitz, and K. S. J. Pister, “Smart Dust: Communicating with a Cubic-Millimeter Computer,” in *Computer*, vol. 34, pp. 44-51, Aug. 2002.

[33] B.W. Cook, A. D. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister., “An Ultra-Low Power 2.4GHz RF Transceiver for Wireless Sensor Networks in 0.13um CMOS with 400mV Supply and an Integrated Passive RX Front-End,” in *IEEE ISSCC 2006 Dig. Tech. Papers*, pp. 1460-1461 Feb. 2006.

[34] D. Steel. (2005, Mar). Title. *Smart Dust* [UH ISRC Technology Briefing]. Available: http://www.bauer.uh.edu/uhisrc/FTB/Smart%20Dust/Smart%20Dust.pdf

[35] *MPR/MIB User’s Manual*, Crossbow Technology Inc., San Jose, CA, 2004.

[36] *TELOS-B User's Manual*, Crossbow Technology Inc., San Jose, CA, 2004.

[37] *Cricket v2 User Manual*, MIT Computer Science and Artificial Intelligence Lab., Cambridge, MA, 2005.

[38] *uPart 014xilmt datasheet*, Particle Team, University of Karlsruhe., Karlsruhe, Germany, 2006.

[39] *TC-Link mXRS User Manual*, MicroStrain Inc., Williston, VT, 2010.

[40] *SG-Link mXRS User Manual*, MicroStrain Inc., Williston, VT, 2010.

[41] *MOTIONBEE datasheet*, STMicroelectronics Inc., Geneva, Switzerland, 2009.

[42] e-CUBES project IST-026461. [Online]. Available: http://www.ecubes.org

[43] G.K.Fedder. "CMOS-Based Sensors," in *IEEE Sensors 2005*, pp. 125-128 Oct. 2005.

[44] Y. Lee, G. Chen, S. Hanson, D. Sylvester, d. Blaauw, "Ultra-low power circuit techniques for a new class of sub-mm^3 sensor nodes," in *IEEE CICC 2010*, Nov. 2010.

[45] K.-K. Huang, and D. D. Wentzloff, "60GHz On-Chip Patch Antenna Integration in a 0.13-um CMOS Technology," *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2010.

[46] C. A. Balanis, Antenna Theory: Analysis and Design, 2nd ed. New York: Wiley, 1997, ch. 4

[47] D. M. Pozar, Microwave Engineering,3rd ed. New York: Wiley, 2005.

[48] M. Pelgrom, A. Duinmaijer, A. Welbers and A.P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.

[49] J. Lee, Y. Huang, Y. Chen, Hsinchia Lu, and Chiajung Chang, "A Low-Power Fully Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly," in *IEEE ISSCC 2009 Dig. Tech. Papers*, pp. 315-316, Feb. 2009.

[50] Agilent Technologies, "N5247A PNA-X Microwave Network Analyzer," data sheet, Dec. 2010 [Online]. Available: http://cp.literature.agilent.com/litweb/pdf/N5247-90002.pdf

[51] J. Lee, "A 75-GHz PLL in 90-nm CMOS Technology," in *IEEE J.Solid-State Circuits,vol.43, no.6*, pp. 1414-1426, Jun. 2008.

[52] C. Lee, and S.-I. Liu, "A 58-to-60.4GHz Frequency Synthesizer in 90nm CMOS," in *IEEE ISSCC 2007 Dig. Tech. Papers*, pp. 195-197, Feb. 2007.

[53] T. Lee and W. Lee, "A spur suppression technique for phase-locked frequency synthesizers," in *IEEE ISSCC 2006 Dig. Tech. Papers*, Feb. 2006, pp. 592–593.

[54] J. Ryckaert *et al*., "A 0.65-to-1.4nJ/burst 3-to-10GHz UWB all-digital TX in 90nm CMOS for IEEE802.15.4a," *IEEE J. Solid-State Circuits*, vol. 42, no.12, pp. 2860-2869, Dec. 2007.

[55] X. Wang *et al*., "A whole-chip ESD-protected 0.14-pJ/p-mV 3.1-10.6GHz impulse-radio UWB transmitter in 0.18-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no.4, pp. 1109-1116, Apr. 2011.

[56] S. Sim *et al*., "A CMOS UWB pulse generator for 6-10 GHz Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no.2, pp. 83-85, Feb. 2009.

[57] J. Ryckaert *et al*., "Ultra-wide-band transmitter for low-power Wireless Body Area Networks: design and evaluation," *IEEE Trans. Circuits Syst. I, Regular. Papers,* pp. 2515-2525, Dec. 2005.

[58] V. Kulkarni, et al., "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB Transmitter With Embedded On-Chip Antenna", JSSC, vol. 44, no. 2, pp. 394-403, Feb. 2009

[59] S. Radiom, M. Baghaei-Nejad, K. Aghdam, G. A. E. Vandenbosch, L.-R. Zheng, and G. G. E. Gielen, "Far-fi "F on-chip antennas monolithically integrated in a wireless-powered 5.8-GHz downlink/UWB uplink RFID tag in 0.18-um standard CMOS," IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1746–1758, Sep. 2010

[60] Y. Lee, G. Kim, S. Bang, Y. Kim, I. Lee, P. Dutta D. Sylvester. and D. Blaauw, "A modular 1mm^3 die-stacked sensing platform with optical communication and multi-modal energy harvesting," *ISSCC Dig. Tech. Papers*, pp. 402-403, Feb. 2012.

[61] K. Choe, O. D. Bernal, D. Nuttman, M. Je., "A Precision Relaxation Oscillator with a Self-Clocked Offset-Cancellation Scheme for Implantable Biomedical SoCs," *ISSCC*, pp. 402-403, Feb. 2009.

[62] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts and B. Nauta., "A 65-nm CMOS Temperature-Compensated Mobility-Based Frequency Reference for Wireless Sensor Networks," *IEEE J. Solid-State Circuits*, vol. 46, no.7, pp. 1544-1552, Jul. 2011.

[63] F. Golnaraghi, and B. C. Kuo, Automatic Control Systems, 9th ed. New Jersey: Wiley, 2010.

[64] V. D. Smedt, P. D. Wit, W. Vereecken, and M. S. J. Steyaert., "A 66 μW 86 ppm/°C Fully-Integrated 6 MHz Wienbridge Oscillator with a 172 dB Phase Noise FOM," *IEEE J. Solid-State Circuits*, vol. 44, no.7, pp. 1990-2001, Jul. 2009.

[65] T. Tokairin, K. Nose, K. Takeda, K. Noguchi, T. Maeda, K. Kawai and M. Mizuno, "A 280nW, 100kHz, 1-Cycle Start-up Time, On-chip CMOS Relaxation Oscillator Employing a Feedforward Period Control Scheme," *IEEE Symp. on VLSI Circuits,* June 2012.

[66] J. He, and Y. P. Zhang, "Design of SPST/SPDT switches in 65 nm CMOS for 60-GHz applications," *IEEE Asia Pacific Microw. Conf.*, Dec. 2008, pp. 1-4.

[67] S.-F. Chao, H. Wang, C.-Y. Su, and J. G. J. Chern, "A 50-94 GHz CMOS SPDT switch using traveling-wave concept," *IEEE Microwave Wireless Compon. Lett*., vol. 17, no. 2, pp.130-132, February 2007

[68] C. M. Ta, E. Skafidas, R. J. Evans, "A 60 GHz CMOS transmit/receive switch," *IEEE RFIC Symp. Dig*., pp. 725-728, June 2007.

[69] Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, ''Low-loss 0.13-μm CMOS 50-70 GHz SPDT and SP4T switches,'' *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.Dig.*, Jun. 2009, pp. 43-46.

[70] C.-S. Kuo, H.-C. Kuo, H.-R. Chuang, C.-Y. Chen, and T.-H. Huang, "A high-isolation 60 GHz CMOS transmit/receive switch," *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig*. pp 1–4, June, 2011.

[71] A Babakhani, X Guan, A Komijani, A Natarajan, and A.Hajimiri, "A 77-GHz Phased-Array Transceiver with On-Chip antennas in silicon: Receiver and Antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795-2806, Dec. 2006.

[72] T. Yao , L. Tchoketch-Kebir , O. Yuryevich , M. Q. Gordon and S. P. Voinigescu "65 GHz Doppler sensor with on-chip antenna in 0.18 µm SiGe BiCMOS", *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 2006.

[73] C. Wang , Y. Cho , C. Lin , H. Wang , C. Chen , D. Niu , J. Yeh , C. Lee and J. Chern "A 60 GHz transmitter with integrated antenna in 0.18 µm SiGe BiCMOS Technology", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 2006.