Wireless Interconnect using Inductive Coupling in 3D-ICs

by

Sang Wook Han

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2012

Doctoral Committee:

Assistant Professor David D. Wentzloff, Chair
Professor David Blaauw
Professor Karl Grosh
Professor John Patrick Hayes

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF APPENDICES

Chapter I.
Introduction

Since invented in the early 20th century, printed circuit boards (PCB) have been the most common method to integrate electrical devices to complete a system. In the initial day of electronics, most circuits were composed of only a small number of discrete components on a PCB. However, as the circuits became complicated, it was necessary to increase the number of components involved in order to make technical advances. The monolithic integrated circuit (IC), the integration of a large numbers of tiny transistors into a small-sized chip, was developed in the mid-20th century [1]. Because ICs enabled lower manufacturing cost and higher performance with lower power than discrete circuits, they were attractive economically and technically, and there were a lot of efforts to achieve higher integration density in ICs. The efforts resulted in very-large-scale integration (VLSI), which today integrates 1B transistors into a single chip.

In order to maximize the benefit of integration, all components needed for a system were integrated into a single chip called a system-on-a-chip (SoC) [2]-[5]. Since an SoC allows a reduced number of components on the PCB, it enables lower assembly cost, lower total size, and reduced power consumption. Therefore, an SoC is a useful solution

for a mobile platform which requires low power and small form-factor, and semiconductor suppliers such as Samsung, TI, and nVidia have developed various types of SoCs for mobile application [6]-[8] Notably, the Snapdragon series from Qualcomm integrates most of the main features required for a smart phone. Because they successfully combine application processing units and wireless connectivity blocks, they provide a one-chip solution reducing the complexity of the PCB and the total power [9].

The design of an SoC, however, requires higher non-recurring engineering (NRE) cost and a longer turn-around time due to its complexity. In addition, excessive integration of disparate components into a single substrate might cause performance degradation and lower yield. Another integrating method, system-in-a-package (SiP) [10]-[12], is able to alleviate these problems. A SiP is a combination of individual ICs enclosed in a single package. For instance, modern memory chips stack multiple memory dies vertically inside a single package as shown in Fig. I.2 [13]. And, most application processors for smart phones include memory in the form of package-on-package to reduce the footprint and enhance the performance [14]. SiP has the same advantages as SoC such as reduced complexity of the PCB and overall design, and smaller total size. Moreover, it provides reasonable design cost and short turnaround time because each component may be designed, fabricated, and verified separately and prior to integration into the complete system. Furthermore, SiP enables heterogeneous integration, which means a combination of different processes such as CMOS logic and DRAM can be integrated [13]. Heterogeneous integration is not possible on SoC implementations because all

components must share the same substrate. Fig. I.1 illustrates the trade-off between performance, cost, and time-to-market of different integration methods.

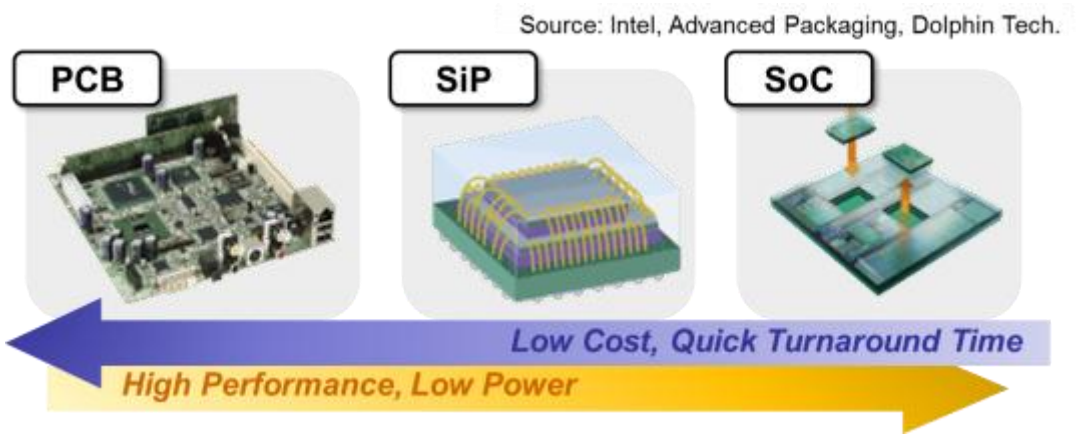


Fig. I.1. Comparison of different methods to integrate system integration.

There are various types of advanced package options for SiPs such as multi-chip modules (MCM), package-in-package (PIP), and package-on-package (POP). In these methods, the dies are connected together with conventional wire-bonding or micro-bump technologies [15][16]. However, wire-bonding has relatively large parasitic resistance, capacitance, and inductance, which degrades the performance. Micro-bumping provides better performance than wire-bonding, but it requires an additional re-distribution layer (RDL) between die. Otherwise, only face-to-face stacking is permitted [17]. Since the RDL is a set of long metal traces on a substrate, it causes performance degradation due to its parasitic capacitance. To eliminate an RDL layer, multiple die can be stacked on top of each other with wire-bonding [18] or micro-bumping [19] between layers. However, in these stacked SiPs, both wire-bonding and micro-bumps are located on only the perimeter of the stacked dies. This limits the maximum number of interconnects between layers, and requires that a signal generated near the center of one die be first routed to the edge

prior to connecting to another layer in the stack. While a SoC does not have a similar constraint on the maximum number of interconnects, the power dissipated in the interconnect across a large area die has become critical in sub-micron processes.

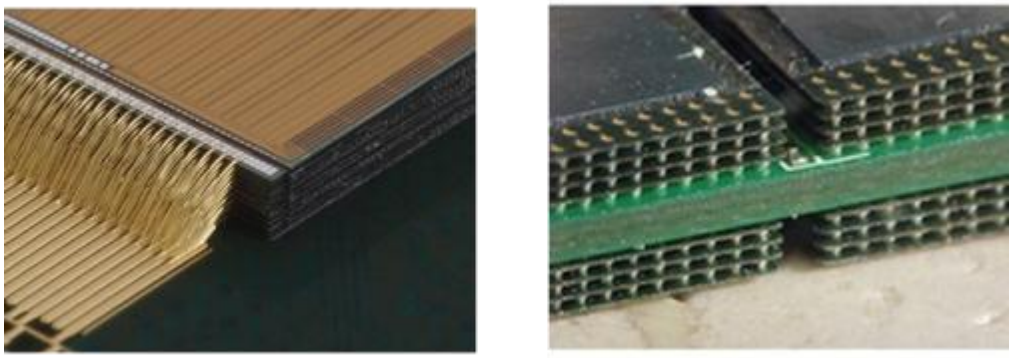


Fig. I.2. Die stacking with wire-bonding (left) and POP with mirco-bumps (right) [Elpida]

I.1 3DIC

The number of transistors per unit area doubles approximately every 2 years (Moore's law) [20]. As transistor size continuously shrinks down, transistor switching performance has continued to improve with every process generation. However, interconnects between transistors have comparatively deteriorated in performance [21]. Therefore, as transistors shrink, interconnect latency becomes more critical than transistor switching speed as shown in Fig. I.3. In order to reduce the RC delay of long interconnects, a number of buffers and flip-flops are necessary to partition them into segments, and these components consume considerable power. In modern micro-processors, the power dissipated in interconnects takes more than one third of the total power consumption [22]. The only way to decrease the power consumption of interconnect without compromising

performance is to reduce the interconnect length. However, interconnections for global routing across an entire IC become inevitably long in most modern semiconductor processes in which transistors are placed in a single plane.

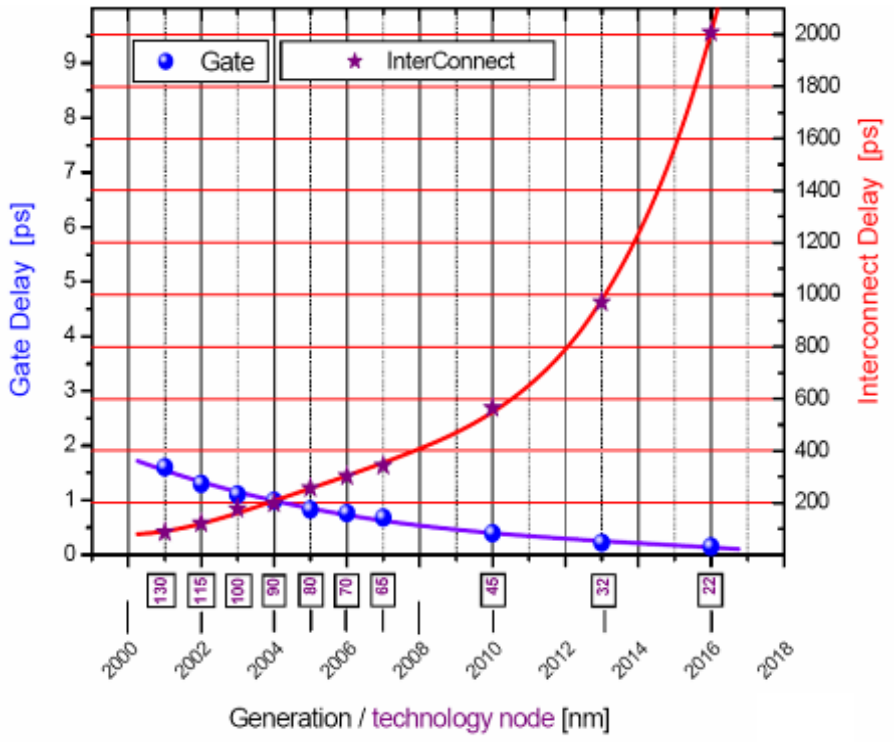


Fig. I.3. Interconnect speed and performance relationship. Beyond 130nm, interconnect delay is dominant. [23]

In order to shorten interconnect in a sub-micron process, methods to integrate multiple device layers three dimensionally have been proposed, termed 3DIC. The major benefit of 3D integration is the reduced interconnects length resulting in smaller RC delay as shown in Fig. I.4. It requires smaller sized buffers and a smaller number of flip-flops [24], and this saves power consumption significantly. In addition, since it converts a planar IC requiring a large area into a three dimensional structure, it achieves a smaller footprint chip, which is essential for mobile devices. The key feature differentiating a 3DIC from a SiP implementation of stacked die with perimeter connections is that a

3DIC is a single chip. All layers in a 3DIC communicates via on-chip interconnects rather than off-chip paths such as wirebonding, microbumpimg and RDL.

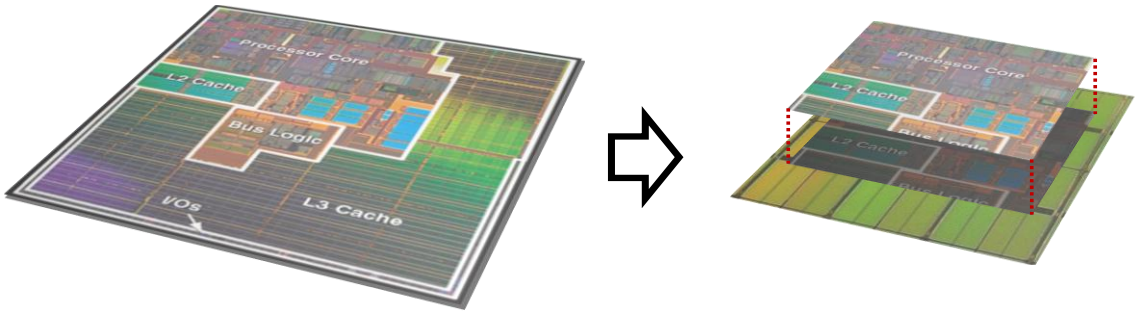


Fig. I.4. Vertical stacking can reduce the length of global interconnect.

Various methods have been proposed to achieve 3D integration, such as vertical transistors [25][26] and vertical circuits [27], but these have not been successful due to the technical difficulty of manufacturing. The most promising method for 3DICs is vertical stacking of multiple wafers with some form of vertical interconnect through the wafer. Even though a 3DIC cannot increase the integration density within a wafer, it enhances the performance and reduces the size of a system by increasing the integration density in a system as shown in Fig. I.5. For this reason, 3DIC is often times viewed as extending Moore's law by packing more transistors into a chip, but doing so using mature silicon technology [28].

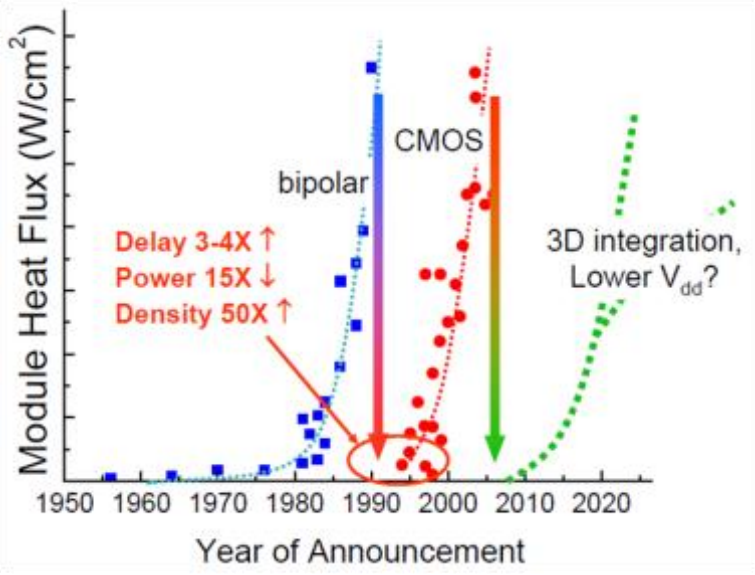


Fig. I.5. 3DIC can increase integration density after planar CMOS process. [29]

I.2 Through-Silicon-Vias

Since a general semiconductor die has openings for electrical connections on only the top surface, it is not proper for vertical stacking. In order to create a 3DIC, electrical connections passing completely through the silicon substrate are necessary. These are called through-silicon-vias (TSVs). Compared to 3D packages such as edge wire-bonding and interposers [30], TSVs allow a high density of vertical interconnects between IC layers that can be placed anywhere on the IC and not just along the perimeter. In addition, because of its smaller parasitic capacitance, inductance, and resistance, a TSV enables high speed and low power. However, a TSV requires extra processing steps when manufacturing the IC, and its manufacturing is still unstable. There has been active research to resolve these issues and improve the TSV process in many companies such as

Tezzaron [31], EVG [32], ZyCube [33], and IMEC [34]. Recently, a 32GB-capacity DRAM module was developed for servers by Samsung using 3DIC technology [35]. It is 67% faster than their previously existing module, and its power consumption is at least 30% less. The TSV technology of Samsung is shown in Fig. I.6.

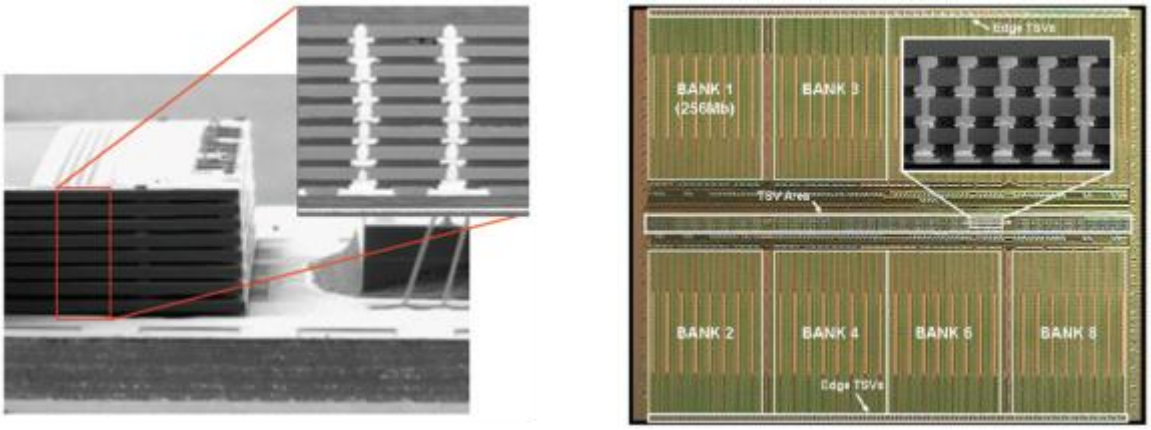


Fig. I.6. Multiple stacked die (left) and photo of DRAM die adapting TSVs (right) [Samsung]

I.3 Capacitive Coupling

TSVs are vertical directly contacted interconnects. They are attractive for 3DIC interconnect, and commercial foundries are recently demonstrating heterogeneous 3D stacks using TSVs. However, TSVs are not nearly as ubiquitous as the planar metallization layers in ICs have been for decades. Non-contact interconnects can also be implemented using wireless techniques such as capacitive coupling [36] or inductive coupling [37]. Therefore, in processes that aren't amenable to TSVs, wireless signal and power transfer between 3DICs using existing metal layers is a better option than reverting to traditional planar packaging. Wireless interconnect using capacitors or inductors is compatible with nearly all planar processes, allows communication between IC layers,

and enables wireless testing of ICs before they are vertically stacked (currently not an option for TSV processes).

The capacitive coupling method transfers the signal by means of the capacitance between two nodes. A capacitive channel is created by placing small metal plates on two silicon dies and stacking two dies so that the metal plates are parallel and close to each other, creating a capacitor. This capacitor connects two circuits by passing an AC signal through it.

Compared to other wireless interconnect methods, capacitive coupling methods have the advantages of simple channel modeling and less crosstalk due to a more confined electrical field [38]. However, its communication distance is limited to only several microns. Since capacitors are basically voltage-driven devices, the voltage across a capacitor should be increased to extend the communication range. In most CMOS process, increasing the signal voltage over the power supply voltage is difficult and may cause devices to break down, which leads to limited communication distances for capacitive coupling interconnect. Furthermore, capacitive coupling only allows face-to-face stacking of two dies.

The short range communication of capacitive coupling can be exploited for wireless testing [39]. Conventional wafer level testing requires a probe card with a large numbers of needles. Since the needle tips make physical contacts on a wafer with a strong force, abrasion and deformation of the needle tips is unavoidable, which increases testing cost [41]. Capacitive coupled wireless testing can eliminate the mechanical contacts and their

corresponding problems. In addition, capacitors for wireless testing can be re-used for wire bonding pads [42].

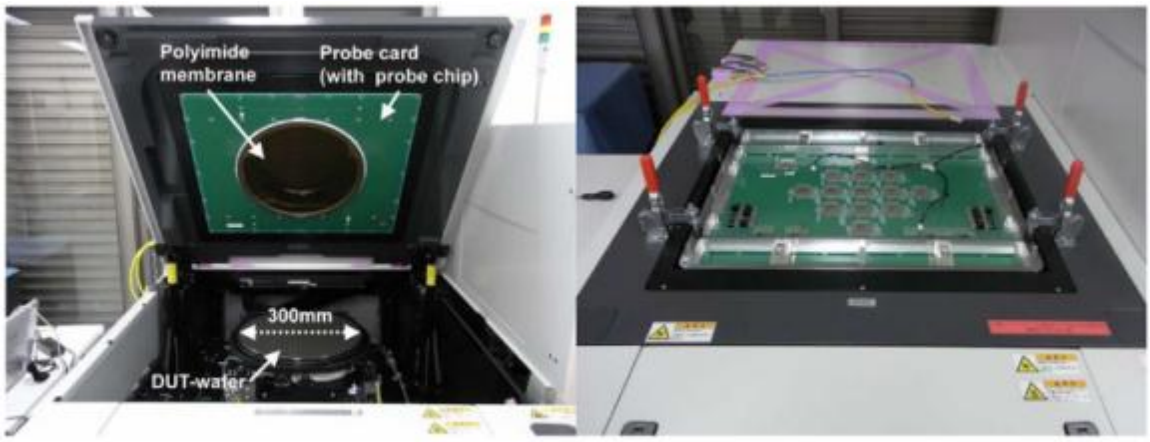


Fig. I.7. Wireless wafer level tester using capacitive coupling (a) head plate open (b) head plate closed [40]

I.4 Inductive Coupling

Wireless inductive coupling methods rely on the coupled magnetic field between a planar spiral inductor pair [43]. Time-varying current in a transmitting coil generates magnetic flux, which induces an electromotive force (EMF) in a receiving coil. An inductive data link transmits data in the form of AC current and senses the induced EMF at the receiver side. And inductive power link collects the EMF and converts it into a usable power source on the receiving IC. The signal strength and power amount is proportional to the amount of linked magnetic flux between the coupled inductor pair. Since an inductor is a current-driven device, this magnetic flux around an inductor in

increased by increasing the current, which is an easier problem than increasing voltage for capacitive coupling in most modern CMOS processes.

The challenges of implementing an inductive link are the typical small aspect ratio and relatively high power consumption compared to TSVs. The strength of the EMF at a receiving coil is proportional to the coupling coefficient *k* between the coils, and the current in the transmitting coil. The coupling coefficient *k* is proportional to the coil size and inversely proportional to the distance between two coupled coils [44]. Therefore, in order to extend the distance between two coils, which in the case of 3DICs is the distance between two stacked die, larger coils are required to maintain *k*, which results in the same aspect ratio. To achieve a larger aspect ratio, the transmitted current could be increased, but this typically results in more power consumption. To avoid increasing power, several circuit techniques have been proposed. Previous work used a sense amplifier in the receiver to compensate for the reduced *k* [46][47]. A phase shaping method has been used to increase the $\frac{\partial I_T}{\partial \mathrm{t}}$ term [48]. However, these require precise sampling to synchronize the data across 3DIC layers. A hysteretic comparator was used to achieve very low energy per bit [49], however its application is limited to high speed and high power, and the aspect ratio of the coupled coils is still a concern.

This thesis seeks to resolve the challenges of inductive coupling by achieving longer distance without increasing power or decreasing aspect ratio. This is accomplished using a technique known as resonant inductive coupling, which is a better way to use coupled inductors for both inductive data links and inductive power links. In addition, this work develops the necessary circuit techniques to exploit the proposed inductive channel.

I.4.1 **Inductive Data Link**

Similar to capacitive coupling interconnect, wireless inductive coupling using planar spirals is compatible with most planar processes. In addition, the communication range of an inductive data link can be extended by increasing the transmitting current, and it allows communication through multiple IC layers. The inductive data link is the result of a trade-off between power, distance, and cost. While larger coils can achieve longer communication distance, they require more silicon area [50]. More transmitting current can extend communication distance without increasing coil size, but it consumes more power. Previous work presented a better trade-off between area and power, but failed to achieve longer distance [46]-[51]. This is because their interconnect solutions rely on standard inductive coupling using air-core, planar spiral inductors. This results in poor efficiency (<5%) and a relatively short communication distance (~15μm) because most of the flux is not linked between the coils.

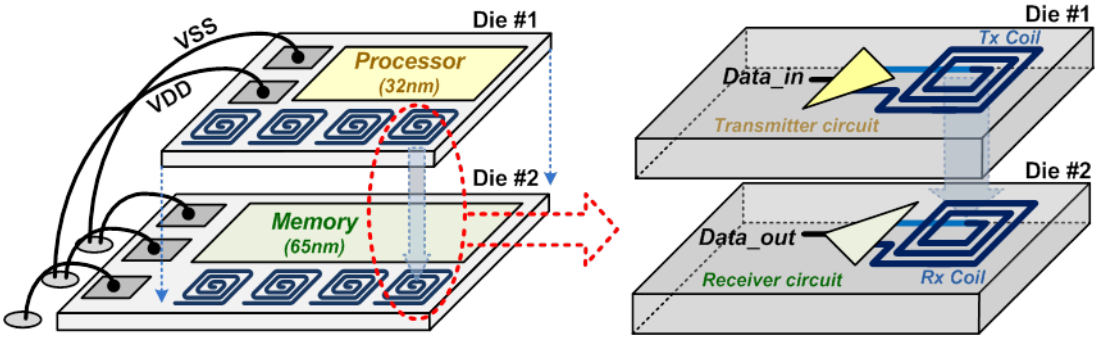


Fig. I.8. Concept of wireless inductive data link.

I.4.2 **Inductive Power Link**

One of the advantages of inductive coupling is that it can transfer power wirelessly. Previous work has reported wireless power transmission between two inductively coupled coils in stacked dies within a package [52][53]. However, their common drawbacks are only 100mW/mm^2 power density and <0.1 aspect ratio. This low performance is also because these designs rely on standard inductive coupling.

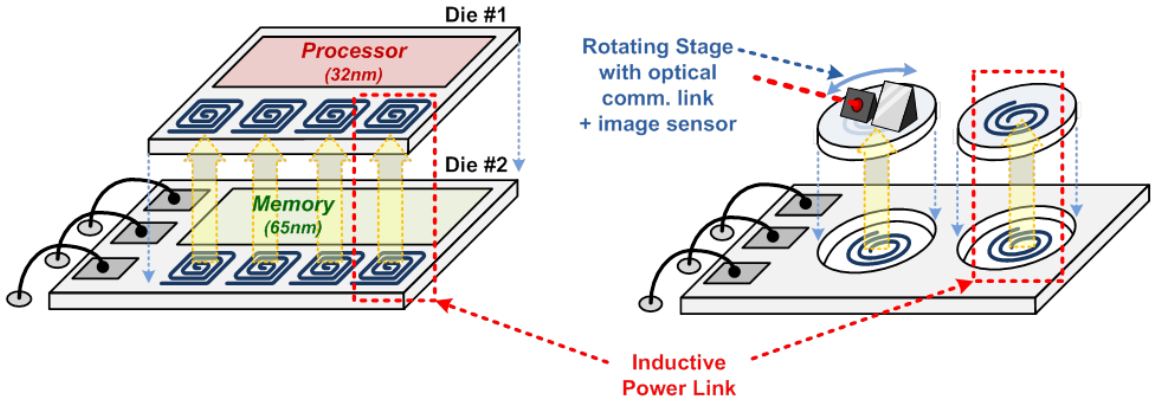


Fig. I.9. Concept of wireless inductive power link.

I.4.3 **Resonant Inductive Coupling**

This thesis studies the advantages of applying resonant inductive coupling (RIC) to 3DIC applications. RIC results in a stronger coupled coil pair and increases the linked flux by resonating coupled coils. RIC will be discussed for improving wireless interconnects between 3DICs to enhance the performance, and wireless power transfer to increase power density.

I.5 Contributions of This Work

This research seeks to provide circuit solutions to implement vertical interconnects for 3DICs. The most promising vertical interconnect methods are through silicon vias (TSVs) as a wired interconnect and inductively coupling as a wireless interconnect. While TSV implementation relies on semiconductor processing technology, circuit designers should be aware of the impact of TSVs on circuits. This work analyzes the effect of proximity of TSVs to FETs on the mobility and threshold voltage, which is a critical design consideration in 3DICs.

Most of this research focuses on the wireless interconnect method, a circuit-domain approach for 3DIC. TSVs are attractive for 3DIC interconnect, and commercial foundries provide both "via-first" and "via-last" technologies and are demonstrating heterogeneous 3D stacks. However, TSVs are not nearly as ubiquitous as the planar metallization layers in ICs have been for decades. Therefore, in processes that aren't amenable even to "via-last" TSVs, the wireless interconnect method between 3DICs using existing metal layers is a better option than reverting to traditional planar packaging. To resolve the disadvantages in previous work on wireless inductive links, this work achieves higher aspect ratio with lower power consumption, especially, in multiple stacked dies. This can be widely exploited in applications requiring multiple stacked layers such as NAND memory stacks and MEM systems comprised of heterogeneous stacks. It also could be utilized as shared vertical buses in 3D multi-core systems, which will be introduced in Appendix. B. The research includes channel characterization to find the best way to utilize an inductive coupling pair. In addition, circuit techniques are proposed to exploit

the inductive coupled channel. Prototypes of inductive data links and one inductive power link prototype will be demonstrated to verify the theory.

A summary of the contributions is as follows:

- Analysis and experimental verification of the proximity effect of TSVs on MOSFETs, which can be used as a design guide when placing circuits near TSVs (Chapter III)
- Characterization of resonant inductive coupling for inductive data links and power links in 3DICs to enhance the aspect ratio and extend the wireless range (Chapter II)
- Demonstration of three fabricated ICs leveraging resonant inductive coupling for data and power link applications (Chapter IV, V, VI)
- An LVS CAD tool for performing verification checks across multiple layers in a 3DIC using TSVs (Appendix A)

Chapter II.
Characterization of Wireless 3D Interconnect

II.1 Introduction

To create 3D interconnect, channel characterization has to be performed before implementing circuits. This chapter and the next chapter provide the channel characterization of the two most promising 3D interconnect methods. First, the inductive coupling wireless interconnect will be studied and characterized in this chapter. After studying the standard inductive coupling channel, a method to improve the inductive link by using resonant coupling will be proposed. Furthermore, this chapter will demonstrate that resonant coupling is more useful to multiple stacked layers when the phases of resonant coupled signals are aligned. In the next chapter, the proximity effect of through silicon vias (TSVs) near active devices will be characterized.

II.2 Inductive Coupling Channel

Fig. II.1 shows a diagram of a typical inductive coupling channel in two stacked dies and its equivalent circuit. Two coils are coupled with mutual inductance M. L_1, L_2 are the self-inductance of coils, assuming a symmetric transformer. The coils also have parasitic

capacitance C_1, C_2 and parasitic resistance R_1, R_2. The transmitter in die #1 can be simplified to a current source I_S, and R_L models the receiver in die #2. Usually the input impedance of the receiver is sufficiently large. Therefore, R_L is also a large resistance, which can typically be ignored in the equivalent circuit.

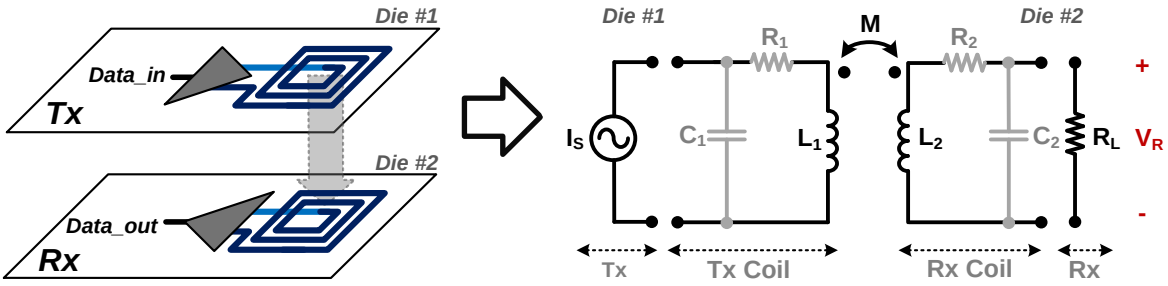


Fig. II.1. Diagram and equivalent circuit of inductive link.

From the equivalent circuit, the gain of the channel, V_R/I_T is given by:

$$\frac{V_R}{I_S} = \frac{1}{1 - j\omega R_1 C_1 + \omega^2 L_1 C_1} \cdot \frac{1}{1 - j\omega R_2 C_2 + \omega^2 L_2 C_2} \cdot j\omega M \qquad (1)$$

where M is mutual inductance between two coupled coils. Eq. (1) has three components. The first comes from the current divider of the transmitting coil, and the second term is from the voltage divider of the receiving coil. Both terms express second order low pass filters having peaks at their self-resonant frequencies. The mutual inductance is captured in the last term, which is linear in the frequency domain. Combining all terms induces a band pass filter having two peaks as shown as Fig. II.2. The frequency at which the peaks appear is a function of the self-inductance L and parasitic capacitance C. For the conventional inductive link, parasitic capacitance of coils is typically decreased in order

to maximize the self-resonant frequency of the coils because the data links operate at a frequency much lower than the self-resonant frequencies.

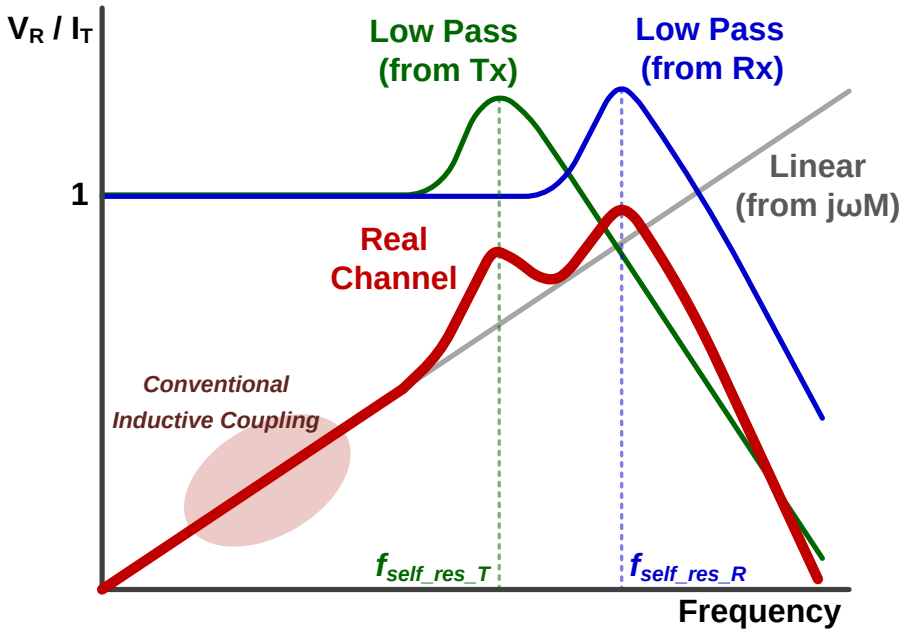


Fig. II.2. Frequency response of general inductive channel.

II.2.1 **Boundary of Near and Far-Fields**

Basically the standard inductive coupling channel is near-field communication. The near-field has a reactive characteristic, where the energy is stored, not radiated [54], and it makes near-field communication energy-efficient. In order to verify the theoretical maximum range of near-field communication, it is necessary to confirm the boundary of the near-field. The space around a radiation source or a transmitting antenna is generally divided into three regions depending on its communication properties as shown in Fig. II.3. The region where the $1/r^3$ term or $1/r^2$ is dominant is normally called the near-field region, and it is the combination of static field and induction field regions. However, the boundary between the near-field and far-field, or the point where the $1/r$ term begins to

be dominant is unclear because it is function of many other factors such as the antenna size and the radiation frequency. Table I shows numerous definitions of the boundary between near-field and far-field [55], where D is the largest dimension of the receiving antenna, and d means that of the transmitting antenna when the two antennae have different dimensions.

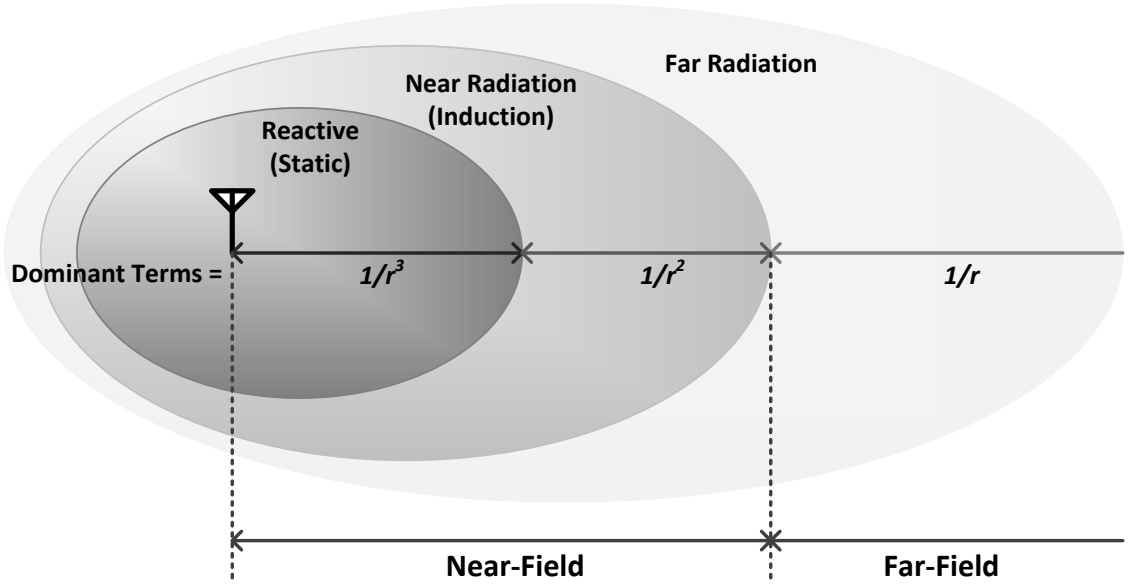


Fig. II.3. Three-region models around an electromagnetic source.

Table I. Definitions of the near-field/far-field boundary for antennas [55]

Boundary	Remarks	Reference
$\lambda/2\pi$	1/r terms dominant	[56]
3λ	D not >> λ	[57][58]
$\lambda/16$	Measurement error<0.1 dB	[56][57]
$\lambda/8$	Measurement error<0.3 dB	[56][57]
$\lambda/4$	Measurement error<1 dB	[56][57]

$\lambda/2\pi$	Satisfies the Rayleigh criteria	[59]
$\lambda/2\pi$	For antennas with $D<<\lambda$ and printed-wiring-board traces	[57][60]
$2D^2/\lambda$	For antennas with $D>>\lambda$	[57][60]
$2D^2/\lambda$	If transmitting antenna has less than 0.4D of the receiving antenna	[61]
$(d+D)^2/\lambda$	If $d>0.4D$	[61]
$4D^2/\lambda$	For high-accuracy antennas	[62]
$50D^2/\lambda$	For high-accuracy antennas	[62]
$3\lambda/16$	For dipoles	[57]
$(d+D)^2/\lambda$	If transmitting antenna is 10 times more powerful than receiving antenna, D	[58]

As described in the following chapters, the size of inductors or antennas used in this work is only tens of microns. Since the carrier frequency of the transceiver will be less than 10GHz, the inductor size should be much smaller than λ of the carrier wave (>>10mm). With this condition, the antenna size has little effect on the near-/far-field boundary, and a conservative approach from Table I implies the boundary should be smaller than $\lambda/2\pi$. The near-field boundary field depending on the operating frequency is shown in Fig. II.4.

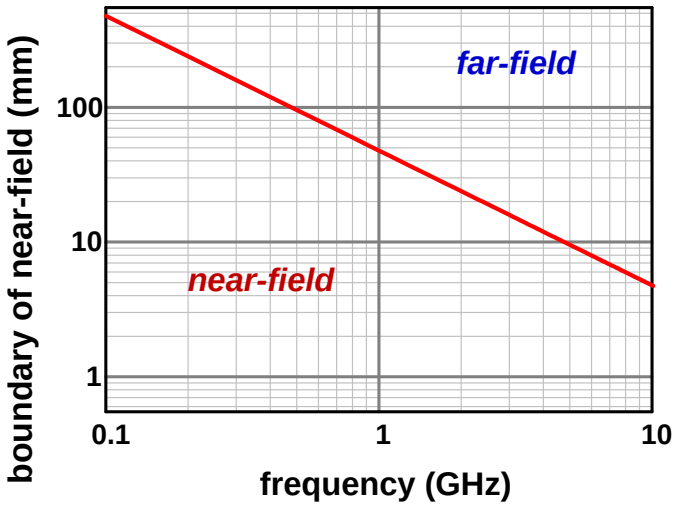


Fig. II.4. Boundary of near-field depending on the frequency.

II.2.2 **Coupling Coefficient *k***

Coupling coefficient *k* is a quantitative description of the coupled flux between a two-coil pair [63]. It plays the most critical role in inductive coupling since the receive signal amplitude highly depends on it. *k* is mainly a function of the coil size and the separation of two coils, and it is well known that *k* is inversely proportional to the separation. However, this is true only when the separation is sufficiently large, for instance, the separation is larger than the coil size. For closer separation, [43] provides an equation for a square-shaped coil pair as follows:

$$k = \left\{ \frac{0.0625\left(d_{out\_T} + d_{in\_T}\right)\left(d_{out\_R} + d_{in\_R}\right)}{X^2 + 0.0625\left(d_{out\_R} + d_{in\_R}\right)^2} \right\}^{1.5} \tag{2}$$

where d_{out_T} and d_{out_R} refer to the outer diameter of the inductors, and d_{in_T} and d_{in_R} indicates the inner diameter. X is the distance between two inductors when their center is vertically aligned. While this equation is based on an empirical approximation, [44] and

[45] provide more theoretically accurate expressions of mutual inductance M for a circular coil pair as follows:

$$M(a,b,p,d)$$

$$= \pi\mu_0\sqrt{ab}\int_0^\infty J_1\left(x\sqrt{\frac{a}{b}}\right)J_1\left(x\sqrt{\frac{b}{a}}\right)J_0\left(x\frac{p}{\sqrt{ab}}\right)exp\left(-x\frac{d}{\sqrt{ab}}\right)dx$$

$$= \pi\mu_0 a\int_0^\infty J_1(x)J_1(x)exp\left(-x\frac{d}{a}\right)dx \qquad \text{where } \pi\mu_0 a = b \text{ and } p = 0 \quad (3)$$

where a and b are the diameters of each coil, p is the horizontal separation (=misalignment), and d is the vertical separation.

Fig. II.5 shows the theoretical value of the two equations, simulated data, and measured data. The vertical offset is mainly due to inductor shape (square, circle, and octagon). Commonly, the coupling coefficient k decreases rapidly when the normalized distance (coil size / distance) is larger than 1. This means k is too small to achieve near-field communication when the communication range becomes larger than the coil diameter. Therefore, the conventional inductive coupling methods are feasible for only a relative short range. Otherwise, larger coils are required to achieve longer distance. In other words, the small aspect ratio (communication distance / coil diameter) is inevitable when using standard inductive coupling.

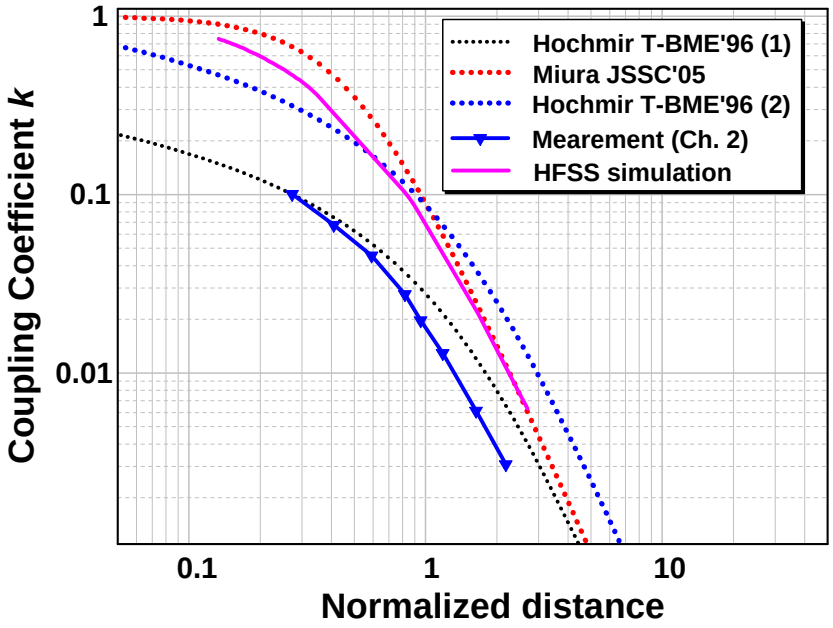


Fig. II.5. Coupling coefficient versus normalized distance.

II.3 Resonant Inductive Coupling

As discussed in Chapter 1, previously demonstrated inductive data links have resulted in a relatively short communication rage due to the small amount of linked magnetic flux between the coupled coil pair [46]-[64]. It has recently been shown that power can be wirelessly transferred using two resonant inductors for powering consumer electronics at relatively long distances, with an efficiency of up to 50% [65]. This technique, termed resonant inductive coupling (RIC), makes a stronger coupled coil pair and increases linked flux by resonating coupled coils. RIC can be used for wireless interconnects between 3DICs and to enhance the performance.

II.3.1 **Theoretical Analysis**

Because the flux density, and therefore signal strength, in inductive links is directly proportional to current in the transmitting coil, the transmitter circuits should maximize current in order to maximize transmission distance. On the receiver side, an amplifier optimized for low noise figure and power presents a high-impedance load on the receiver coil, therefore received voltage should ideally be maximized. Standard inductive coupling (SIC) links operate well below the self-resonant frequency of the inductors, therefore typically all parasitic capacitances are ignored and the SIC link is modeled as the equivalent circuit in Fig. II.6(a). R_1 and R_2 model the losses in the coils. The transmitter is modeled as a current source operating at a fixed frequency. The receiver is modeled as a large resister R_L. The received voltage V_R for the SIC link is given by Eq. (4)

$$V_{R\_SIC} = j\omega k\sqrt{L_1 L_2} I_S = j\omega k L I_S \tag{4}$$

where k is the transformer coupling coefficient, L_1 and L_2 are the self-inductances of the transmitter and receiver coils, respectively. Since the transmitter and receiver coils are typically identical for SIC and RIC links, $L_1 = L_2 = L$. I_S is the transmitter current amplitude. The value of k is found from simulations, and is a strong function of the separation between coils ($k \propto \text{distance}^{-3}$), therefore its value determines the communication distance.

The RIC circuit is shown in Fig. II.6(b). External capacitors C_1 and C_2 have been added to create resonant tanks at the transmitter and receiver sides. The resonant frequency can be tuned by adjusting the capacitor values. RIC links operate in two

regimes, depending on the values of k and quality factor of the resonant tank ($Q = \omega L/R$), where R is the loss in the inductor. These regimes are 1) the strongly coupled regime ($kQ \geq 0.1$), and 2) the weakly coupled regime ($kQ < 0.1$). The link characteristics are different in each regime, as discussed in the following two sections.

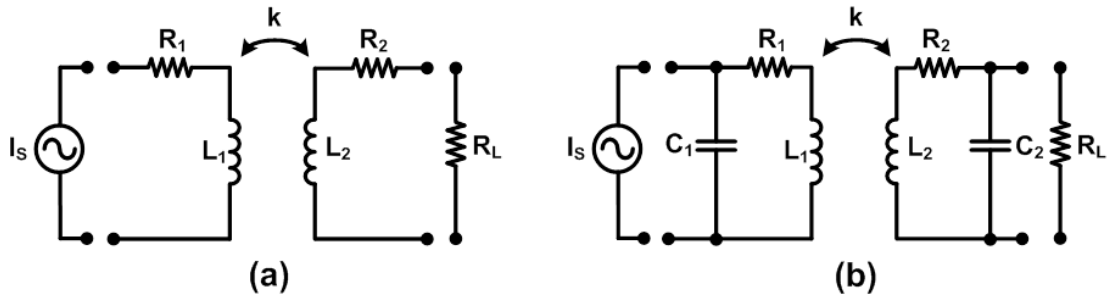


Fig. II.6. (a) SIC equivalent circuit and (b) RIC equivalent circuit

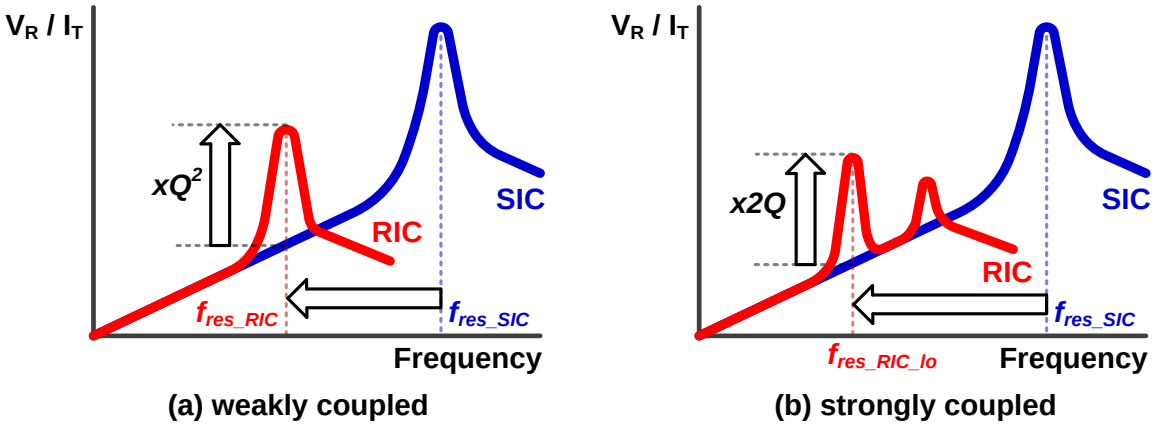


Fig. II.7. Frequency response of RIC.

The strongly-coupled regime is defined by $kQ \geq 0.1$, that is, when the coils are close together. In this regime, the coupling is strong enough that the loading on the receiver side affects the resonant frequency at the transmitter side when reflected through the transformer, and vice versa. Therefore, the transimpedance gain can be expressed by

$$\frac{V_R}{I_S} = \frac{1}{1 - j\omega R_1 C_1 + \omega^2 L_1 C_1 - \frac{\omega^4 M^2 C_1 C_2}{1 - j\omega R_2 C_2 + \omega^2 L_2 C_2}} \cdot \frac{1}{1 - j\omega R_2 C_2 + \omega^2 L_2 C_2} \cdot j\omega M \quad (5)$$

This creates two resonant frequencies for the strongly-coupled RIC system, given by:

$$\omega_{0\_low} = \frac{\omega_0}{\sqrt{1+k}} = 2\pi f_{res\_RIC\_lo} \quad (6)$$

$$\omega_{0\_hi} = \frac{\omega_0}{\sqrt{1-k}} = 2\pi f_{res\_RIC\_hi} \quad (7)$$

where $\omega_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = 2\pi f_{res\_RIC}$ is the unloaded resonant frequency. At each resonant frequency, the received voltage V_R for RIC with strong coupling is given by:

$$V_{R\_RIC\_low} = jQ^2 \left(\frac{1+k}{1+kQ}\right) \omega_{0\_low} k L I_S \quad (8)$$

$$V_{R\_RIC\_hi} = jQ^2 \left(\frac{1-k}{1+kQ}\right) \omega_{0\_hi} k L I_S \quad (9)$$

When *k* approaches 1, the advantage of RIC over SIC (Eq. 4) is an increase in received voltage by a factor of approximately $2Q$. As the coil separation increases, k reduces, and ω_{0_low} and ω_{0_hi} converge on a single resonant frequency ω_0. The RIC link then transitions from the strongly-coupled regime into the weakly-coupled regime as described below.

The weakly-coupled regime is defined by $kQ < 0.1$; that is, when the coils are far apart. In this regime, the receiver load reflected to the transmitter side is negligibly small so that it has no impact on the transmitter circuit. Therefore, its transfer function is given

by the similar equation to Eq. (1), and the system has one resonance frequency $\omega_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2}$. At ω_0, the receiver voltage V_R is given by Eq. (10).

$$V_{R\_RIC} = jQ_1Q_2\omega_0 k\sqrt{L_1L_2}I_S = jQ^2\omega_0 kLI_S \tag{10}$$

In this regime, RIC significantly improves the received signal amplitude over SIC (Eq. 1) by a factor of Q^2, which is typically much greater than 1.

II.3.2 **Simulations**

To verify these models, planar spiral coils were designed for SIC and RIC using a Chartered 130nm CMOS process (Fig. II.8). Two identical coils are vertically stacked to simulate communicating through stacked ICs. The distance between them is swept from 5μm to 95μm, and HFSS is used to extract the lumped-element models for the coils. These models are imported into Spectre to simulate the received voltage for a given transmitter current excitation. The results are shown in Fig. II.9 and Fig. II.10. The nominal value of Q is 3.1, and the boundary of the weakly/strongly coupled regimes is k = 0.03. In the weakly coupled regime, the RIC link has one resonant frequency, but as k increases, the frequency splits into ω_{0_hi} and ω_{0_low} (Fig. II.9). Fig. II.10 shows V_{R_SIC}, V_{R_RIC} at ω_{0_low}, and the ratio of the two. RIC improves the coupling over SIC by a factor of 10 ($\approx Q^2$) in the weakly-coupled regime, and 5~10 ($\approx 2Q$) in the strongly-coupled regime. As k increases, the stronger coupling increases V_{R_RIC}. However, the ratio V_{R_RIC}/V_{R_SIC} will decrease as the coupling gets stronger, approaching $2Q$ for $k = 1$, and further decreases with reducing Q as frequency ω_{0_low} decreases.

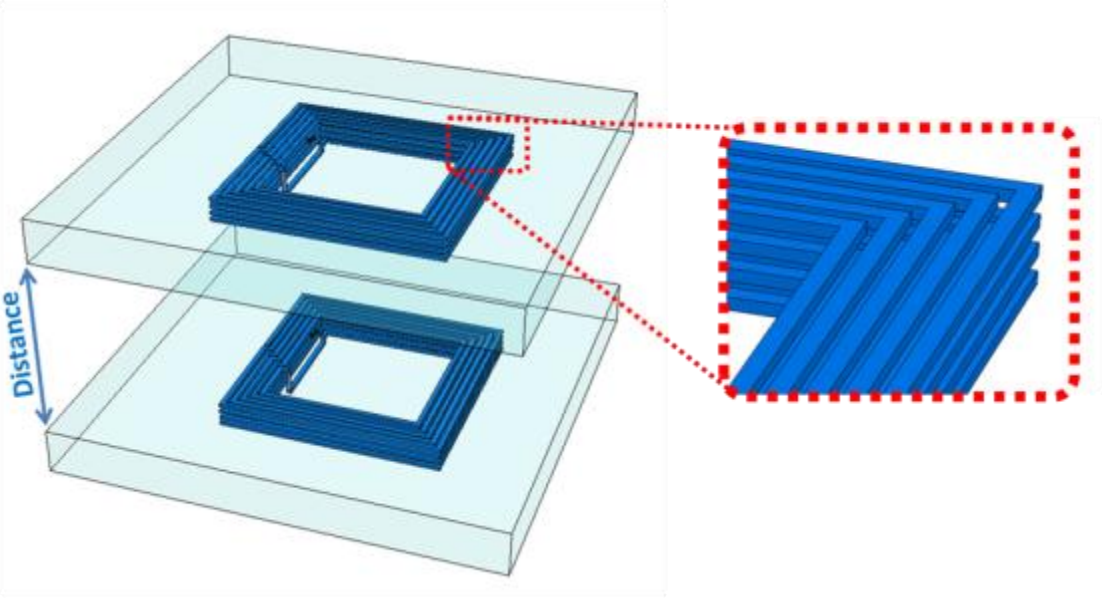


Fig. II.8. Coupled coil pair structure for HFSS.

Table II. Details of coils

Parameter	Value
Diameter	30μm
Width	0.65μm
Space	0.35μm
Number of turns	5
Number of layers	4
L	22nH
C	40fF
R	240Ω

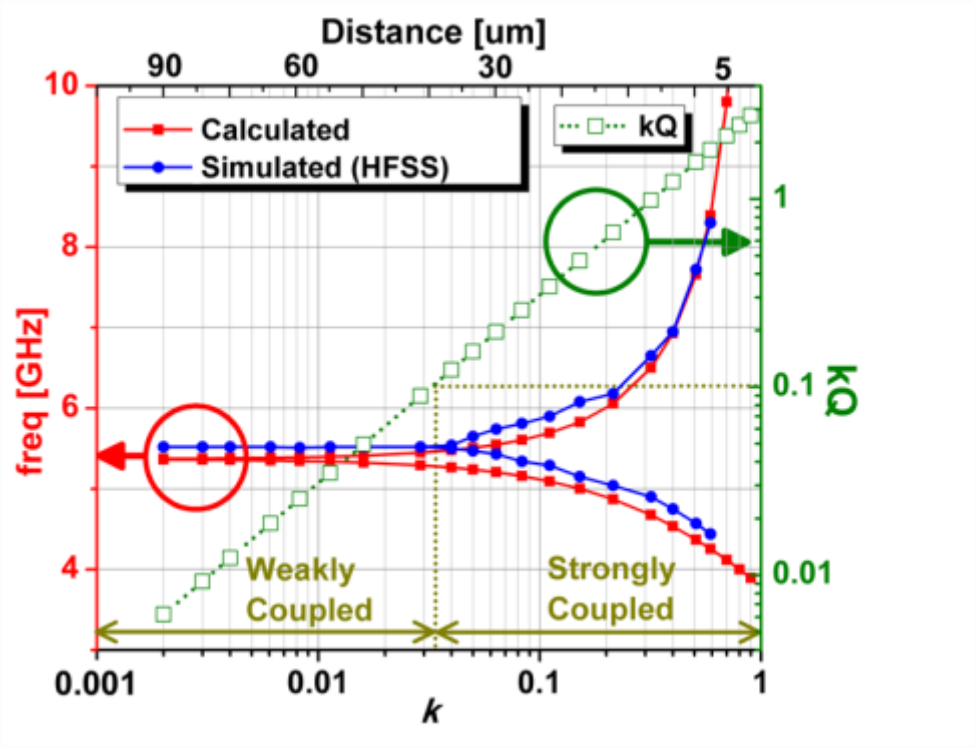


Fig. II.9. RIC resonant frequency.

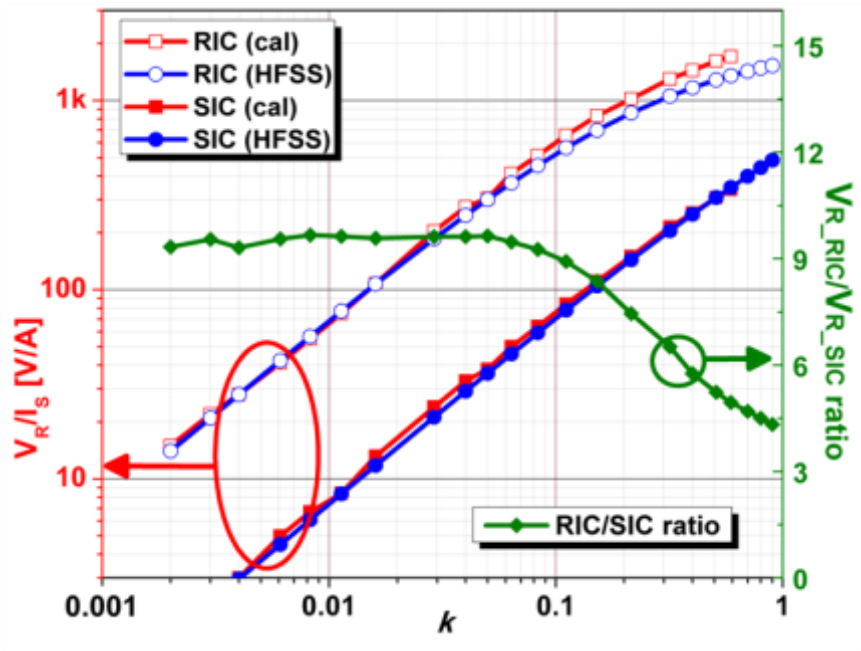


Fig. II.10. RIC improvement over SIC.

The performance of inductive links for 3D wireless interconnects in a package can be improved by using resonant inductive coupling over standard inductive coupling. Without increasing the size of the coils or power consumption, RIC can increase the received voltage by factors of Q^2 (weakly coupled) and $2Q$ (strongly coupled) compared to SIC. The improvement of RIC is the highest in the weakly-coupled regime when the received signal is smallest. Therefore, RIC can be exploited for small k to increase the communication distance and separation between coils, enabling communication through thicker die or multiple die, as well as wireless testing and verification.

II.4 In-phase Resonant Inductive Coupling for Multiple Stacked Dies

Inductive coupling is one technique used to create through-die-interconnect between multiple stacked layers as depicted in Fig. II.11. In this application, the aspect ratio (communication distance / coil diameter) limits the area-efficiency of the link, and the number of layers that can be communicated through.

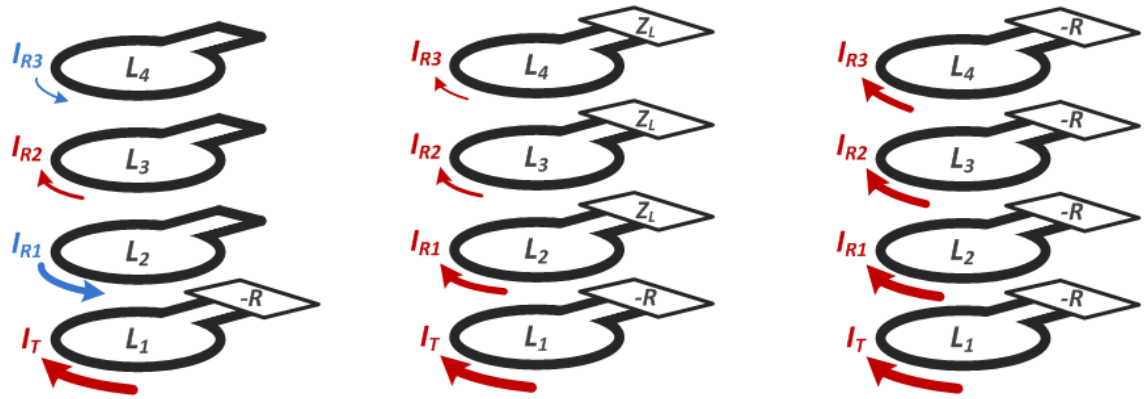
Fig. II.11. Concept of wireless through-die-interconnect in 3DIC.

Since *k* decreases rapidly for aspect ratios larger than 1 as shown in Fig. II.5, conventional wireless inductive data links usually have aspect ratios less than 1. For this reason, prior inductive links for multiple die stacking send data only to the adjacent layer, and relay data to communicate through multiple dies [46][66]. This relay method takes a number of cycles to transmit data to the destination. While direct communication through multiple-stacked dies resolves this latency problem [67][68], prior work uses large coils to do so due to the limited aspect ratio.

This work analyzes a technique termed multi-layer signal boosting (MLSB) intended for inductive data links in 3DIC applications. By exploiting resonant inductive coupling, it enables a larger aspect ratio, which means direct transmission through multiple dies with relatively small coils.

II.4.1 **Theoretical Analysis**

Consider four vertically stacked planar coils as shown in Fig. II.12. When an AC current is applied in the bottom coil, it induces out-of-phase AC current in the second and fourth coils and in-phase AC current in the third coil when the coil terminals are all shorted, according to Faraday's law of induction (Fig. II.12(a)). If the coils are instead loaded by a large impedance, an AC current close to in-phase is induced in all coils (Fig. II.12 (b)). As shown in Fig. II.12 (c), if regeneration is added to the coils, the magnitude of the induced current is amplified. This roughly explains the operation of MLSB.



(a) **(b)** **(c)**

Fig. II.12. Concept of multi-layer signal boosting.

The two major elements of MLSB are the in-phase strongly-coupled resonant inductive coupling (RIC) and the regeneration of the oscillations. RIC provides signal gain depending on the product of *kQ* of the inductors as discussed previously, and this chapter shows that the phase difference is affected by the *kQ* value as well.

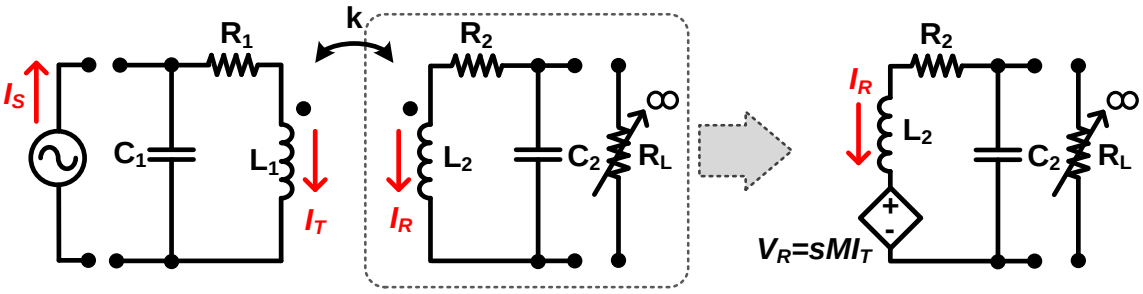


Fig. II.13. Equivalent circuit of inductively coupled circuits.

Fig. II.13 shows the equivalent circuit of an inductively coupled data link across two layers. The transmitter is simplified to current source I_S, and R_L is a model of the receiver circuits loading the coils. Because R_L is generally large for data links, it can be ignored to simplify the circuit. It results in the following equation according to Kirchhoff's voltage law (KVL).

$$\left(sL + R + \frac{1}{sC}\right) \cdot I_R + sMI_T = 0 \tag{11}$$

Eq. (11) is modified to present current gain across the coils:

$$\frac{I_R}{I_T} = -\frac{sM}{sL + R + \frac{1}{sC}} = \frac{\omega^2 MC}{1 + j\omega RC - \omega^2 LC} \tag{12}$$

By inserting three different resonant frequencies of strongly-coupled and weakly-coupled RIC systems into Eq. (12), the ratio is concisely written as follows.

$$\left(\frac{I_R}{I_T}\right)_{Strongly\ Coupled\ RIC, low\ res.freq.} = \frac{kQ}{kQ + j} \tag{13}$$

$$\left(\frac{I_R}{I_T}\right)_{Strongly\ Coupled\ RIC, high\ res.freq.} = \frac{-kQ}{kQ - j} \tag{14}$$

$$\left(\frac{I_R}{I_T}\right)_{Weakly\ Coupled\ RIC} = -jkQ \tag{15}$$

Eq. (13) is for low frequency and strongly-coupled RIC, Eq. (14) is for high frequency and strongly-coupled RIC, and Eq. (15) is for weakly-coupled RIC, respectively. In the weakly coupled regime, the magnitude of the induced current is proportional to the *kQ* value. And the phase difference between inducing and induced currents is always -90°, regardless of the *kQ* value. In the strongly-coupled regime, however, the phase difference between I_R and I_T is a function of *kQ* as shown as Fig. II.14. When *kQ* is small (the boundary of strongly- coupled and weakly-coupled), the phase difference is almost -90°

for both cases of low and high resonant frequency. As the *kQ* value increases, the phase at the lower resonant frequency converges to 0^0 (in-phase) and at the higher frequency converges to 180^0 (out-of-phase). The amplitude of the induced current is increasing as the *kQ* value increases for both cases. By operating the link at the lower resonant frequency and in the strongly-coupled regime, the induced current has a similar phase to the inducing current. The weakly-coupled regime can be exploited as well, but improvement is smaller compared to the strong-coupled RIC due to the large phase difference.

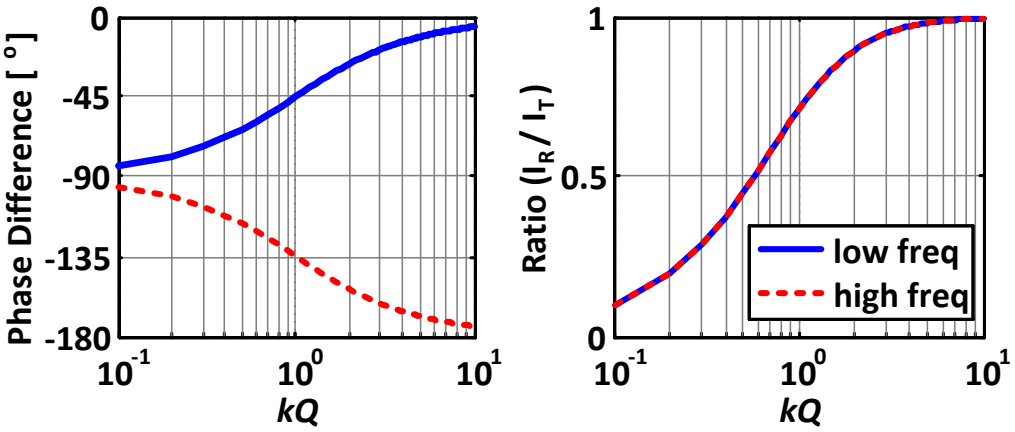


Fig. II.14. Phase difference between I_R and I_T and magnitude ratio.

The larger *kQ* value results in a smaller phase difference and a larger induced current. In practice, it is difficult to increase *kQ* because *k* is limited by the coil size and die thickness, and an on-chip inductor has a relatively small *Q*-factor. Furthermore, larger *Q* will reduce the data-rate of the inductive coupling using RIC as explained in Chapter 4. Because of the *kQ* limitation, in-phase RIC cannot increase the induced current amount significantly by itself.

Another main element of MLSB, regenerative oscillation, is able to amplify the current amount in company with in-phase RIC. The regenerative oscillator has a feedback whose loop gain is slightly less than one as shown in Fig. II.15 [70]. When the induced signal is applied to a regenerative oscillator, it triggers sustained oscillations and amplifies the induced in-phase current. Since this oscillation is in phase with original transmitter current, they sum to induce a stronger signal in the next layer. This process then repeats at each layer.

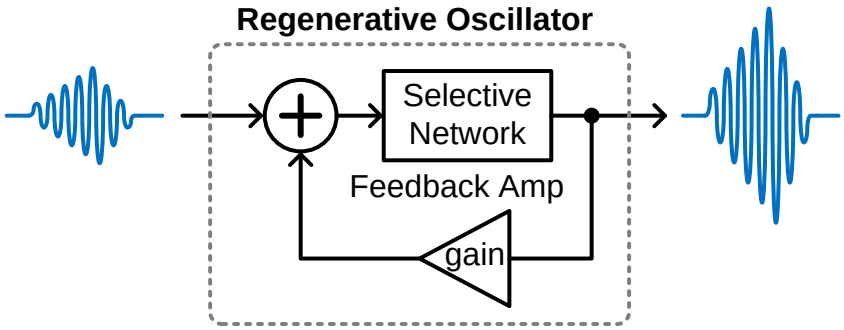


Fig. II.15. Diagram of regenerative oscillator.

In the MLSB scheme, in-phase RIC provides the proper input signals into the regenerative oscillation as depicted in Fig. II.15. For the worst-case example, the coil at layer 3 has two different components of induced current. $I_{3\text{-}by\text{-}1}$ is induced by I_T, and $I_{3\text{-}by\text{-}2}$ is induced by I_2. Because all of I_T, I_2, $I_{3\text{-}by\text{-}1}$, and $I_{3\text{-}by\text{-}2}$ have similar phase, the vector summation of $I_{3\text{-}by\text{-}1}$ and $I_{3\text{-}by\text{-}2}$ results in a significantly larger current, $I_{3\text{-}total}$. This induced current is large enough to be amplified in a regenerative oscillator, resulting in amplified current I_3.

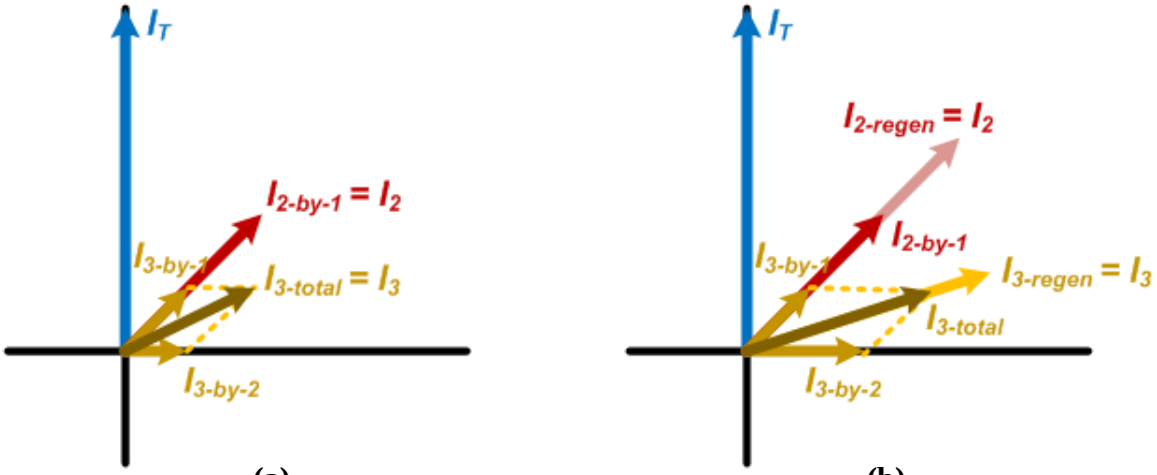


Fig. II.16. Vectors of boosted current signals on multiple layers. (a) without regeneration (b) with regeneration

While super-regenerative oscillating provides larger gain and higher sensitivity, it requires complicated control signals compared to regenerative oscillating [71][72]. Because it is hard to generate analog signals for the control of 1Gbps processing, regenerative oscillating is adopted in spite of its disadvantages.

II.4.2 **Measurement Results**

To verify the theory, a prototype system is designed with a planar coil on PCB and discrete components to implement the regeneration.

The coil on each PCB has an octagon shape, is a single turn, and has a 23mm diameter. Each PCB layer has a cross-coupled oscillator for regeneration, using discrete FETs, a bias current of 30mA, and a supply voltage of 3V. Four layers are stacked as shown in Fig. II.17, and the separation between layers is changed to sweep k from 0.01 to 0.1. Since the coil Q-factor is 20, the links operate in the strongly coupled regime. The resonant frequency of the system is tuned to 75MHz.

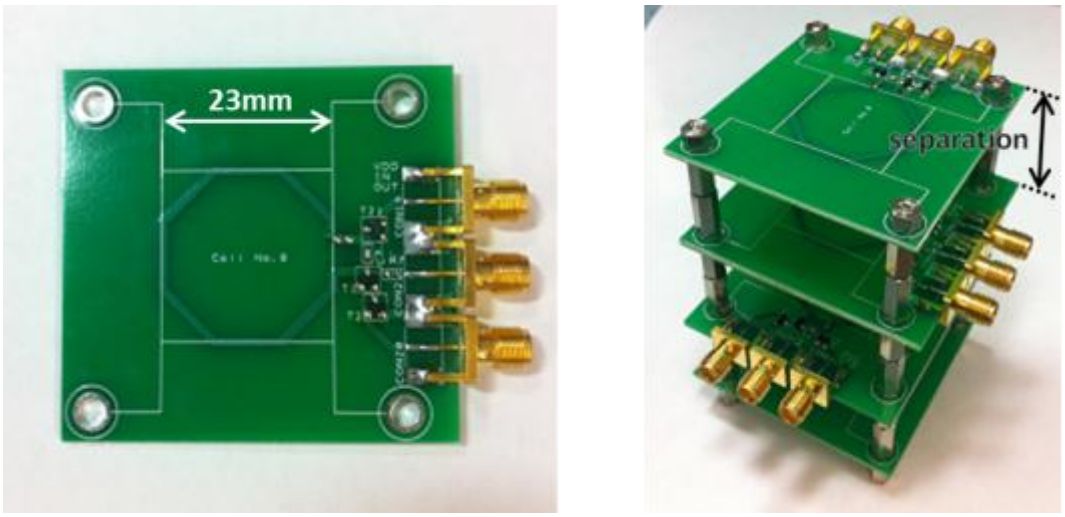


Fig. II.17. A prototype system on PCB for MLSB.

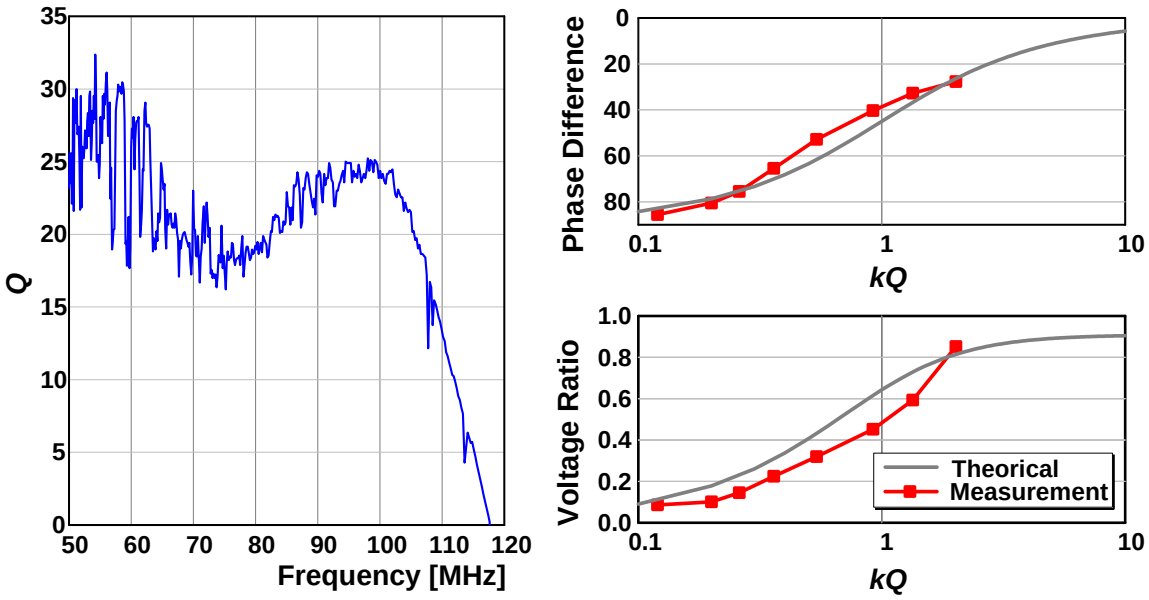


Fig. II.18. Measured Q and comparison of phase and magnitude to theory.

Fig. II.19 shows signal transmission from layer 1 to layer 4 with 23mm separation per layer. The source signal at layer 1 and the induced signal at layers 2-4 are almost in-phase, with the phase difference ranges from 0° to 24°. The comparison between MLSB, RIC without regeneration and standard inductive coupling (SIC) is shown in Fig. II.20. As the

separation increases, the SIC signals reduce, eventually becoming too small to sense. RIC alone induces larger signals than SIC, but fails to deliver sufficient signals to layers 3 and 4 when the distance is long. However, if regeneration is used with RIC, communication distance is significantly enhanced. When the aspect ratio is 4:1 (the separation = 31mm), the received signal at layer 4 is 9.8dB larger than RIC-only and 16.2dB larger than SIC.

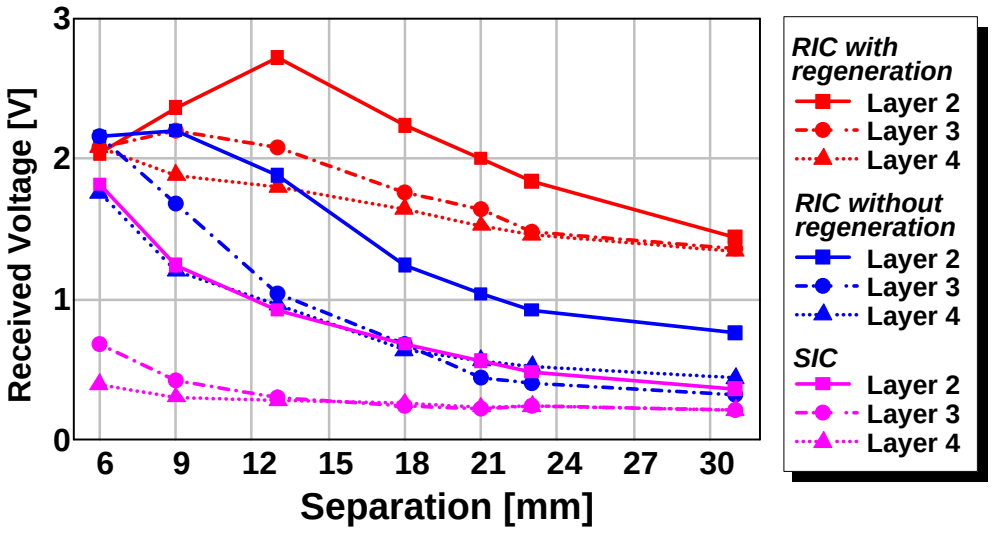


Fig. II.19. Measurement received voltage of MLSB, RIC-only, and SIC.

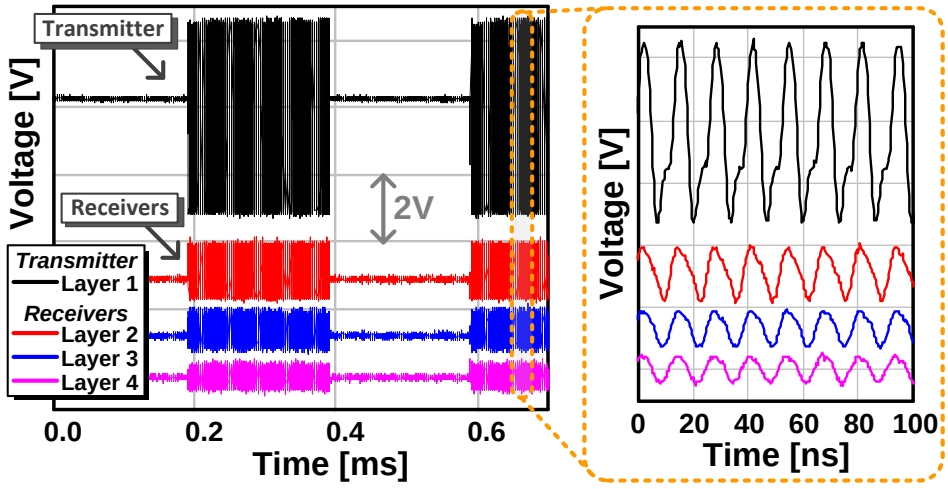


Fig. II.20. Measured waveform of MLSB when separation = 23mm.

Chapter III.
Characterization of Wired 3D Interconnect

III.1 Introduction

As discussed in the previous chapter, the most promising method among 3D interconnects is through-silicon-vias (TSVs). To fabricate high aspect ratio vias within a silicon substrate and achieve high yield have been huge challenges for CMOS technology [73]. In addition, while TSV technology provides new opportunities for circuit designers, it requires new considerations during the circuit design. They should be aware of not only the electrical performance of TSVs such as the parasitic capacitance, resistance, and inductance, but also the performance change of active devices due to their proximity to TSVs.

There have been concerns that the proximity of a TSV to a device such as a transistor can impact its electrical performance, and previous research has reported the proximity effect of TSVs on devices [74]-[77]. TSV processes have multiple categories defined by their processing steps, including via-first, via-last, and via-middle. Furthermore, different materials can be used for TSVs such as copper, tungsten, and poly silicon. This diversity produces varied results of the impact of TSVs on other devices, and experimental research for other cases is required.

This work presents a study of the proximity effect for via-middle Tungsten-filled cylinder-shape TSVs using a process from Tezzaron [78]. A 2-layer stacked test structure with TSVs was fabricated with a 130nm CMOS process in order to evaluate the proximity effect of TSVs on MOSFETs. The key parameters of different-sized PMOS and NMOS devices were measured to characterize the impact of TSV proximity and provide guidelines for design with the specified TSVs.

III.2 Test Structure for Characterizing Proximity Effect

The TSVs in this work are fabricated by a via-middle process [78]. After front-end of line (FEOL) processing, TSV holes are etched and W is deposited into SiO_2 lined holes. Once a wafer is completed including backend of line (BEOL) processing, two wafers are stacked face-to-face using Cu-metal micro-pads bonding. To implement vertical interconnect to other wafer or wirebonding pads, the top die is thinned to expose the TSVs.

Active devices and TSVs for characterization are implemented on the top layer. Probe pads to access the devices are made on the thinned backside of top die and connected to metal layers inside of top die with multiple TSVs. The channels of all devices are placed in the vertical direction in Fig. III.1. The TSV is a cylindrical shape with almost a 90° slope. Its diameter is 1.2μm, and the height is 6μm after the wafer thinning process. This work was fabricated with the Chartered 130nm CMOS process and Tezzaron TSV technology.

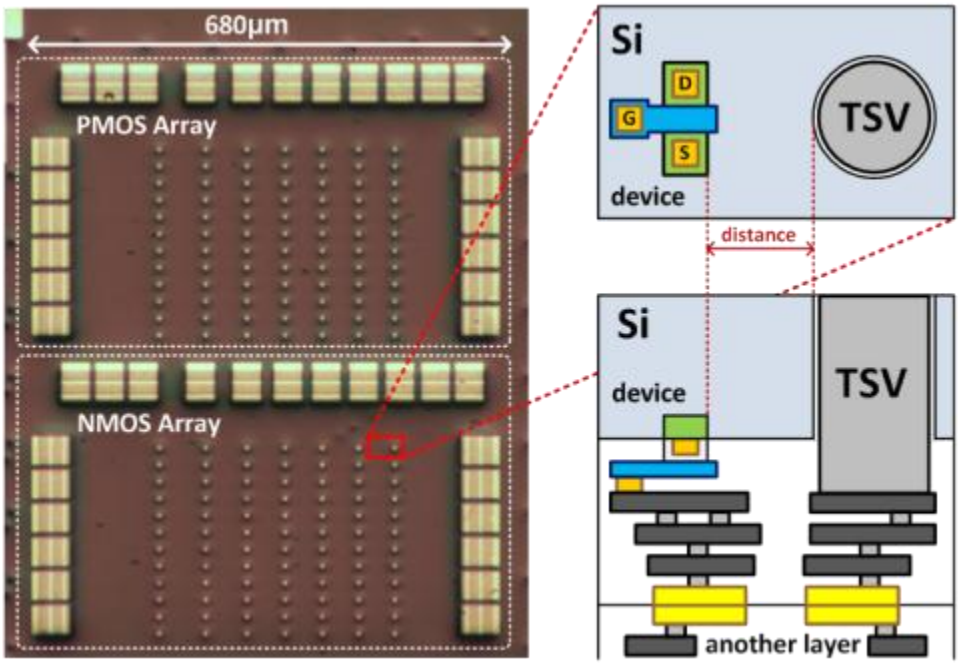


Fig. III.1. Die-photo of the test structure and schematic of one cell which consists of one MOSFET and one TSV. (top view and cross-sectional view)

The fabricated test structure has two arrays for PMOS and NMOS devices as shown in Fig. III.1, and its schematic is shown in Fig. III.2. Each array has 12 rows and 9 columns. Every column corresponds to one of 8 distances between a TSV and a device that range from 0.7μm to 50μm. The array also includes control cases without TSVs. Each row represents one among 12 combinations of the channel width from 300nm to 1200nm and the channel length from 130nm to 1040nm. It has a total 216 combinations. One column has 12 different sized MOSFETs, and they share one DC probe pad connected to gates of the MOSFETs. One row has 9 equal-sized MOSFETs sharing one DC probe pad connected to the drains of the MOSFETs. The source and body terminals of all MOSFETs are connected to a shared DC probe. Other peripheral circuits, for instance, a scan chain, mux, or ADC, are not implemented to allow more accurate measurements of the device performance.

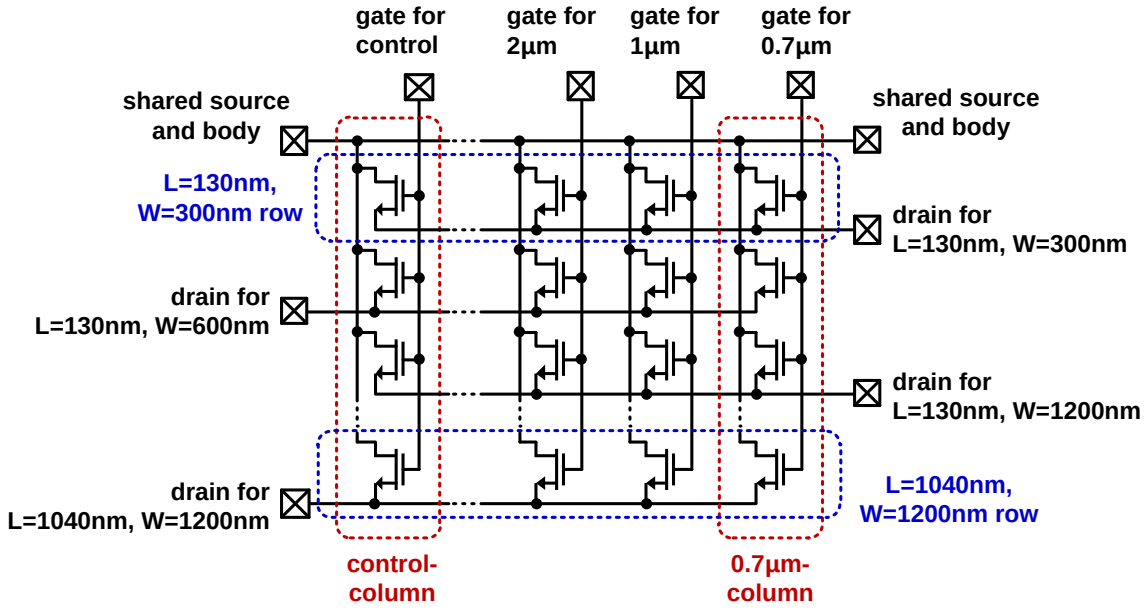


Fig. III.2. Schematic of the test structure (one array).

III.3 Measurement Results

In order to characterize each device, its V_{TH} and mobility was calculated from the I_{DS}-V_{GS} curve, which was measured with an Agilent 4156C semiconductor parameter analyzer and DC probes as shown in Fig. III.3. V_{GS} is swept from 0V to 1.5V with 15mV steps for V_{DS}=10mV (linear region) and V_{DS}=1.5V (saturation region) respectively. Both of V_{TH} and the mobility are extracted by the maximum g_m method [79] and the normalized mobilities from the control case value are used.

Fig. III.4 shows the V_{TH} shift observed in the devices. In both NMOS and PMOS devices, the V_{TH} shift is unnoticeable. Fig. III.5 shows the observed mobility change. While electron mobility change is not observed, hole mobility increases significantly as

the distance between the PMOS device an TSV reduces below 4µm. Different widths and lengths of the devices make no noticeable difference in V_{TH} shift or mobility change.

(a) (b)

Fig. III.3. Measurement setup. (a) light shielded probe station (b) Agilent 4156C parameter analyzer

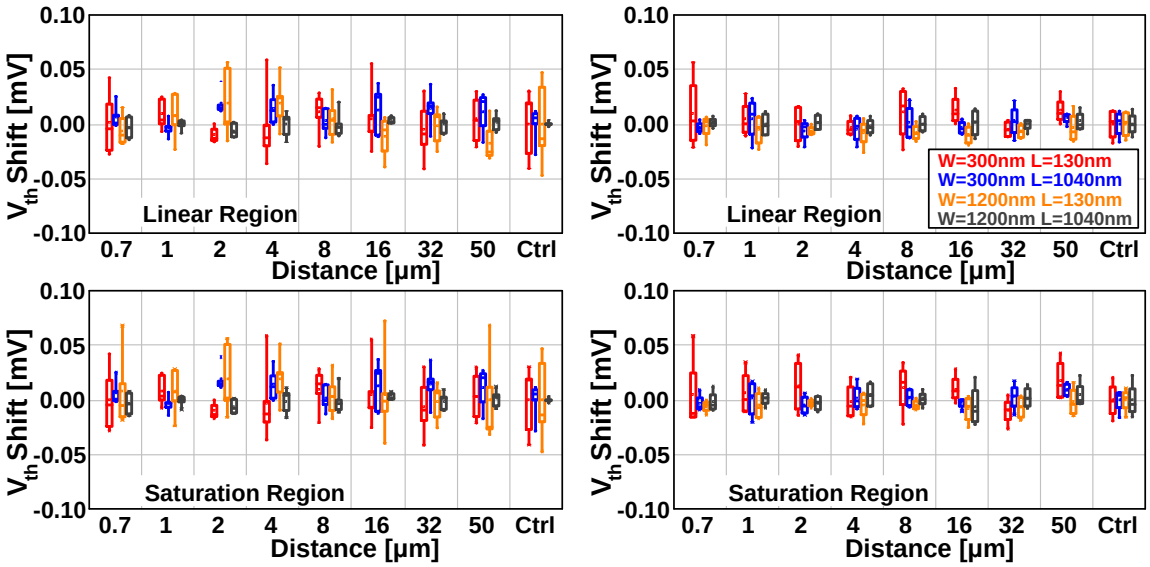


Fig. III.4. V_{th} shift of NMOS (left) and PMOS (right).

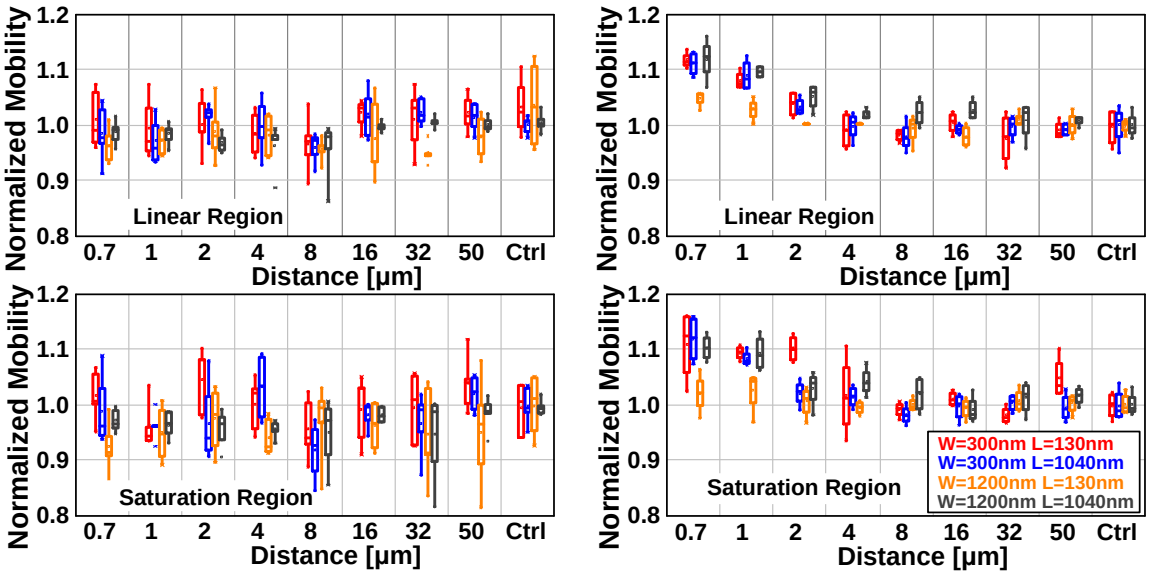


Fig. III.5. Mobility change in NMOS (left) and in PMOS (right).

III.4 Analysis

Mobility changes are most likely due to the mismatch in the coefficient of thermal expansion (CTE) between Silicon and Tungsten. The CTE of Silicon (Si: 2.7ppm/°C) is smaller than that of Tungsten (W: 4.3ppm/°C) as shown in Table III, which adds strain to the Si surrounding the TSV as the wafer cools after fabrication [80]. W is deposited at ~400°C and has a larger CTE than Si. At room temperature, the W shrinks more than the surrounding Si, which causes compressive stress σ_θ in the tangential direction to the TSV, tensile stress σ_r in the radial direction to the TSV, and compressive stress σ_z in the vertical direction as shown in Fig. III.6.

Table III. CTE of Materials

Material	CTE (ppm/K)	
Si	2.7	0°C
	3.3	270°C
	4.4	400°C
SiO_2	0.55	
W	4.3	
Cu	16.7	

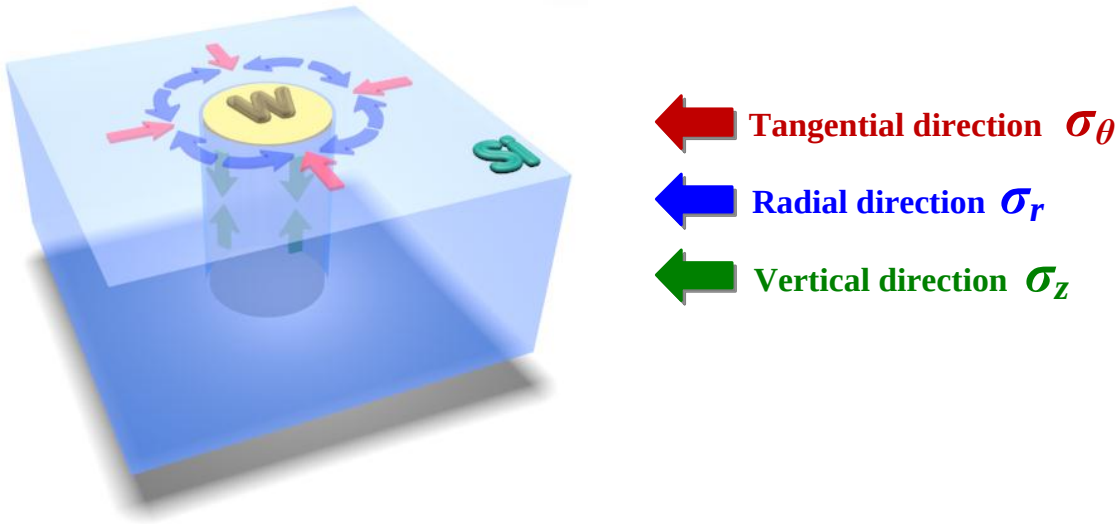


Fig. III.6. Stress direction due to CTE mismatch.

According to the piezoresistance model, the hole and electron mobility change due to stress direction and strength is shown at Fig. III.7 [81]. The impact of these stresses depends on the orientation of the devices. While device channels drawn in the radial direction will suffer from compressive longitudinal stress and transverse tensile stress, devices with channels drawn in the tangential direction will suffer from tangential stress and longitudinal compressive stress. Therefore, device channels in the radial and

tangential direction will suffer from opposite directions of stress in the (100) plane (σ_{xx}, σ_{yy}) and common stress in the [100] direction (σ_{zz}) as shown in Fig. III.8.[1]

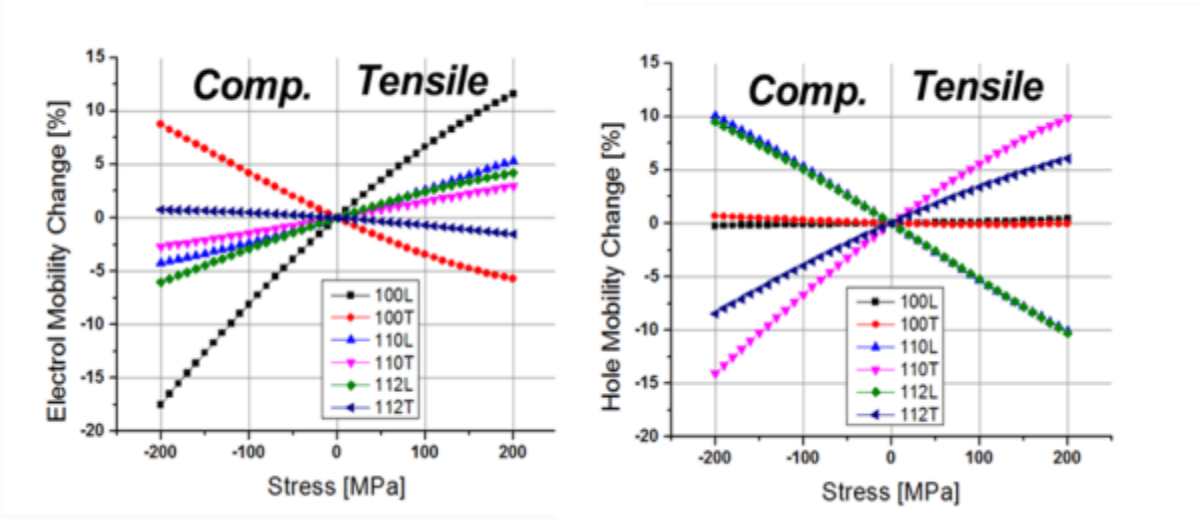


Fig. III.7. Impact of stress to mobility change.

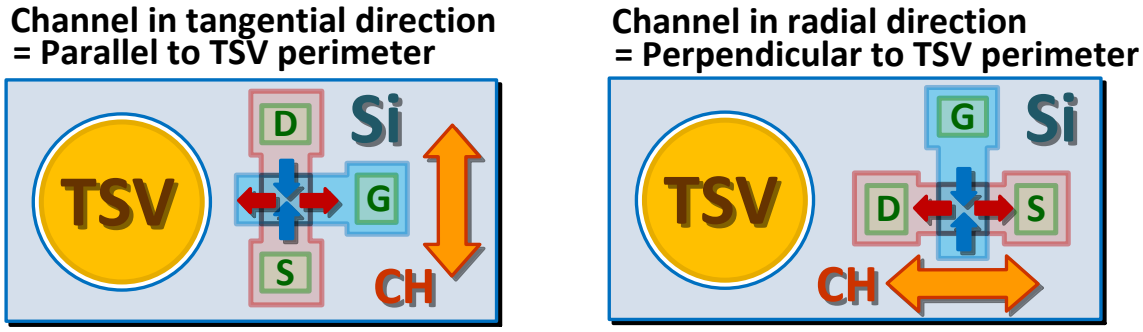


Fig. III.8. Stress direction due to CTE mismatch.

III.5 Modeling the Proximity Effect

To verify this, 3D finite element method (FEM) modeling is performed. The commercial FEM tool COMSOL can be utilize to characterize the thermal stress around a

[1] Miller index notation for cubic crystals. With three integers *h*, *k*. *l*, [*hkl*] denotes a direction in the basis of the lattice vectors. (*hkl*) denotes a plane orthogonal to [*hkl*].

single TSV. While the detailed process information on Tezzaron technology (e.g. doping concentrate, accurate dimension of MOSFET structure, and etc.) is not available, it is possible to simulate the thermal stress with physical dimension information and general information on the CMOS process. Table IV shows the information of the Tezzaron TSV technology used for modeling.

Table IV. Information on the Tezzaron TSV process

Parameter		value
Wafer crystal orientation		Standard (100), <110>
TSV dimension		W = 1.2μm, L = 6μm
SiO_2 linear thickens		100nm
Process condition (temperature)	W fill deposition	425°C
	SiO_2 liner deposition	400°C
	Cooling	25°C

Table V. Homogeneous Material Properties

Material	Young's modulus *E* (GPa)	Poisson's ratio, *v*
SiO_2	71.4	0.16
Si	131	0.278
W	411	0.29
Cu	115	0.343

In addition, the parameters describing material properties should be set carefully. Since COMSOL has material libraries having default values as shown as Table V, these are used without modification except for the most critical parameter, the orthotropic stiffness matrix. This describes the wafer crystal orientation and gives the stress/strain relationships [82].

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{zx}\\ \sigma_{xy}\end{bmatrix} = \begin{bmatrix} \frac{1-v_{yz}v_{zy}}{E_yE_z\Delta} & \frac{v_{yx}+v_{yz}v_{zy}}{E_yE_z\Delta} & \frac{v_{zx}+v_{yx}v_{zy}}{E_yE_z\Delta} & 0 & 0 & 0 \\ \frac{v_{xy}+v_{xz}v_{zy}}{E_zE_x\Delta} & \frac{1-v_{zx}v_{xz}}{E_zE_x\Delta} & \frac{v_{yz}+v_{yz}v_{xy}}{E_zE_x\Delta} & 0 & 0 & 0 \\ \frac{v_{xz}+v_{xy}v_{yz}}{E_xE_y\Delta} & \frac{v_{yz}+v_{xz}v_{yx}}{E_xE_y\Delta} & \frac{1-v_{xy}v_{yx}}{E_xE_y\Delta} & 0 & 0 & 0 \\ 0 & 0 & 0 & G_{yz} & 0 & 0 \\ 0 & 0 & 0 & 0 & G_{zx} & 0 \\ 0 & 0 & 0 & 0 & 0 & G_{xy} \end{bmatrix} \begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ \varepsilon_{yz}\\ \varepsilon_{zx}\\ \varepsilon_{xy}\end{bmatrix} \quad (16)$$

where $\Delta = \frac{1-v_{xy}v_{yx}-v_{yz}v_{zy}-v_{zx}v_{xz}-2v_{xy}v_{yz}v_{zx}}{E_xE_yE_z}$, Young's modulus ($E$), Poisson's ratio ($v$), and the shear modulus (G) in the x, y, z Cartesian axes. The default orthotropic stiffness matrix for silicon in COMSOL is the <110> direction whose three axes at [100], [010], and [001] as follows.

$$E_x = E_y = E_z = 130\text{GPa} \quad (17)$$

$$v_{yz} = v_{zx} = v_{xy} = 0.28 \quad (18)$$

$$G_{yz} = G_{zx} = G_{xy} = 79.6\text{GPa} \quad (19)$$

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{zx}\\ \sigma_{xy}\end{bmatrix}=\begin{bmatrix}165.7 & 63.9 & 63.9 & 0 & 0 & 0\\ 63.9 & 165.7 & 63.9 & 0 & 0 & 0\\ 63.9 & 63.9 & 165.7 & 0 & 0 & 0\\ 0 & 0 & 0 & 79.6 & 0 & 0\\ 0 & 0 & 0 & 0 & 79.6 & 0\\ 0 & 0 & 0 & 0 & 0 & 79.6\end{bmatrix}\begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ \varepsilon_{yz}\\ \varepsilon_{zx}\\ \varepsilon_{xy}\end{bmatrix} \quad (20)$$

This matrix should be modified for a standard (100)/<110> wafer.

$$E_x = E_y = 169\text{GPa} \qquad E_z = 130\text{GPa} \quad (21)$$

$$v_{yz} = 0.36 \qquad v_{zx} = 0.28 \qquad v_{xy} = 0.064 \quad (22)$$

$$G_{yz} = G_{zx} = 79.6\text{GPa} \qquad G_{xy} = 50.9\text{GPa} \quad (23)$$

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{zx}\\ \sigma_{xy}\end{bmatrix}=\begin{bmatrix}165.7 & 35.7 & 64.1 & 0 & 0 & 0\\ 35.7 & 165.7 & 64.1 & 0 & 0 & 0\\ 64.1 & 64.1 & 165.7 & 0 & 0 & 0\\ 0 & 0 & 0 & 79.6 & 0 & 0\\ 0 & 0 & 0 & 0 & 79.6 & 0\\ 0 & 0 & 0 & 0 & 0 & 50.9\end{bmatrix}\begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ \varepsilon_{yz}\\ \varepsilon_{zx}\\ \varepsilon_{xy}\end{bmatrix} \quad (24)$$

With these settings, the FEM modeling is performed, and Fig. III.9 shows the results. σ_r is 200MPa tensile stress, and σ_θ is 200MPa compressive stress. σ_z is in compressive direction but relatively small.

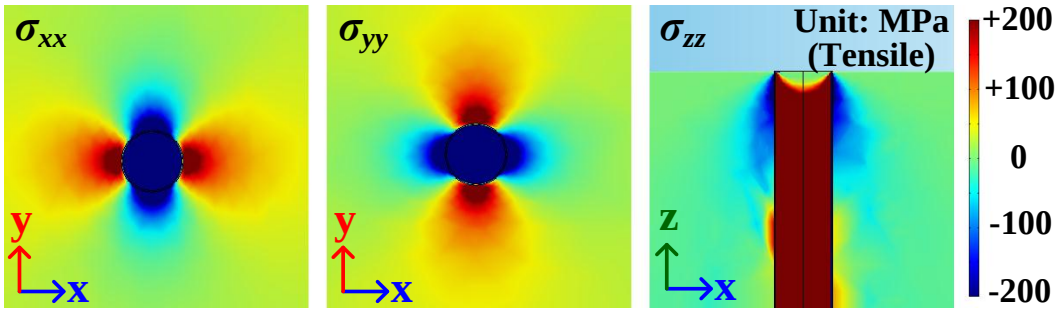


Fig. III.9. Stress along the x, y, and z axis.

As described previously, the CTE mismatch induces tensile σ_r, compressive σ_θ, and compressive σ_z stresses. Both σ_r and σ_θ are less than 300Mpa, while σ_z shows negligible strength. At stresses less than 1GPa, the linear piezroresistance model can be used as follows [83][84].

$$(\text{mobility change}) = \pi_L \cdot \sigma_L + \pi_T \cdot \sigma_T + \pi_{12} \cdot \sigma_{ZZ} \tag{25}$$

where σ_L, σ_T, σ_{ZZ}, π_L, π_T, and π_{12} denote the longitudinal, transverse, transverse and vertical stresses and piezoresistive coefficients. The values of σ_L, σ_T, and σ_{ZZ} can be obtained from a FEM simulation. π-coefficients are material properties explaining the relationship between the stress and the induced resistivity change. Table VI shows three different π-coefficients for n-doped and p-doped silicon substrate [85].

Table VI. Piezroresistive Coefficients of bulk Silicon

Material	ρ_0 [Ω·cm]	π_{11} [10^{-11}/Pa]	π_{12} [10^{-11}/Pa]	π_{44} [10^{-11}/Pa]
n-Si	11.7	-102.2	53.7	-13.6
p-Si	7.8	6.6	-1.1	138.1

From [86], current change can be expressed as follows.

$$\left.\frac{\Delta I_D}{I_D}\right|_{0^\circ} = \left(\frac{\pi_{11}+\pi_{12}}{2}+\frac{\pi_{44}}{2}\right)\sigma_{xx} + \left(\frac{\pi_{11}+\pi_{12}}{2}-\frac{\pi_{44}}{2}\right)\sigma_{yy} + \pi_{12}\sigma_{zz} \tag{26}$$

$$\left.\frac{\Delta I_D}{I_D}\right|_{90^\circ} = \left(\frac{\pi_{11}+\pi_{12}}{2}-\frac{\pi_{44}}{2}\right)\sigma_{xx} + \left(\frac{\pi_{11}+\pi_{12}}{2}+\frac{\pi_{44}}{2}\right)\sigma_{yy} + \pi_{12}\sigma_{zz} \tag{27}$$

Also, [87] indicates piezoresistive coefficients as shown in Table VII.

Table VII. Piezroresistive Coefficients depending on the channel and stress directions of (100)/<110> wafer

Channel (φ')	Stress (Φ)	π_{eff}
[110] ($\varphi'=45^0$)	[110] ($\Phi=45^0$)	$(\pi_{11}+\pi_{12}+\pi_{44})/2$
[110] ($\varphi'=45^0$)	[$\bar{1}$10] ($\Phi=135^0$)	$(\pi_{11}+\pi_{12}-\pi_{44})/2$
[100] ($\varphi'=0$)	[010] ($\Phi=90^0$)	π_{12}

From the equations, longitudinal, transverse, and vertical piezoresistive coefficients can be expressed as follow.

$$(\text{Longitudial piezoresistive coefficient}) = \pi_L = \frac{\pi_{11}+\pi_{12}+\pi_{44}}{2} \quad (28)$$

$$(\text{Transverse piezoresistive coefficient}) = \pi_T = \frac{\pi_{11}+\pi_{12}-\pi_{44}}{2} \quad (29)$$

$$(\text{Vertical piezoresistive coefficient}) = \pi_{12} \quad (30)$$

Finally, all piezoresistive coefficients can be express as shown in Table VIII.

Table VIII. Piezroresistive Coefficients for bulk Silicon of (100)/<110> wafer

Carrier	π_L [10^{-11}/Pa]	π_T [10^{-11}/Pa]	π_{12} [10^{-11}/Pa]
electron	-31.6	-17.6	53.7
hole	71.8	-66.3	-1.1

Based the thermal stress and piezoresistive coefficients, Fig. III.10 shows the FEM simulation results of the hole and electron mobility change due to stress direction and strength. The diagonal directions of TSVs are stress-free, and there is no mobility change.

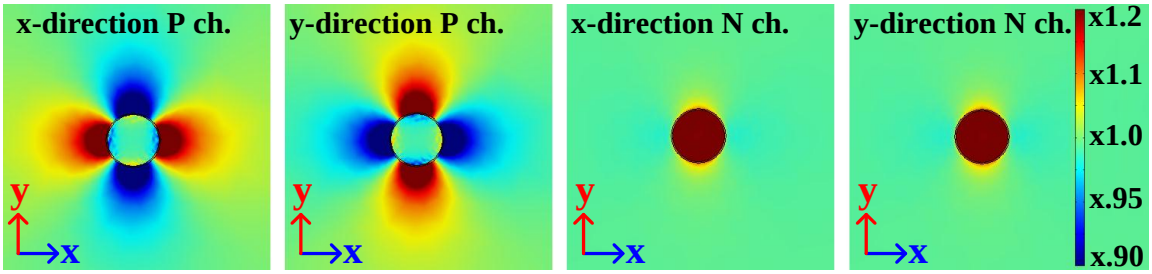


Fig. III.10. Mobility change of PMOS and NMOS.

From the results, mobility changes depending on the distance are extracted which show good agreement with measurements as depicted in Fig. III.11. For comparison, Cu TSVs were also simulated in the same environment, and these simulation results show much more severe mobility change compared to W TSVs due to the lager CTE mismatch between Si (2.7ppm/^{0}C) and Cu (16.7ppm/^{0}C).

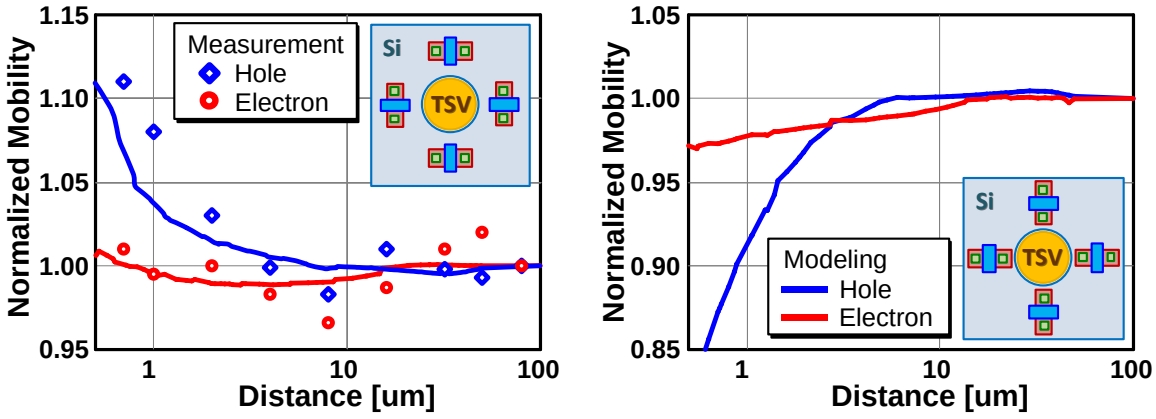


Fig. III.11. Comparison of measured and modeling results.

Threshold voltage is not affected by TSVs, while mobility is affected by as much as 10% for devices within 4μm of a TSV. A keep-away-zone of 4μm should be considered for minimal impact on device performance.

Chapter IV.
IC using Resonant Inductive Coupling

IV.1 Introduction

Based on the theory described in Chapter II, the first prototype IC of an inductive data link has been fabricated. It exploits RIC (resonant inductive coupling) to extend communication range without increasing the coil size. The prototype has not only vertical channels but also routing channels for a network on chip (NoC). Crosstalk is utilized to communicate between coils in a routing coil array as shown in Fig. IV.1. Usually crosstalk among coils has a small coupling factor *k*. RIC is applied to overcome this small *k*.

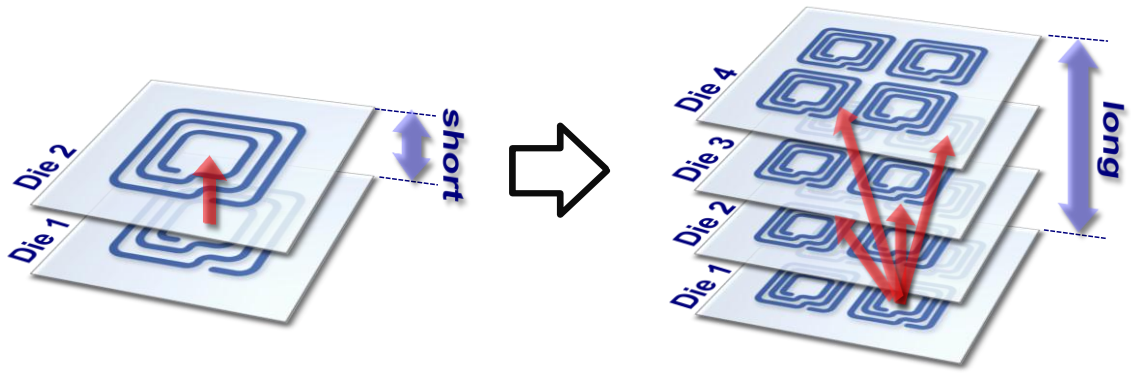


Fig. IV.1. Concept of the proposed system.

Conventional inductive data links transmit mono-pulses using binary phase shift keying (BPSK) [46][47]. This current mono-pulse at a transmitter induces a mono-cycle voltage at the receiver. The receiver senses the polarity of the first peak of the pulse with a sense amplifier as shown in Fig. IV.2(a). Because the peak width is narrow, this method requires accurate control of the sampling time at the receiver. To relax the timing requirements on the receiver, another method has been proposed in which the pulse level is directly latched [48]. When the transmitter current is inverted, the transition induces a voltage pulse at the receiver large enough to be recovered using a hysteretic comparator as shown in Fig. IV.2(b). This method eliminates the clock timing issue, but it consumes significant power because of the DC current at the transmitter. Because it shows low energy-per-bit values only at high-speed data-rates, it is not suitable for low-speed applications. In addition, in order to produce an induced voltage large enough to flip the hysteretic comparator, it requires a large k, resulting in low aspect ratio (i.e. short communication distance or larger coils).

The proposed method uses on-off keying (OOK) modulation and transmits multiple cycles of current in order to transmit a '1', and no signal when transmitting a '0'. The sinusoidal signal at the transmitter induces a sinusoidal voltage signal at the receiver, which is much larger when compared to other single-pulse methods due to the boost from RIC. Because the data are recovered by integrating the received voltage, accurate timing is also not necessary. The proposed waveform is shown in Fig. IV.2(c).

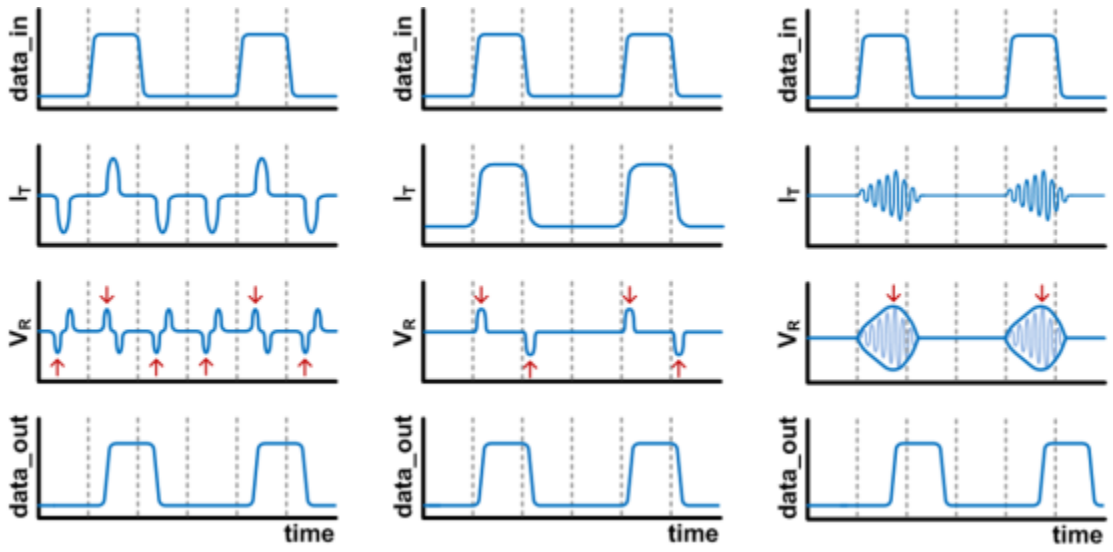


Fig. IV.2. Comparison of operation. (a) Transmitting current pule and receiving with sense amplifier. (b) Transmitting current level and receiving with hysteresis comparator. (c) Transmitting tone and receiving by integrating.

IV.2 Channel Modeling

Inductor design for RIC is more critical than for SIC because its inductance and *Q*-factor play a significant role in the performance of an RIC channel. In addition, in order to implement a coil array for routing channels, not only coil size, but also the relative position of coils in the coil array is important. The channel modeling is the first step for the system design.

IV.2.1 **Basic Coupled Inductor Pair**

Before creating a coil array for a routing system, the effect of the relative location of the coils on the coupling coefficient should be analyzed. Fig. IV.3 shows the contour of

the coupling coefficient of two coupled coils. A transmitting coil is fixed at the origin, and the position of a receiving coil is changed along the x, y, and z axes. The coupling coefficients between two coils are measured, and the same values are connected together by one contour face. The contour is lobe-shape along the vertical direction and donut-shape in a horizontal plane. It has nulls between the main lobe and the donuts. It has a dead zone for inductive coupling at about a 45 degree angle that should be avoided when implementing the routing system.

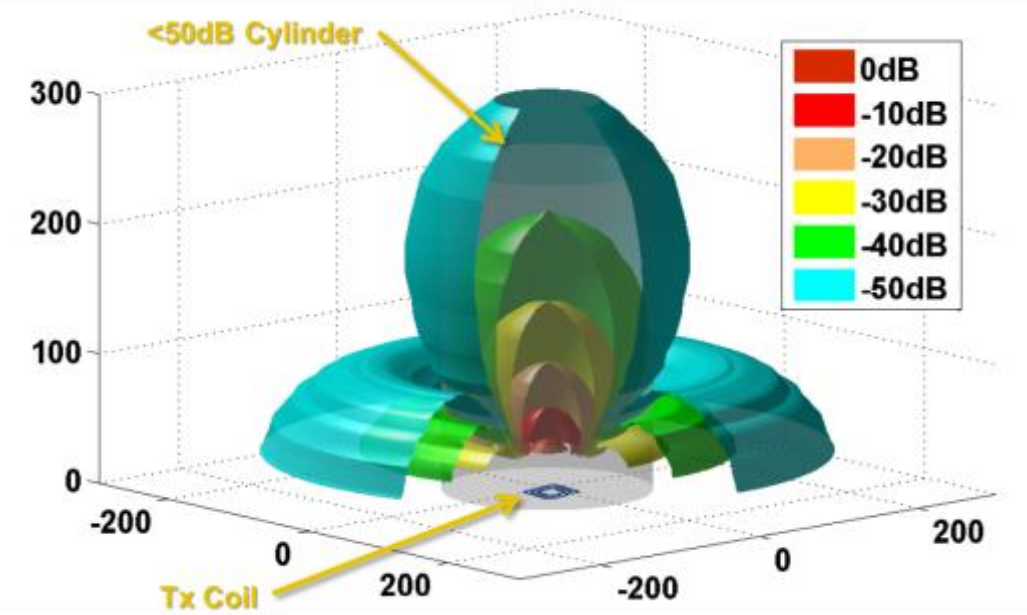


Fig. IV.3. Contour of coupling strength between two coils.

IV.2.2 **4x4 Routing Coupled Inductors**

The prototype routing system has 4 layers with 2-by-2 coils per single layer. It includes a total of 16 coils, and it is designed so that one coil can talk to any coil in the

stack. Fig. IV.4 shows the 4-by-4 coil array structure. Because of Tezzaron's stacking method [88], the distance between adjacent layers except the second layer and the third layer is 6μm. The gap between second layer and third layer is 18μm. To minimize the dead zone between coils, the coil size is empirically selected as 30μm in diameter.

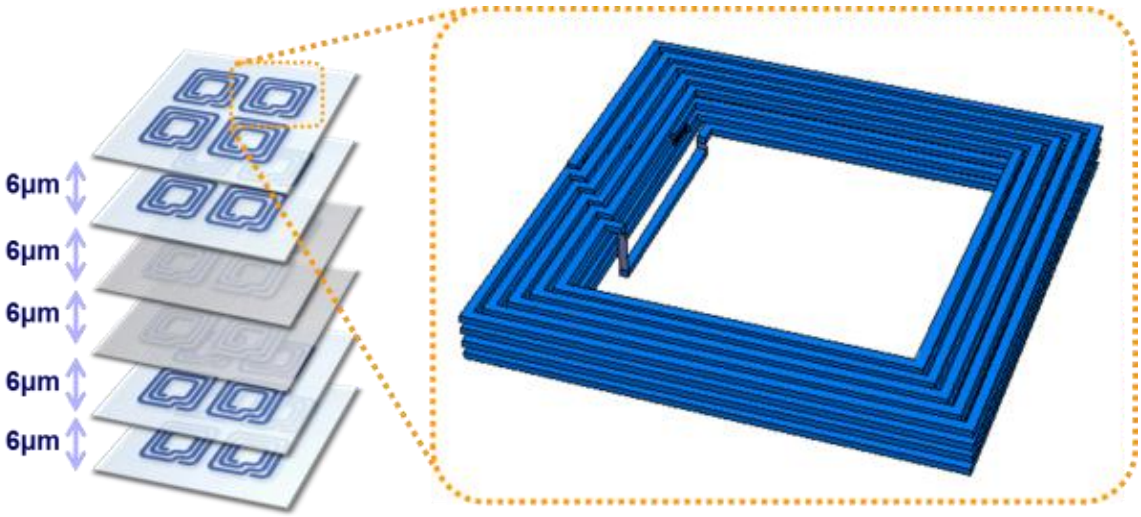


Fig. IV.4. 4-layer 2x2 coil array structure.

The channel modeling of the coil array is simulated using the commercial 3D Electromagnetic field analysis tool, HFSS, and the self-inductance and mutual inductance between coils with frequency sweeping are shown in Fig. IV.5. At a 6μm distance, which corresponds to the distance between first and second layers, or third and fourth layers, the mutual inductance along a 2D diagonal direction and a 3D diagonal direction has a negative value. This is because the receiving coil is located in the donut area in Fig. IV.3. It doesn't affect the inductive data link other than inverting the polarity of the data, which can be easily compensated for.

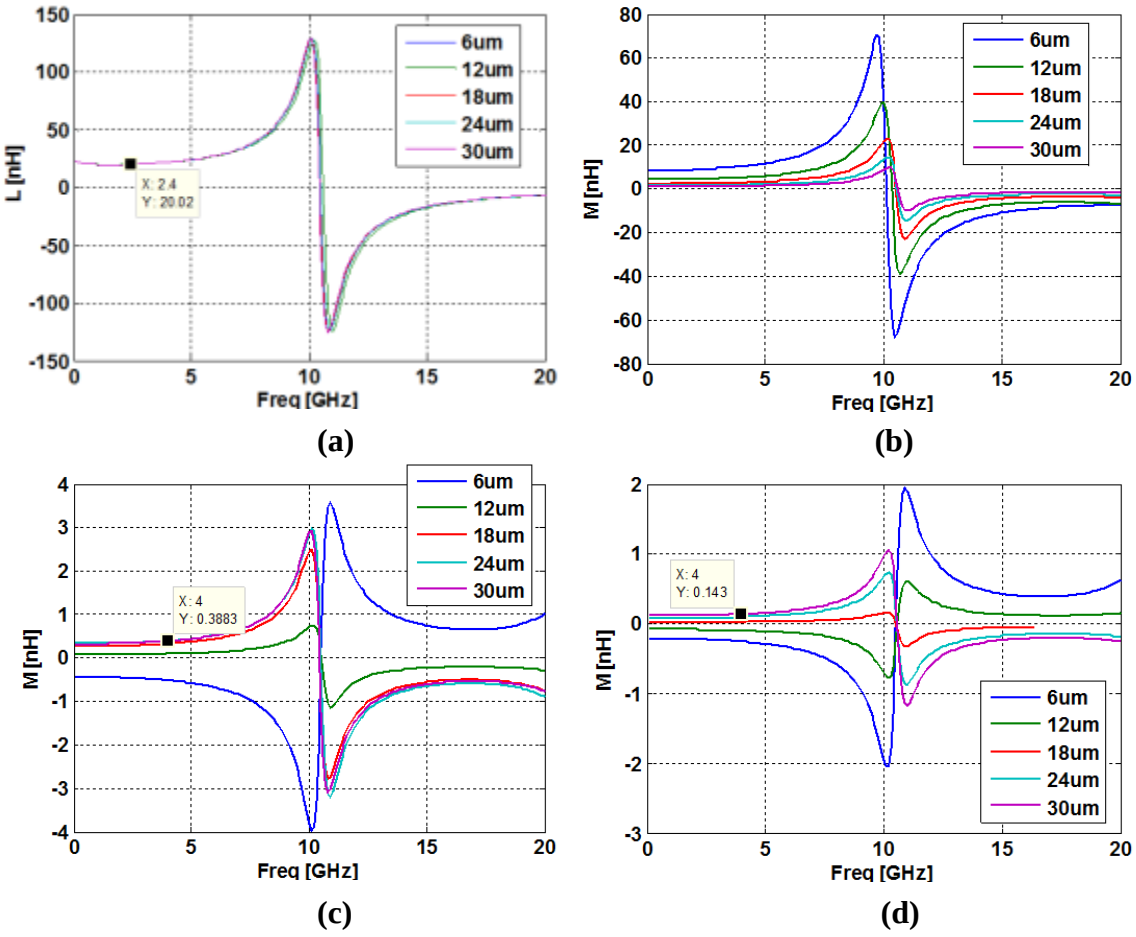
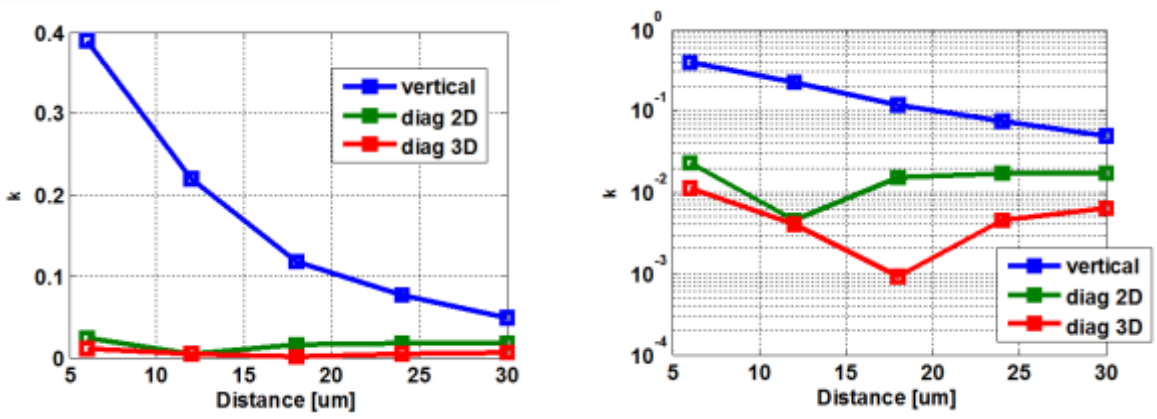


Fig. IV.5. Frequency sweep of inductance (a) Self-inductance (b) Mutual inductance along vertical direction (c) Mutual inductance along 2D diagonal direction (d) Mutual inductance of 3D diagonal direction

The self-resonant frequency of the design coil is approximately 10GHz, and the operating frequency of the RIC link should be lower than this value. 5-6GHz is chosen as the operating frequency considering the parasitic capacitance of the transceiver circuits. This will be explained further in the following section.

Fig. IV.6 shows the relationship of the distance between two coils and the coupling coefficient at the operating frequency. The minimum value comes from the 3D diagonal direction between 18μm-apart layers (the second and third layers). It is expected that the

communication at these channels is infeasible based on the extremely low simulated value of coupling coefficient *k*.



(a) **(b)**

Fig. IV.6. Coupling coefficient vs. distance at 5GHz (a) Linear (b) Logarithm.

In Chapter 2, the induced voltage from RIC was found to be Q^2 times larger when compared to SIC in the weakly coupled regime. While larger Q increases the received signal strength and enables longer-range communication, it might negatively affect the data-rate because of the narrower bandwidth. The growth rate of oscillations at the receiver is proportional to $1/Q$; larger Q increases the time it takes to turn on and off the oscillations, resulting in a reduction of data-rate. Therefore, the Q-factor is designed to trade off the received signal strength and data-rate. A Q-factor of 3-4 is selected to achieve a 1Gbps of data-rate. This provides approximately 10x improvement in signal strength, corresponding to more than a 2x increase in distance.

IV.3 Circuit Design

The prototype IC has four different communication channels to test communication at different distances: 1) short-range channel, 2) middle-range channel, 3) long-range channel, and 4) routing channel. These four channels have different communication ranges, coil size and allocation as shown in Fig. IV.7. For the sake of simplicity, the routing channel will be described here because it includes all functionality of the other channels.

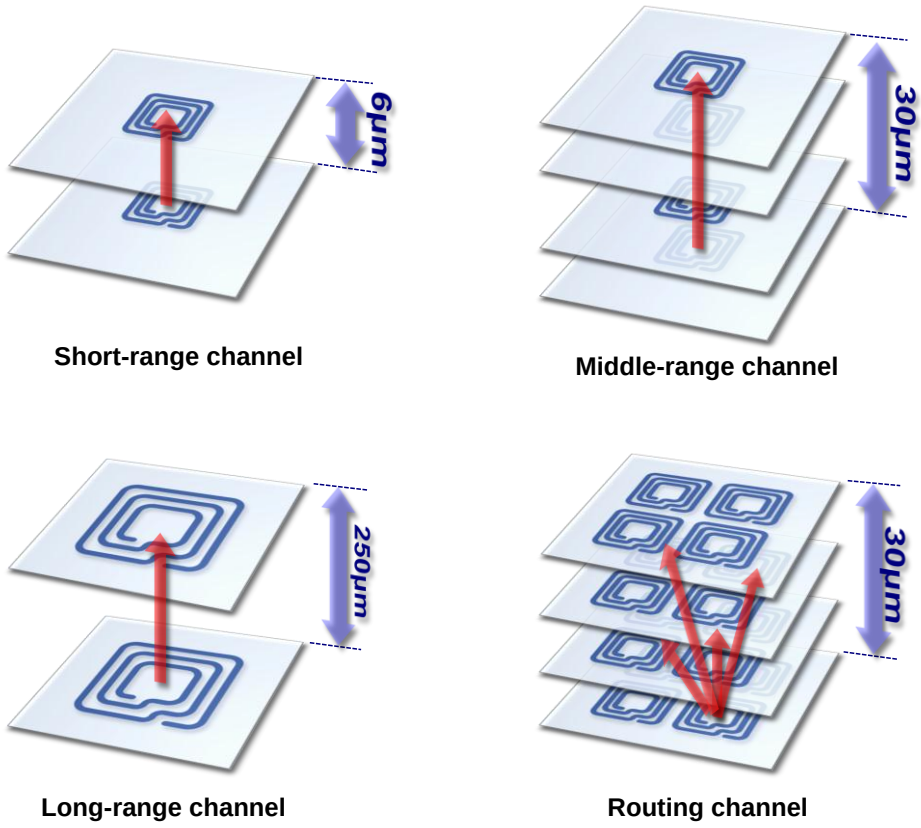


Fig. IV.7. Diagram of four different channels.

Fig. IV.8 shows the overall architecture of the routing system and a block diagram of one communication node. The communication node works as both a transmitter and

receiver, and the selection between the two is programmed externally. A transmitter and receiver share the inductor as the antenna for wireless communication. Each layer has four communication nodes, and four layers are stacked vertically for a total of 16 nodes altogether.

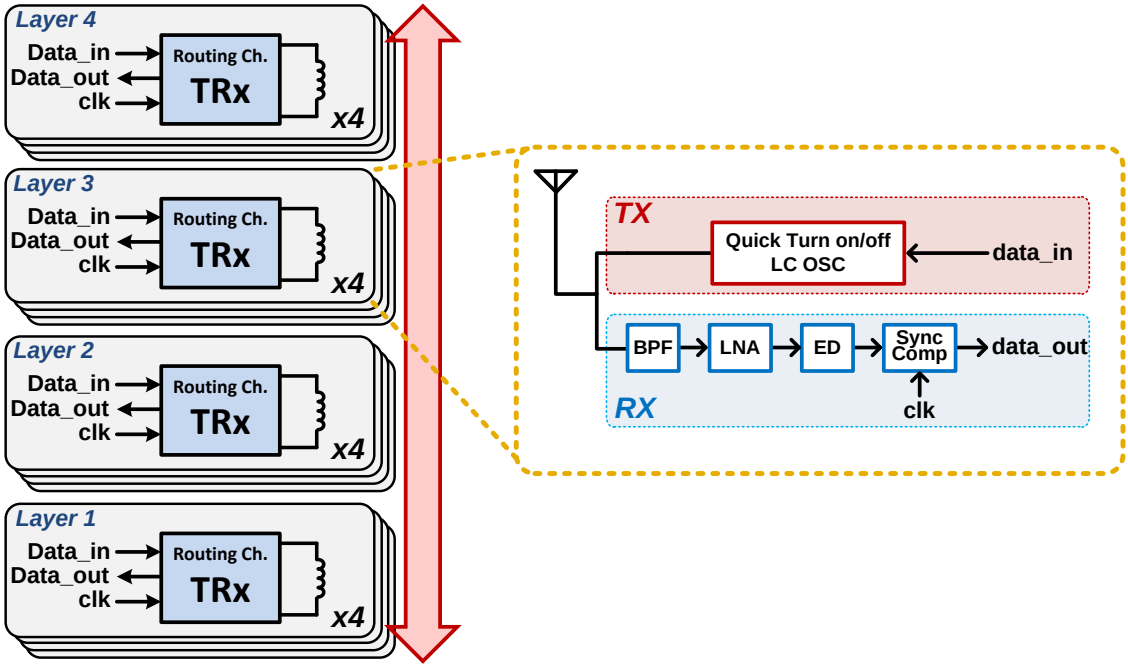


Fig. IV.8. Block diagram of overall system. (Routing Channels)

IV.3.1 **Transmitter**

The transmitter is basically an LC oscillator because, in RIC, an inductor is used not only for the antenna, but also in an LC tank for generating oscillations. It is designed to have a 1Gbps data-rate at a 5~6GHz center frequency, which means there are 5~6 RF cycles in one data period. Since this cycle number is small compared to general OOK, quick turn-on and turn-off circuits are required to generate and detect the signals. Even though a cross-coupled LC oscillator is widely used to make oscillations due to its small

phase noise, it is not suitable for this application because it requires relatively large turn-on time. Therefore, a modified cross-coupled LC oscillator is used instead since it has a quick turn-on time and drives a relatively large amount of current as depicted in Fig. IV.9. The transmitter adopts this topology and uses the combination of a communicating inductor and parasitic capacitance C_{gd}, C_{ds} as the LC tank for oscillation. When a high signal comes into *data_in* pin, it turns on the oscillation in the LC tank and generates an oscillating magnetic field. When data is low, it stops the oscillation.

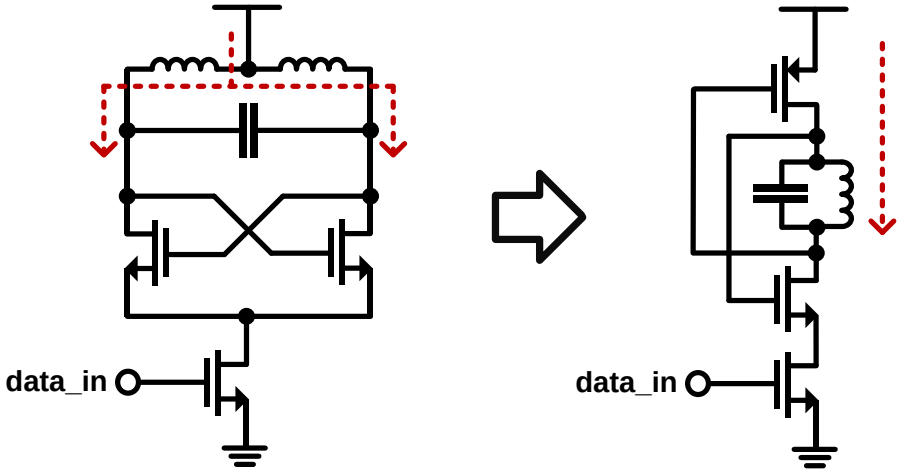


Fig. IV.9. Different types of LC oscillator. Instead of Cross-coupled LC oscillator, a modified cross-coupled LC oscillator is used.

In order to achieve a fast turn-off time, a quenching switch is added across the LC tank. It is made with a 2.5V thick-oxide transistor to reduce the on-resistance. Fig. IV.10 shows the transmitter schematic with the quenching switch and the simulated output waveforms. When *data_in* = 1, the switch is shut off and does nothing. A low signal into the *data_in* pin makes the switch turn on and detours the current which was in the LC tank into the drain quickly. The signal into the /*data_in* pin and the signal into the

data_in pin should have the opposite phase without overlapping. In order to generate the signal into the *data_in* pin, conventional level converters are used.

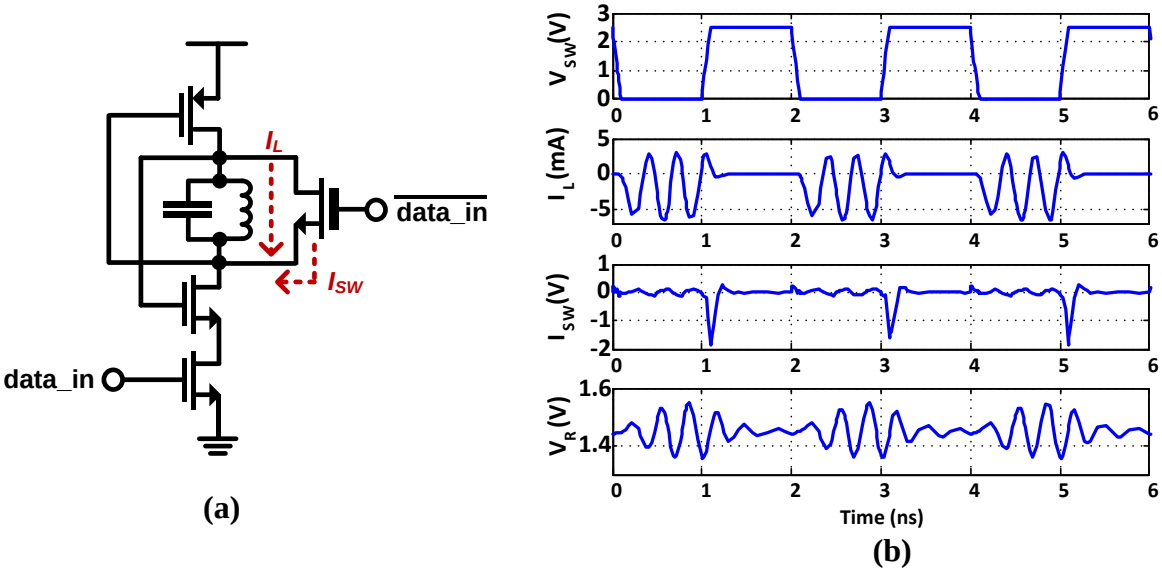


Fig. IV.10. Transmitter with a quenching switch. (a) schematic (b) waveform

IV.3.2 **Receiver**

When using RIC, the receiver should have a LC oscillator with a resonant frequency matched to that of the transmitter. When considering the process variation of the inductor and parasitic capacitance, it is safer to use an identical layout of the LC tank at both the transmitter and receiver. Therefore, the receiver shares the same LC tank as that of the transmitter by integrating these together as shown in Fig. IV.11. When in receiving mode, the data input becomes '0', and the *Tx_mode* switch is turned off. This makes the transmitter circuit work as a passive LC tank or band pass filter (BPF). After the LC tank, the receiver has low noise amplifiers (LNAs), a differential envelope detector and a synchronous comparator. Because LNAs require DC biasing, the center tap of the inductor is connected to a bias voltage.

The stage after the LC tank and LNAs is an envelope detector with differential input and single-ended output as shown in Fig. IV.12. It is designed to be an active type envelope detector to have sufficient gain for the following comparator stage [90].

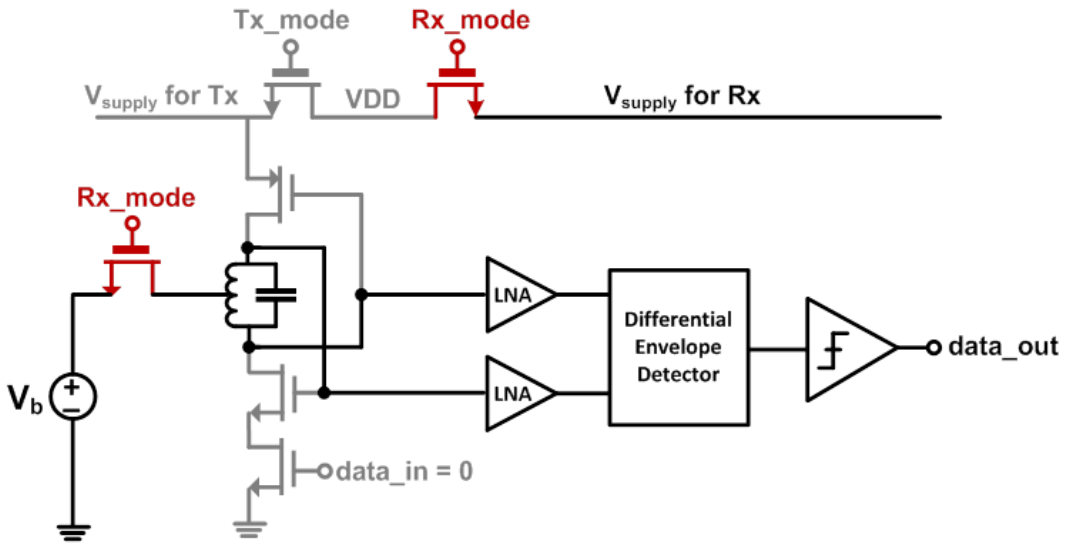
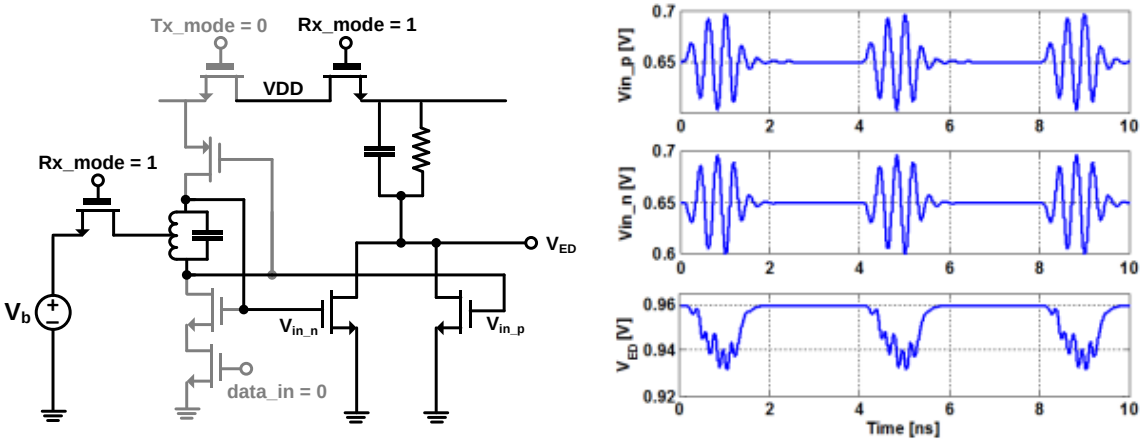


Fig. IV.11. Schematic of a receiver.



(a) **(b)**

Fig. IV.12. Active envelope detector. (a) schematic (b) transient waveform

The last part of the receiver is a two-stage synchronous comparator as shown in Fig. IV.13. One input of the comparator is the output of the envelop detector. The other input is connected to a replica circuit to generate a DC voltage to be compared [91]. Since its timing window is larger than 500ps (half of the data bit time) the clock timing is relaxed relative to the clocked-sense amplifier approaches [46][47]. The minimum detectable voltage is 9mV at 1Gpbs considering offsets in the receiver and simulation across all process corners.

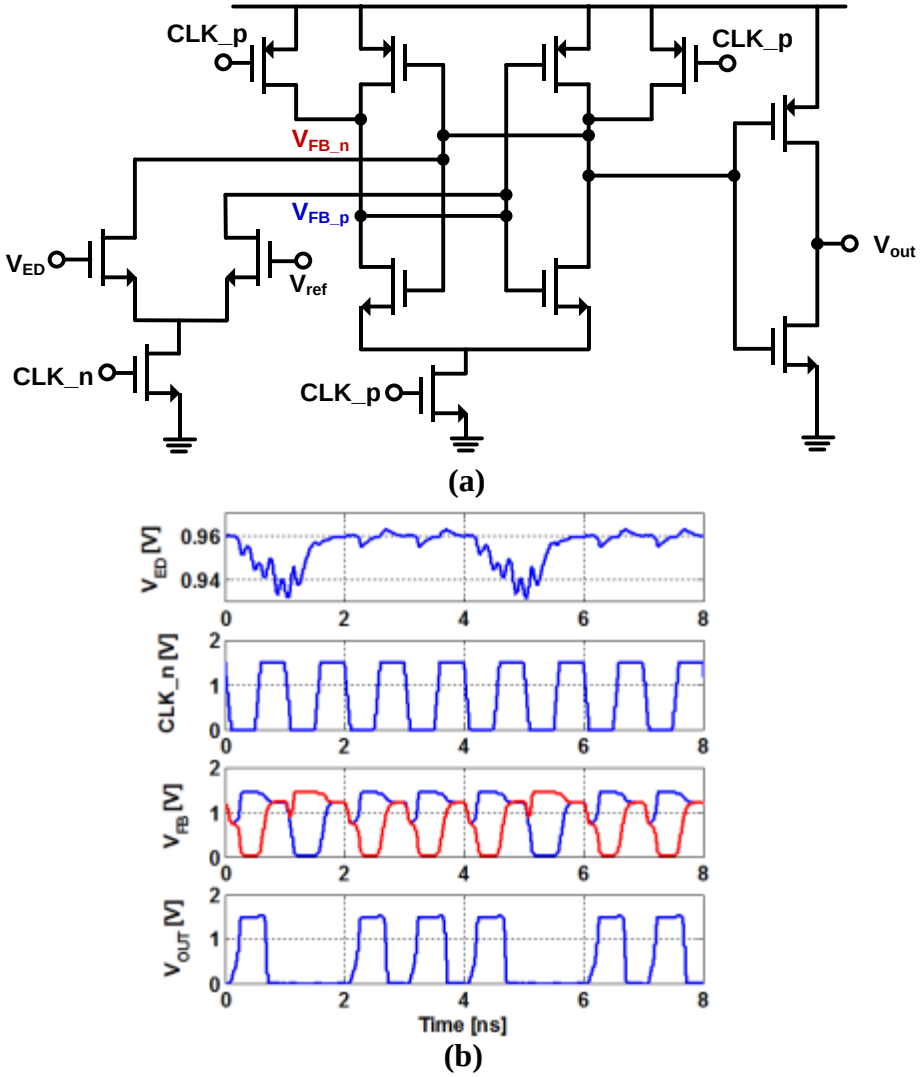


Fig. IV.13. Synchronous comparator. (a) schematic. (b) transient waveform.

IV.3.3 **Transceiver**

As explained before, the receiver and the transmitter are integrated together, and its function is selected by controlling a header switch. When in the transmitting mode, the power for the receiver circuits are disconnected, and the power for the transmitting oscillator is turned off for receiving mode. Fig. IV.14 shows the different prototype circuits implemented in the test chip, targeting different range communication channels.

The short-range channel consists of an LC oscillator, active envelope detector, and baseband amplifier. Since it targets very short communication, any block for large gain is not required such as LNA and comparator. The middle-range channel, however, has a synchronous comparator since the output of the envelop detector is smaller than that of the short-range channel. The routing channel requires LNAs as well because the induced signal at BPF could be too small to be detect at the envelop detector without LNAs.

The middle-range channel and routing channel have multiple *Tx_mode* switches to control the strength of oscillation based on the distance to the target node. All power switches use 2.5V thick-oxide transistors.

IV.3.4 **System for Testing**

In order to test the wireless interconnect, peripheral blocks are designed as well. A linear feedback shift register (LFSR) generates a pseudo random sequence for input data. Output data from the wireless channel is compared to the original input data, and the number of errors is counted with an on-chip bit-error-rate (BER) counter. Fig. IV.15 shows the system with middle-range and routing channels including all peripheral blocks.

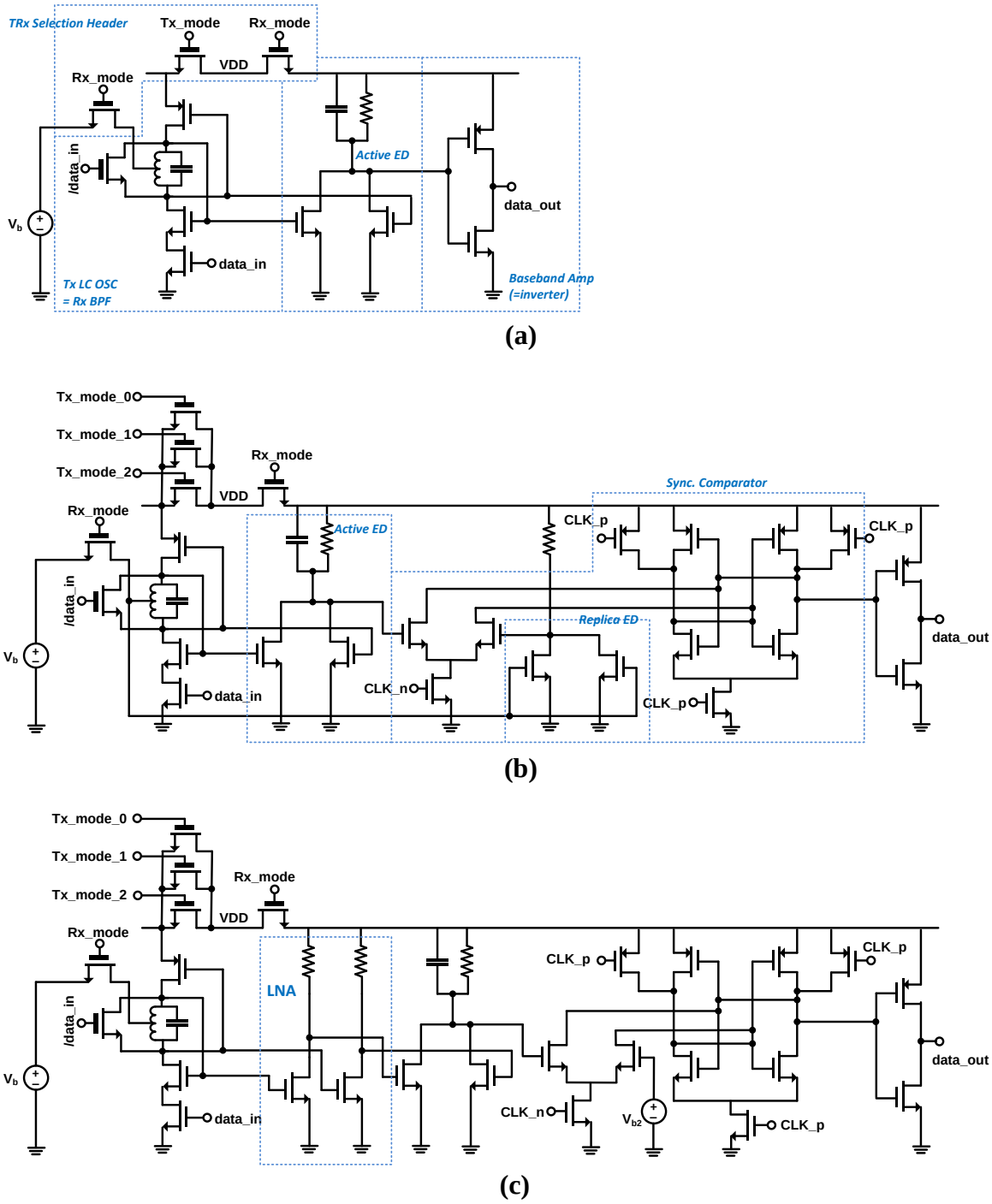


Fig. IV.14. Overall schematic of channels. (a) short-range channel. (b) middle-range channel. (c) Routing channel.

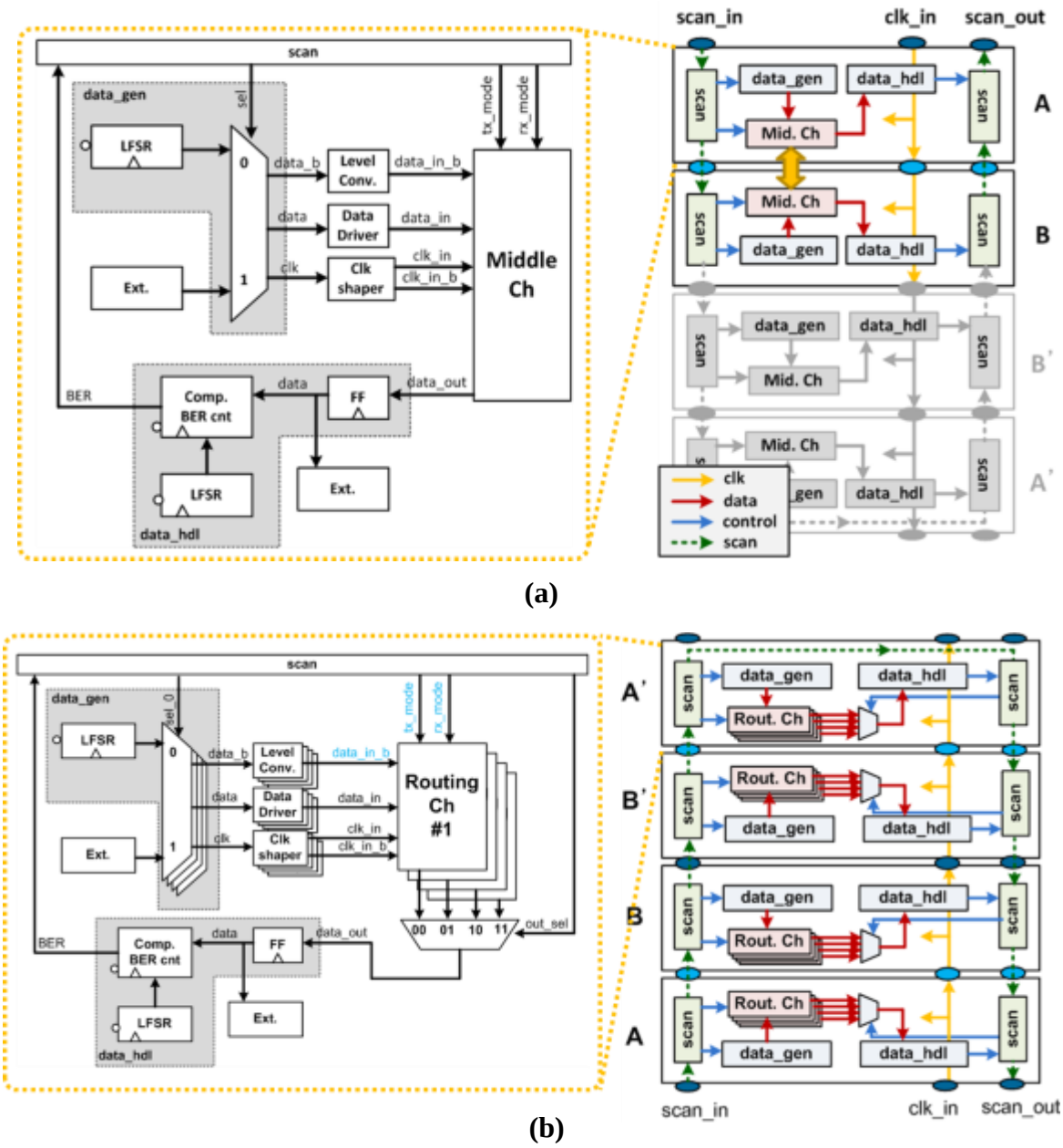
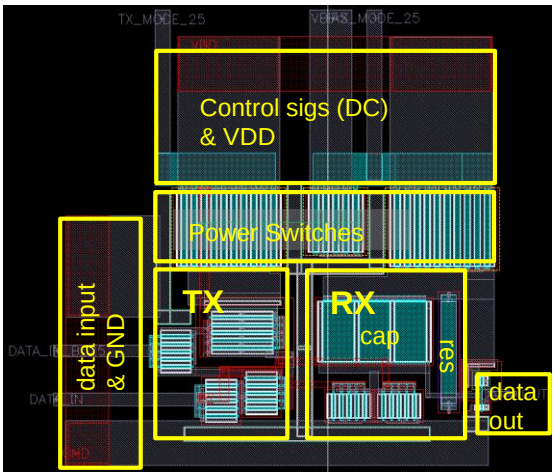


Fig. IV.15. Bock diagram of whole system. (a) middle range channel (b) routing channel

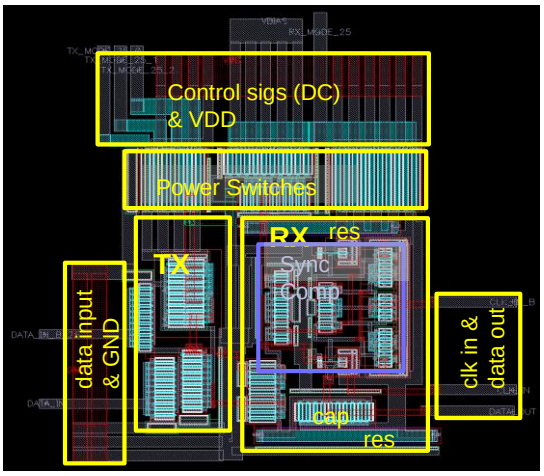
IV.4 Layout

In order to save silicon area, all transceiver circuits are located beneath the coil. This could cause several problems if not designed correctly. The area for design is highly

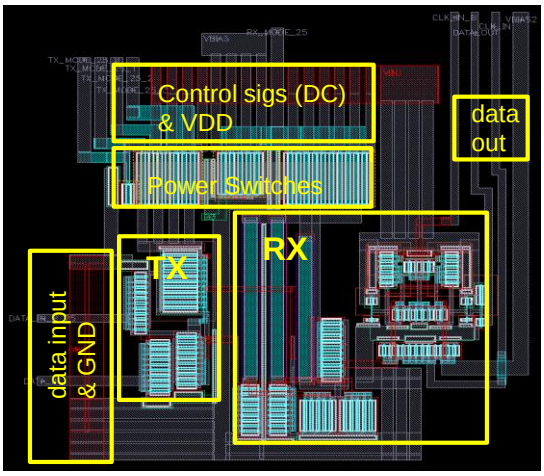
constrained, and the circuit might reduce *Q*-factor of the coil. The most critical issue is that the magnetic field could generate an eddy current in the circuit, and this might cause malfunction.



Short-range channel



Middle-range channel



Routing channel

Fig. IV.16. Layout of different channels.

Therefore, the circuit layout should be performed carefully considering the above-stated issues. Fig. IV.16 shows the layout of the short-range, middle-range, and routing channel except for the coils respectively. All circuits are designed to use only poly and

metal 1 layers since upper metal layers are designated for the coil layout. Whole layouts are packed into the square coil size (25x25μm or 30x30μm). Fig. IV.17 shows the 2-by-2 routing channel on one layer.

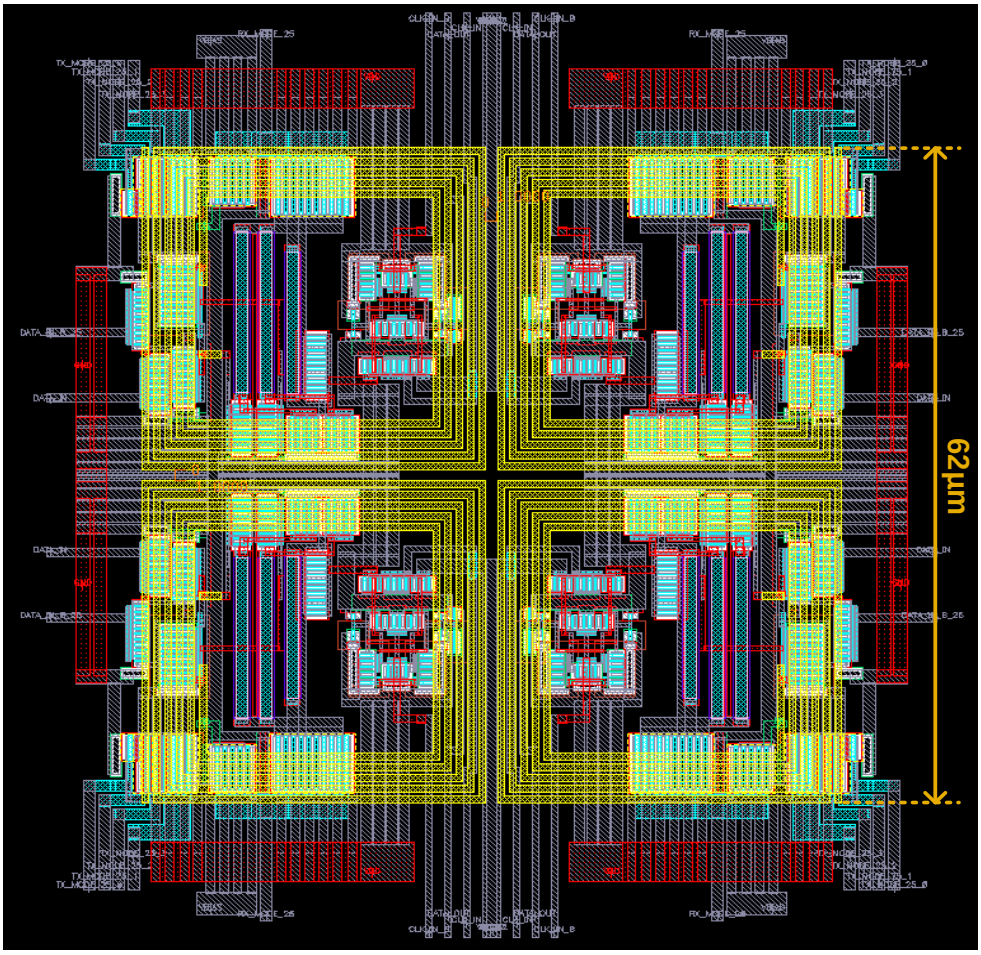


Fig. IV.17. Layout of 2-by-2 routing channels on one layer.

No closed loops are made since eddy current could be induced in them. Self-inductance of any unclosed interconnect in the circuit is small relative to self-inductance of the coil, which means the induced current in the interconnect will be negligible. Moreover, since the parasitic capacitance of the net is also small, its self-resonant frequency will be much higher than the RIC operating frequency, and the induced current

will not be grown by oscillation. Finally, any large metal plate, for instance power and ground connections, are slotted to prevent the induction of eddy current and degradation of *Q*-factor.

Fig. IV.18 depicts 2-by-2 routing channels at the center and the peripheral circuits for testing surrounding them. The pseudo-random binary sequence (PRBS) generator and data comparator are synthesized with standard cells. Thick and long metal wires are for DC or low frequency signals.

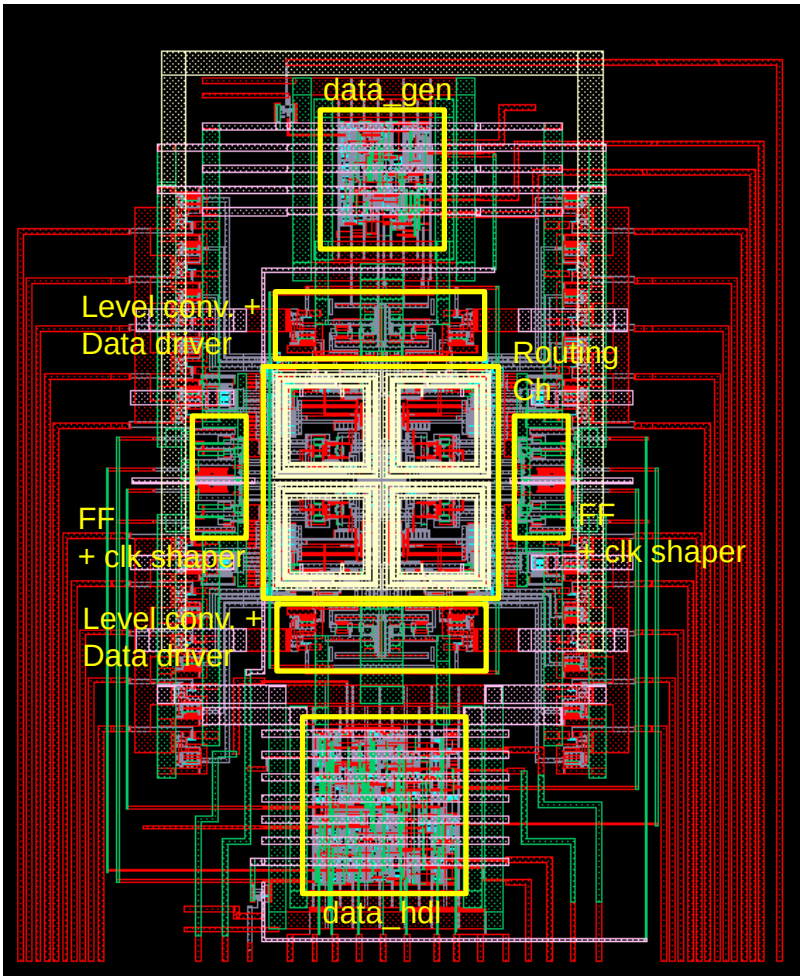


Fig. IV.18. Layout of 2x2 routing channel and peripheral blocks for testing.

The layout of the whole system is shown in Fig. IV.19. It consists of four layers. The short-range channels are designed on layer 1 and layer 2. The middle-range and routing channels are made over all layers. Since layer 1 is the only one exposed to the external world when stacked, it has a pad-ring.

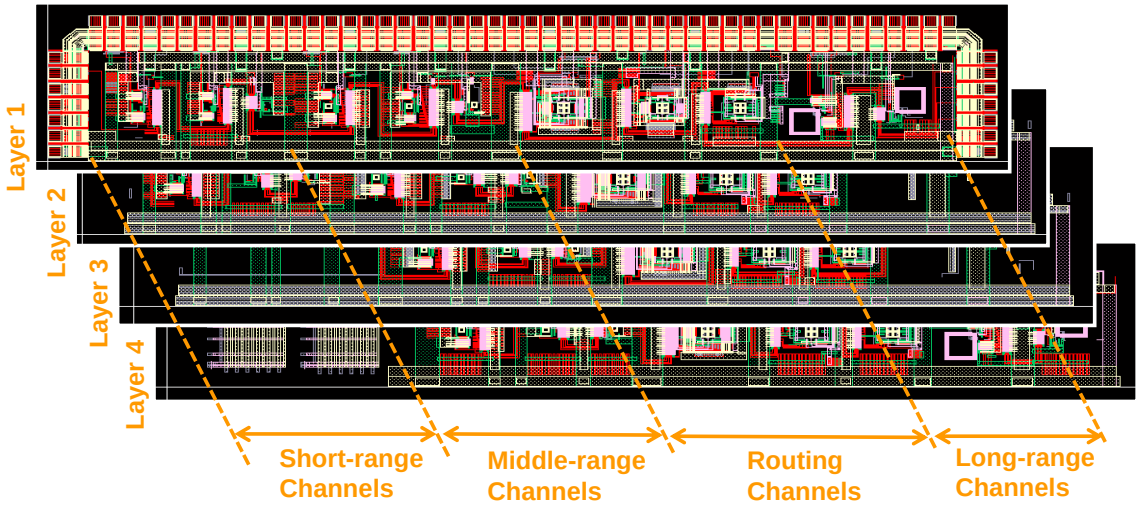


Fig. IV.19. Layout of whole system.

IV.5 Measurements

This prototype IC was taped out on March 2010. However, fabrication of the 4-layer stack has not been completed yet as of April 2012, and only two-layer stacks have been delivered. Because the routing channel was designed for a four-layer stack, only the short-range channel and middle-range channel have been tested.

The diameter of the coils used for the short-range channel is 25μm, and the channel's communication distance is 6μm. It has a data rate of 1Gbps with 1.2mW power consumption, resulting in an energy per bit of 1.2pJ/b. The middle-range channel uses 30μm-diameter coils, targeting a communication distance up to 30μm but only 6μm is measured. The measured data rate of this channel is 1Gbps, and the power consumption

is 1.55mW. The measured BER of both channels is less than 10^{-12}. Table IV shows a summary of the measurements from these channels. The simulation results of the routing channel and middle channel with 30μm distance are also shown.

Table IX. Measurement Summary

Parameter		Short-range	Middle-range	Middle-range *	Routing *
Coil Size		25μm	30μm	30μm	30μm
Comm. Distance		6μm	6μm	30μm	Min.: 6μm (vertical) Max. :52μm (3D diagonal)
Area of Channel		625μm^2	900μm^2	900μm^2	900μm^2
Supply		1.5V	1.5V	1.5V	1.5V
Data Rate		1Gbps	1Gbps	1.1Gbps	1.05Gbps
Bit Error Rate		<10^{-12}	<10^{-12}	N/A	N/A
Bandwidth / Area		1600Gbps/mm^2	1111Gbps/mm^2	1222Gbps/mm^2	1167Gbps/mm^2
Power Consumption	Tx	400μW	350μW	540μW	580μW **
	Rx	800μW	1200μW	1200μW	2100μW **
Energy / bit		1.2pJ/b	1.55pJ/b	1.58pJ/b	2.55pJ/b

* Simulation results for comparison

** The maximum power consumptions when the maximum distance

Fig. IV.20 shows the die photo of whole system, and Fig. IV.21 shows a bird's-eye view of the two-layer stacked die and test PCB board. Since the chip size is relatively large (12mm x 5mm) compared to the size of the wireless links, it is difficult to find proper packaging for the die. Instead of using a typical package or chip-on-board (COB),

a substrate having castellated holes was designed, and the dies are attached on the substrate using COB. This substrate is then attached to a larger PCB for testing.

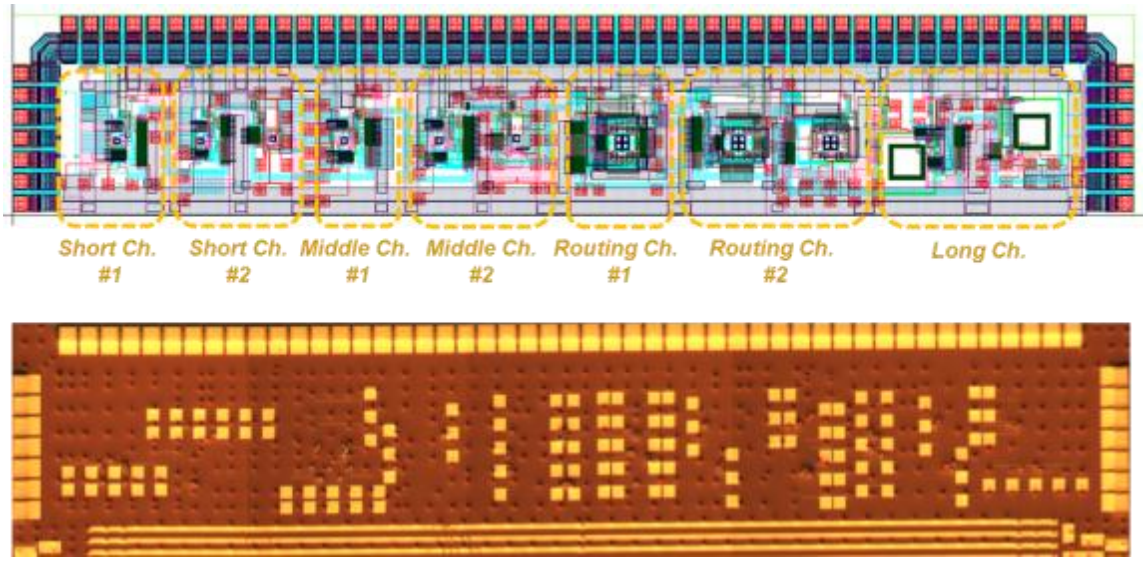
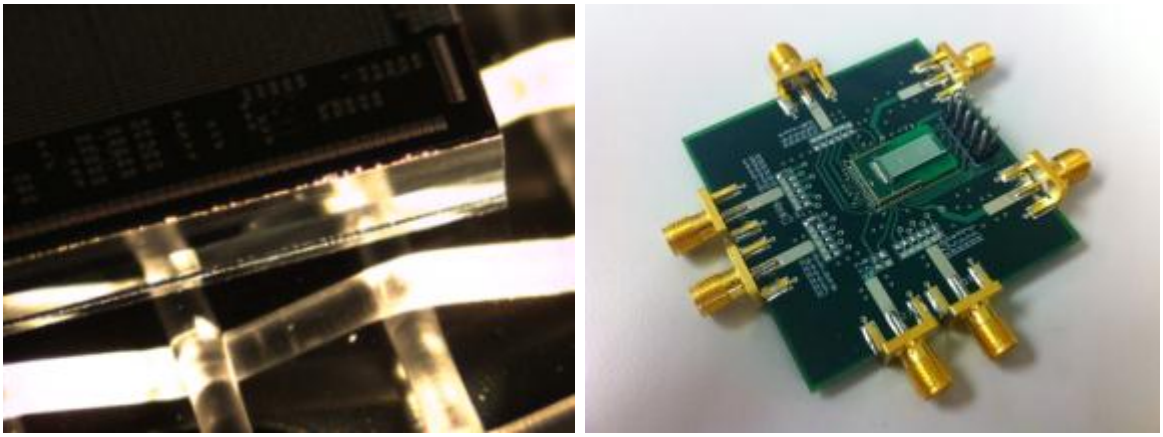


Fig. IV.20. Die photo of whole system. The area is 5mm x 1mm.



(a) **(b)**

Fig. IV.21. (a) Two layer stacked die. (b)test board.

Chapter V.
IC using Multi-Layer Signal Boosting

V.1 Introduction

The second prototype IC of an inductive data link has been fabricated based on the MLSB (multi-layer signal boosting) scheme discussed in Chapter II. Inductive coupling is one technique used to create through-die-interconnect between vertically stacked multiple die. In this application, the aspect ratio limits both the area-efficiency of the wireless interconnect, and the number of layers that can be communicated through.

Previous work has presented wireless inductive data links for multiple die stacking. Because most of them are able to send data to the adjacent layer only due to small *k*, they should relay data transmission to deliver data through multiple dies [67]. This relay method takes a number of cycles to transmit data to the destination, and other layers cannot communicate with each other while the channel is occupied for relaying. In order to solve this problem, a direct transmission method has been proposed [68]. However, this has relied on SIC with extremely large coils to extend the communication range. This chapter will introduce a fabricated IC of a wireless inductive data link for multiple layers using MLSB.

Fig. V.1 depicts how MLSB improves the wireless interconnect of multiple stacked die. In order to deliver data from layer 1 to layer 4, a conventional method delivers data to the next adjacent layer, which then relays it to the next layer, etc., and every relay transmission takes at least one cycle, resulting in the latency of at least four cycles for a 4-layer stack (Fig. V.1(a)) [68][69].

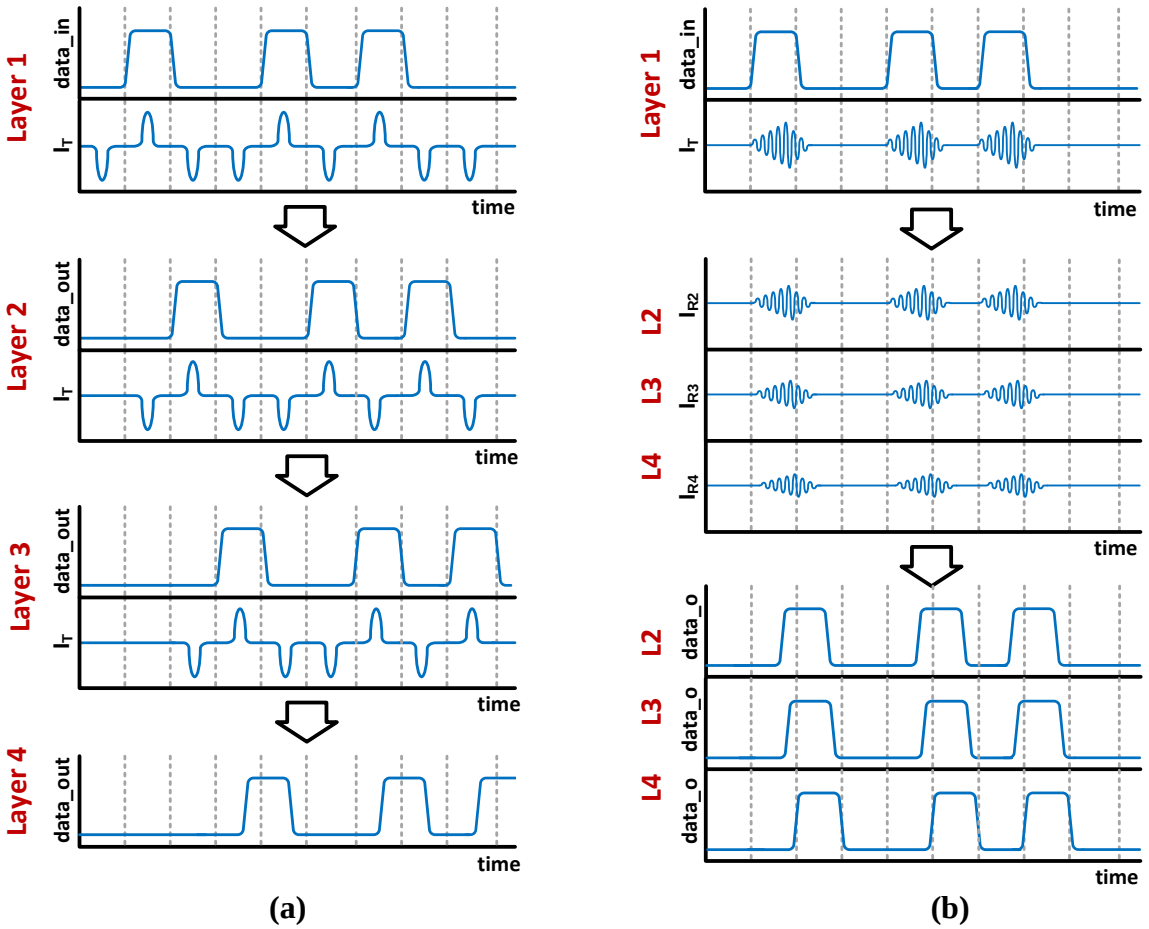


Fig. V.1.Benefit of multi-layer signal boosting. (a) Conventional inductive data link relays data to the next layer (b) Multi-layer signal boosting transmits data using intermediate layers as repeaters

However, in a system utilizing MLSB, data in layer 1 induces signals via RIC (resonant inductive coupling) in all layers at the same time, and these signals are converted to data as depicted in Fig. V.1(b). Even though these signals have a delay

compared to original signal, the total latency to deliver data to the destination is just one cycle.

V.2 Circuit Design

The prototype consists of four vertically stacked dies, and the system has only one vertical inductive data link through all layers. Fig. V.2 shows the overall architecture of the prototype IC and the block diagram of one communication node. Similar to the previous prototype, the communication node works as a transceiver. It can operate in one of three different modes: transmitter, receiver, and repeater. In the repeater mode, the communication node amplifies the received signal and delivers it to the next layer. In this mode, all receiving circuits except the regenerative oscillator are turned off to save power dissipation. The selection among a transmitter, a receiver, and a repeater is programmable.

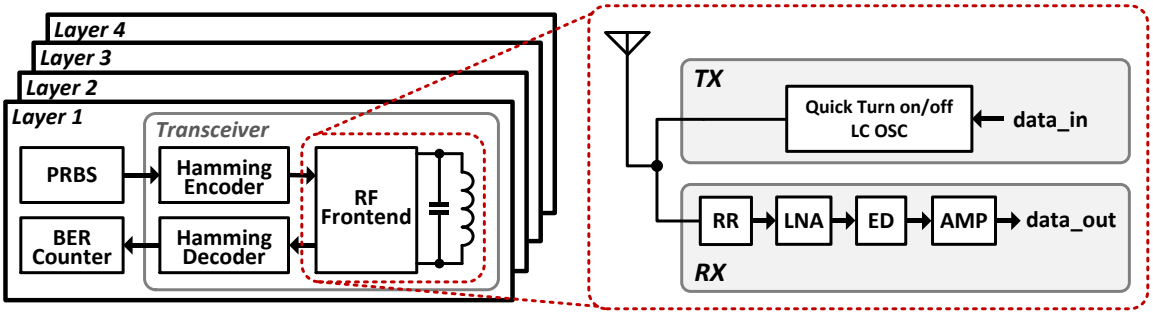


Fig. V.2. Overall architecture of prototype IC.

OOK modulation is used, which transmits multiple RF cycles of current to transmit a '1', and no signal when transmitting a '0'. The transceiver has one inductor used for both communication and to form a LC oscillator tank. It is designed to have a raw data rate of 1Gbps at a 7~8GHz center frequency. Since the oscillator is only active for 7~8 RF

cycles per bit interval, quick turn-on and turn-off circuits are required to generate and detect the signals. For quick turn-on time, a modified cross coupled oscillator is used similar to the previous prototype. However, this prototype does not use a quenching switch for quick turn-off time, because the result of the previous IC shows a quenching switch makes no significant difference despite its overhead. Finally the transceiver includes a Hamming (15, 11) error correction block to improve BER.

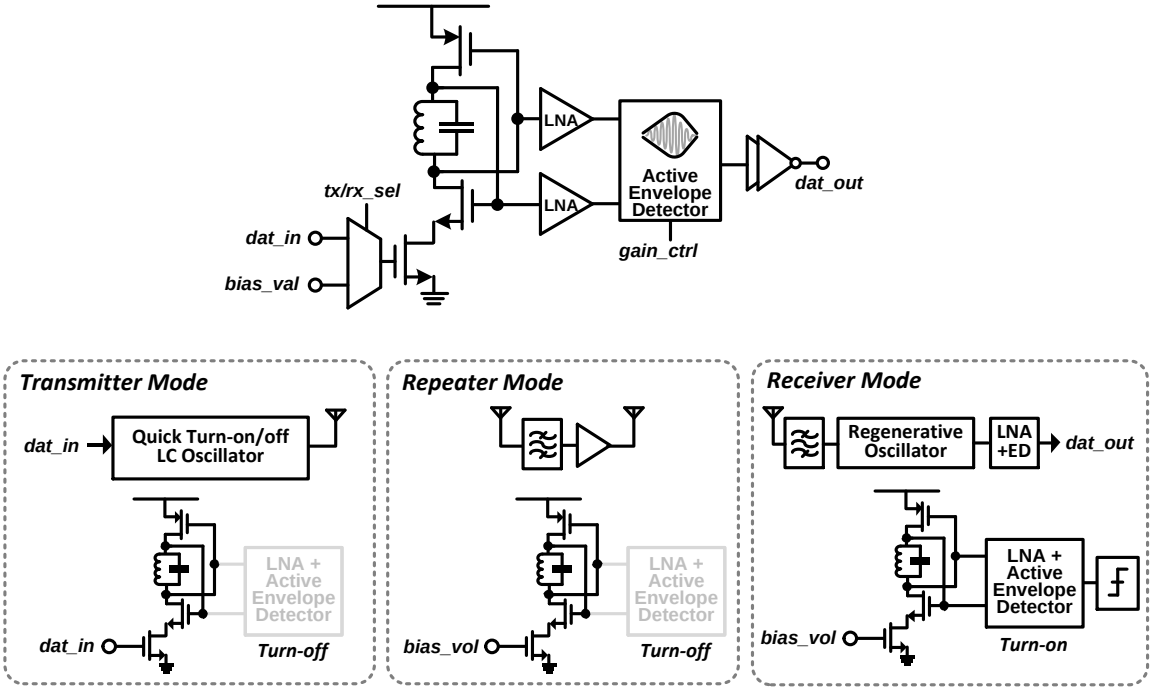


Fig. V.3. Schematic of proposed transceiver and its three different modes.

Adopting MLSB allows a significant reduction in the system complexity. The synchronous comparator that was the most complicated block in the previous prototype is eliminated. Also the quenching switches and power headers are removed, which require thick-oxide transistors. The center-tap of the inductors was removed because it is not compatible with the regenerative receiver. This reduction saves silicon area and power consumption. Fig. V.3 shows the schematic of the proposed transceiver. The oscillator is

controlled by the *tx/rx_sel* signal at the footer. When in transmitting mode, *tx/rx_sel* selects *data_in* as the input signal of the footer. This produces a full-swing oscillation at an LC tank. In receiving mode, *bias_vol* is selected as the input signal, which controls the gain of the regenerative oscillator. The value of *bias_vol* is changed based on the distance to a source node. When the communication distance is short, e.g. from layer 1 to layer 2, *bias_vol* is the smallest. However, *bias_vol* increases when the communication distance is long, e.g. from layer 1 to layer 4. Depending on the distance between the source and destination, the value of *bias_vol* is chosen manually from among four different values. One value is zero, which turns off the receiver as shown in Table X. The variation in *bias_vol* is approximately 50mV. When in repeating mode, all RF circuits except the oscillator are turned off in order to save power and reduce interference. The feedback gain of the regenerative oscillator is controlled by the value of *bias_vol* as well.

Table X. Bias voltage control at each layer when layer 1 is transmitting

Destination	Layer 2	Layer 3	Layer 4
bias_vol @Layer 2	150mV (receiver mode)	260mV (repeater mode)	430mV (repeater mode)
bias_vol @Layer 3	0 (turn-off)	260mV (receiver mode)	430mV (repeater mode)
bias_vol @Layer 4	0 (turn-off)	0 (turn-off)	430mV (receiver mode)

* supply voltage = 1V

Fig. V.4 shows the simulated oscillating current at each layer. The oscillating source current in layer 1 induces current in layers 2-4. The phase difference between the

transmitting current and induced current in layer 2 is 34°, and all induced currents in the receiving coils are in-phase with the total phase difference less than 40°. The smallest current, induced at layer 4, is sufficiently large for being recovered and converted to data.

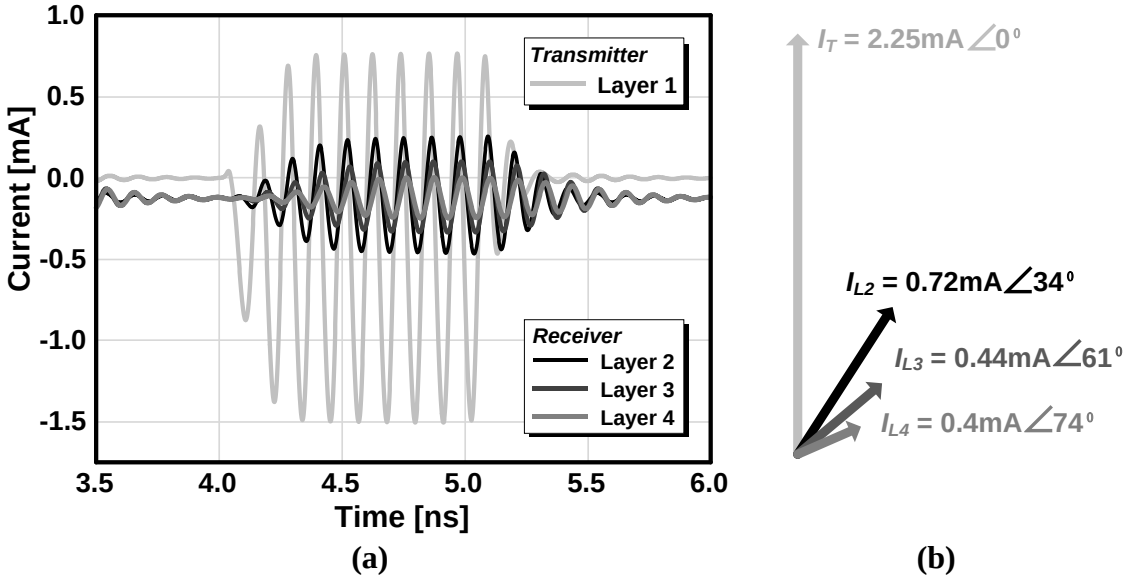


Fig. V.4. (a) Waveform of transmit current at layer 1 and induced current at layer 2-4. (b) magnitude of each current and relative phase.

A prototype was fabricated using IBM CMOS SOI 45nm technology. After fabrication, Advotech performed the post processing such as dicing, thinning, stacking, and packaging the 4-layer 3DIC as shown at Fig. V.5 and Fig. V.6. Each die is thinned with the thickness of approximately 50μm. Including the adhesive thickness, the total distance between adjacent dies is measured to be 54μm with Vecco Daktek 6M stylus surface profilometer. The longest communication distance is from layer 1 to layer 4, and its length is 162μm. The diameter of the coil is 60μm, resulting in an aspect ratio of 2.7:1.

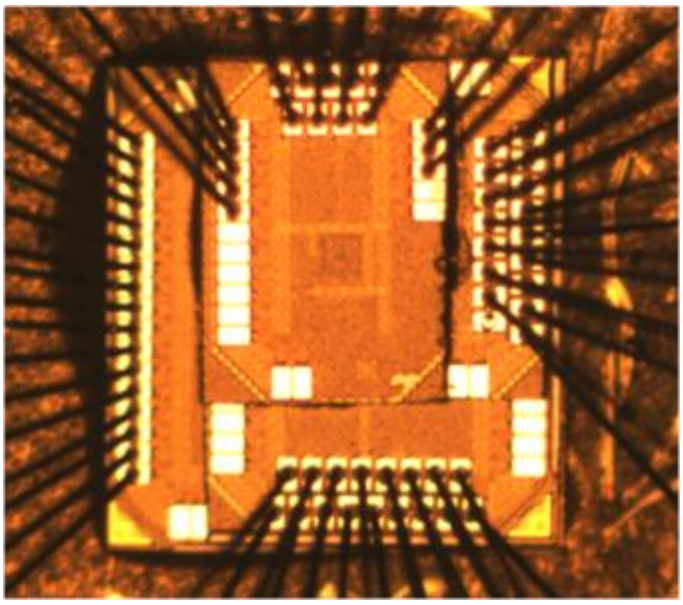


Fig. V.5. Stacked die photo. Total area is 1.12mm x 1.07mm.

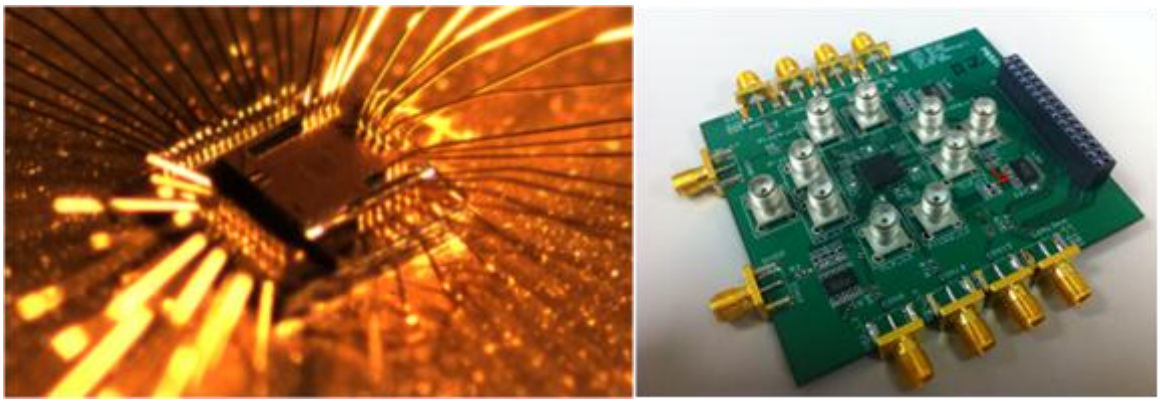


Fig. V.6. Bird-eye's view of stacked die and test board.

V.3 Layout

Since all transceiver circuits are located beneath the coil, the same layout techniques from the previous IC are also applied to this work. Furthermore, this work includes synthesized blocks such as Hamming code decoder and encoder while the previous work has only custom circuits. Those synthesized designs are modified manually after

automatic place and routing so that they can satisfy the additional layout constraints from being directly underneath the coil.

Fig. V.7 shows the layout of the prototype IC. Within the transceiver circuit, the area of the RF circuits takes up approximately 40%, and the digital synthesized block takes the remainder. Since all circuits are located beneath the coil, large metal plates including metal-insulator-metal (MIM) capacitors cannot be used. Instead of MIM capacitors, lateral capacitors and MOS capacitors are used.

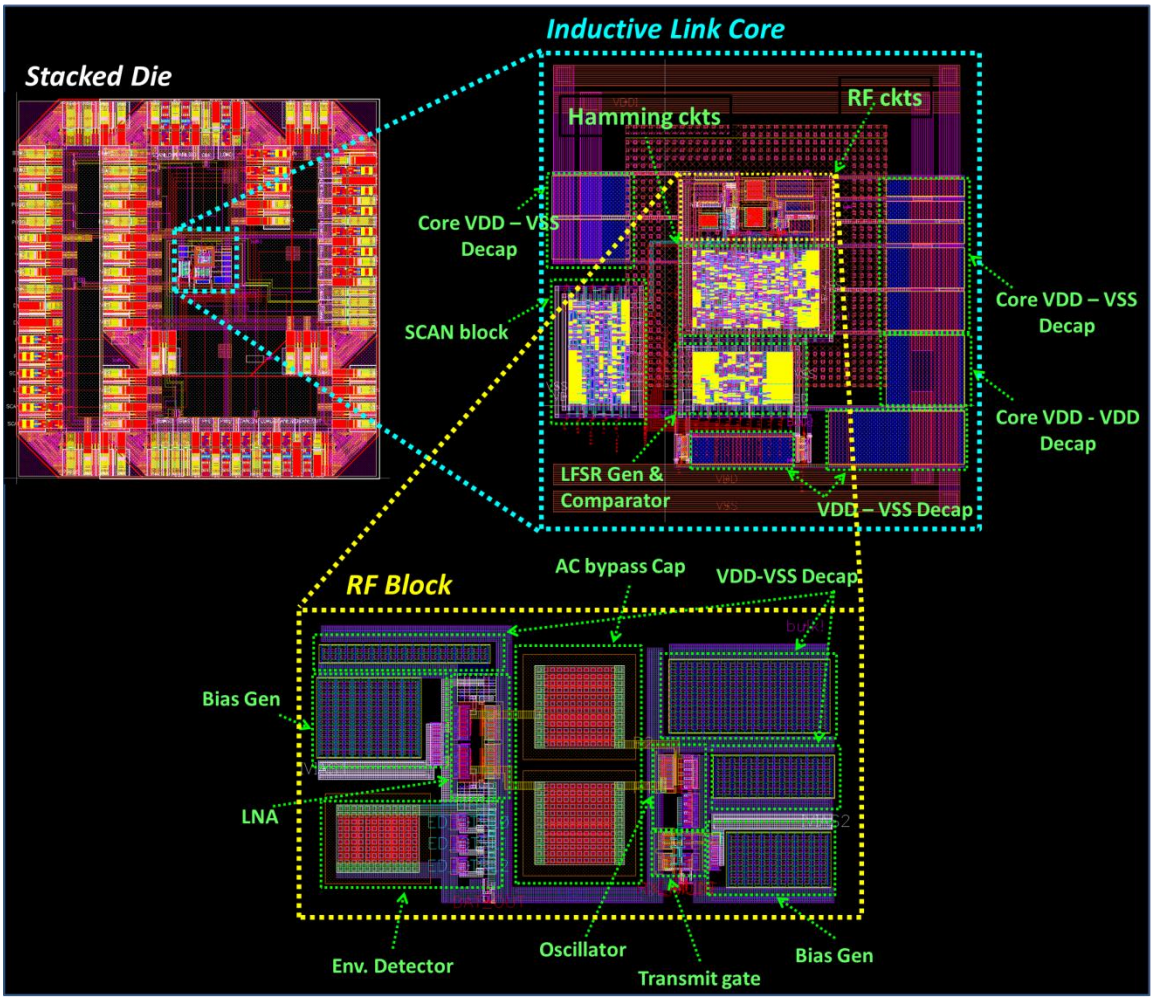


Fig. V.7. Layout.

V.4 Measurement

Fig. V.8 shows the measured BER vs. data rate when layer 1 transmits data to layers 2-4. At a data rate of 807Mbps including Hamming overhead, or a 1.1GHz raw data rate, the BER at layer 4 is measured as $< 10^{-8}$, and a BER $< 10^{-11}$ is measured at layer 2. The bathtub curve at a data rate of 807Mbps is also measured as depicted in Fig. V.9. It shows the allowed worst-case skew between the transmitter and receiver clocks is more than 400ps, nearly half of one clock cycle. For this reason, no additional clock phase alignment circuits are required for demodulation.

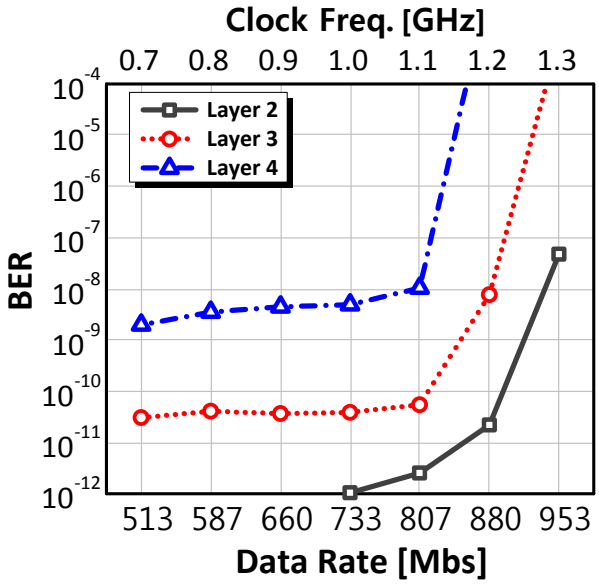


Fig. V.8. Measured BER vs. data rate with Hamming code.

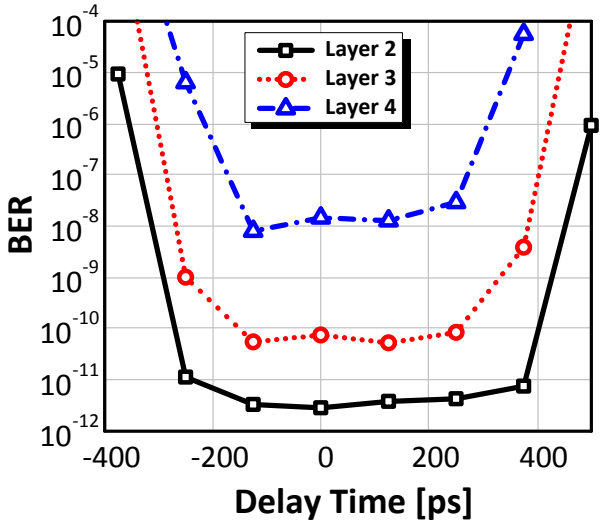


Fig. V.9. Bathtub curve when 807Mbps data rate (=1GHz clock).

The performance summary is shown in Table XI. Compared to other recent works on inductive coupling links intended for multiple-layer communication, this work achieves a x4.5 higher aspect ratio at the maximum distance, using smaller coils and leveraging RIC.

Table XI. Performance Comparison

Parameter	Sugimori ISSCC'09[67]	Saito ISSCC'10[68]	Miura ISSCC'11[69]	This Work		
Technology	Bulk 180nm	Bulk 250nm	Bulk 180nm	SOI 45nm		
Supply Voltage	N/A	N/A	N/A	1V		
Power Diss.	3.2mW*	12.8mW*	2.16mW*	2.1mW/Link**		
Energy Dissipation	1.6pJ/b	6.4pJ/b	0.9pJ/b	2.6pJ/b		
Coil Size	1.1mm	200μm	0.9mm (data)	60μm		
Date rate	2.0Gb/s/ch	2.0Gb/s/ch	2.4Gb/s/ch	807Mb/s/ch		
Bandwidth / Area	1.65G/b/mm^2	50G/b/mm^2	2.96G/b/mm^2	**224G/b/mm^2**		
Thickness / Die	30μm	60μm	25μm	54μm		
Transmission	Across 8 layers	Across 2 layers	Across 2 layers	Across 4 layers		
Max Comm. Range	210μm	120μm	25μm	54μm	108μm	162μm
Max Aspect Ratio	0.19	0.6	0.027	**0.9**	**1.8**	**2.7**
BER	10^{-12}	10^{-12}	10^{-12}	10^{-11}	10^{-10}	10^{-8}

* The power consumption is the total power of a transmitter and a receiver.

** The power consumption is the total power of a transmitter, a receiver and two repeaters.

Chapter VI.
IC for Wireless Power Transfer

VI.1 Introduction

Wireless inductive coupling using planar spirals is compatible with nearly all planar processes, allows communication through multiple IC layers, and enables wireless testing to eliminate the Known-Good-Die issue in 3DICs. Wireless power transfer using inductive coupling has been demonstrated for 3DICs [52][53] and wireless testing [64]. The common drawbacks are the limiting 100mW/mm^2 power density and <0.1 aspect ratio. The links require large coils to transmit sufficient power, and distances less than 1/10th the diameter to maximize the coupling coefficient. This chapter demonstrates a wireless power transfer link with 0.61W/mm^2-power density with a simulated 0.4 aspect ratio in a TSMC 65nm CMOS process. This is achieved by using RIC, operating at higher frequency for increased coupling coefficient, and a cross-coupled rectifier circuit that benefits from the larger voltage as a result of RIC. This chapter presents the design of the inductively coupled link and rectifier, and a comparison with SIC that highlights the improvement due to RIC.

Fig. VI.1 illustrates the concept of stacking 3DICs and using wireless power transfer between layers. Coils are implemented in heterogeneous layers, aligned face-up, and

stacked at the wafer level. After dicing, only the top layer has exposed pads for bonding, and all lower layers are wirelessly connected.

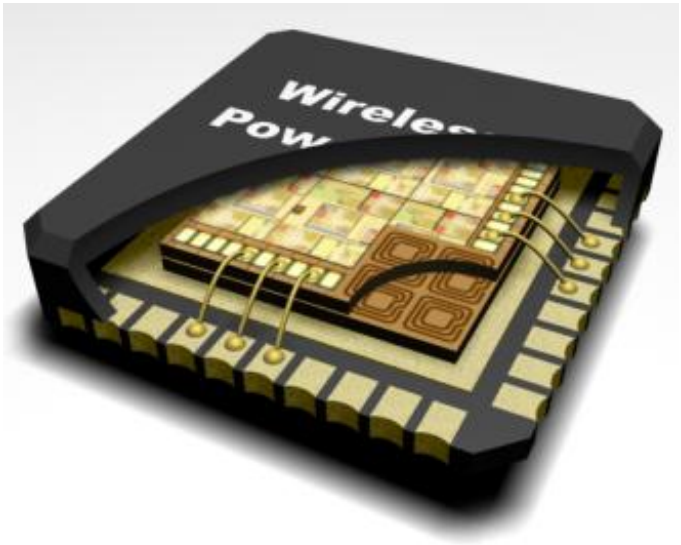


Fig. VI.1. Concept of the wireless inductive power link.

VI.2 Channel Modeling

Operating an inductively coupled system at resonance increases the amount of magnetic flux linked between the coils and enhances the ratio of energy delivered to energy consumed in parasitic resistance in the coils [92]. This results in a significant improvement in power transmission, especially at long distances when SIC coupling is low. In the transmitter, the current I_T and thus the magnetic flux increases by Q times at the resonant frequency of the series LC tank. This results in an xQ larger voltage V_R induced in the receiving coil.

Furthermore, V_R is boosted by a factor of Q at the resonant frequency of the receiver LC tank in Fig. VI.2. Therefore, when the transmitter and receiver resonant frequencies are matched, the received voltage increases by Q^2 times. Because the peak voltage at the

receiver is usually a limiting factor of an on-chip rectifier, the boosted voltage can significantly improve range, aspect ratio, and power density.

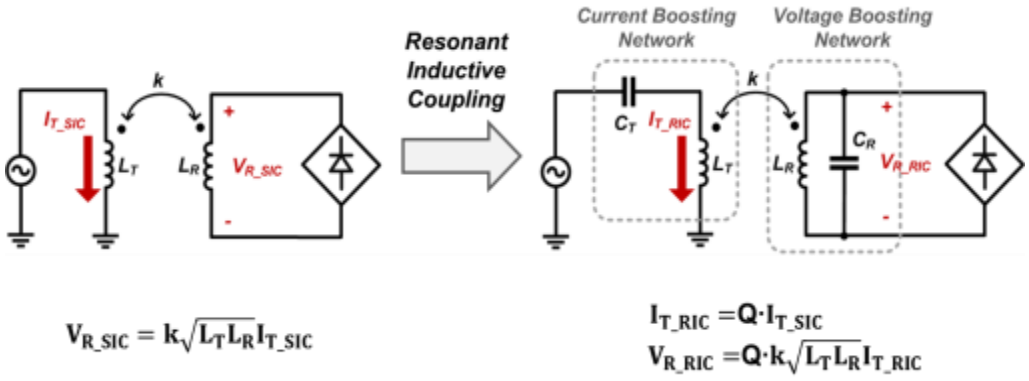


Fig. VI.2. Resonant inductive coupling for inductive power link.

Fig. VI.3 and Fig. VI.4 show how the operating frequency and inductor size are selected in order to maximize power density. The power available at the receiver is proportional to V_R^2, and V_R is proportional to frequency for current-limited inductive links. Therefore, the available power is proportional to ω^2. The power loss depends on V_R, ωC_{sub}, and R_{sub}. Since V_R and ωC_{sub} are functions of frequency, the power loss is proportional to ω^4, which presents an optimum operating frequency [93]. The net available power after subtracting the loss shows a peak at 4.5GHz. However, the highest power efficiency occurs at 3.5GHz. This is selected as the operating frequency, and an inductor is designed so that it has the peak *Q*-value at 3.5GHz. With fixed separation, larger coils will have a higher coupling coefficient *k* and may typically deliver more power. However, larger coils have lower self-resonant frequencies and higher C_{sub}, which means they cannot fully utilize the advantage of high frequency and will have more power loss at the same frequency. To avoid these problems, the inductor size is reduced, decreasing *k* as well.

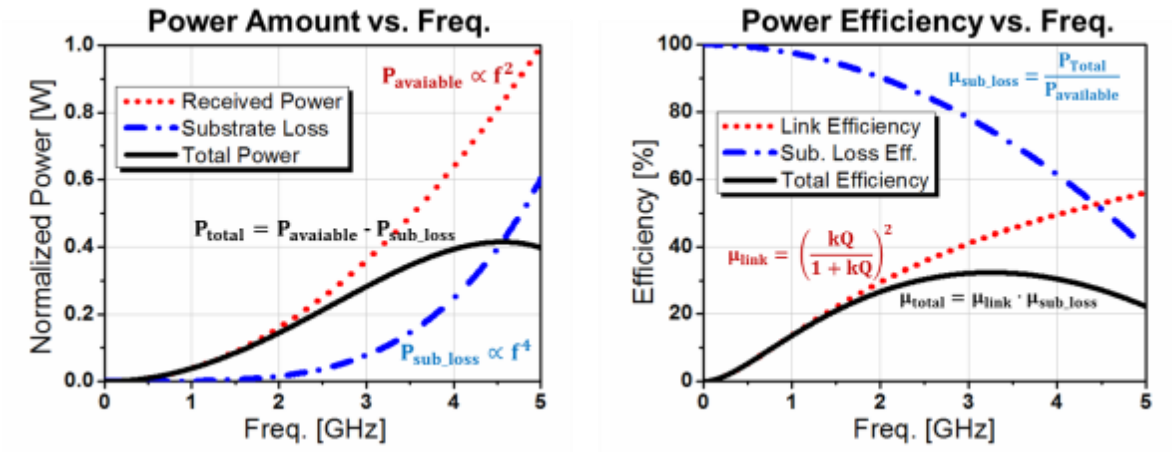


Fig. VI.3. Frequency analysis of the inductive power link for the high frequency operation.

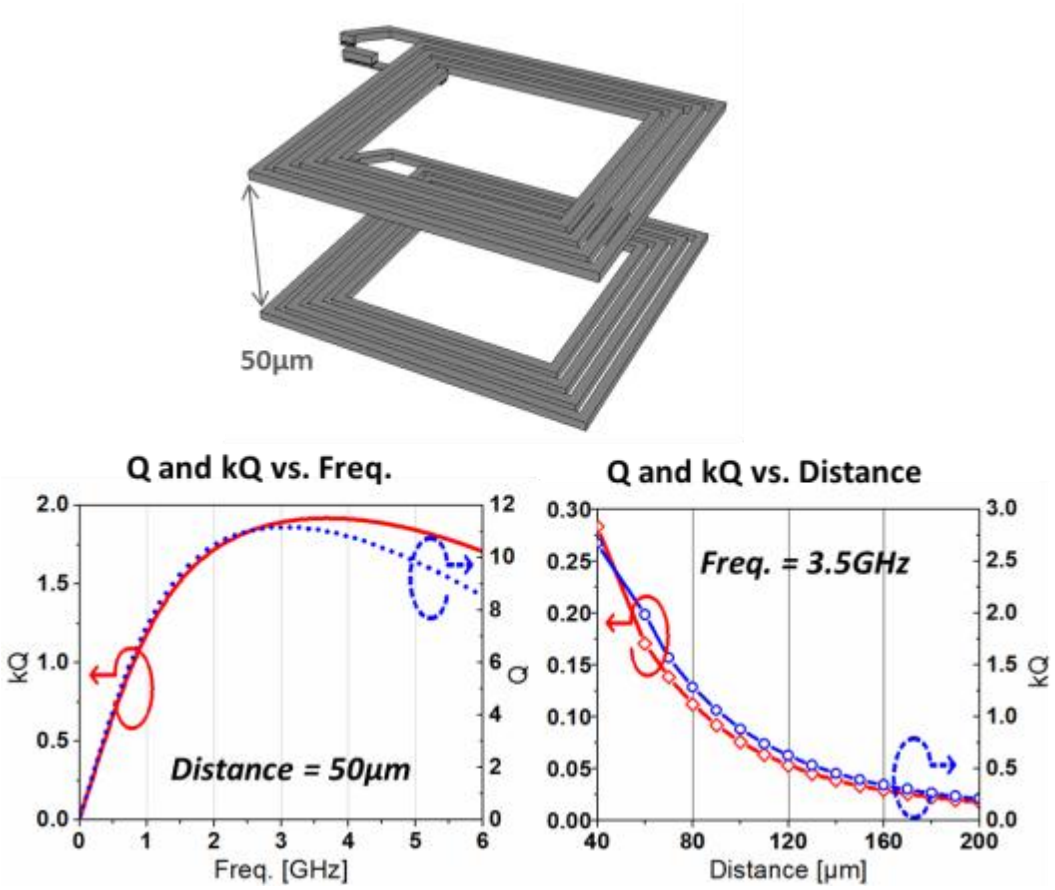


Fig. VI.4. Frequency analysis of the inductor design.

However, from [92], the RIC link efficiency is a function of kQ, therefore a large Q-value can overcome the smaller k due to the reduced coil size. A simulated Q-value of 11 is achieved by using ultra thick metal and an un-doped p-substrate with no-metal fill around the coil. In a 3DIC application, the coupled coils are designed to have a k of 0.18, which leads to transmit and receive coils that are 120μm x120μm with 50μm separation. The simulated value of kQ is 1.98, resulting in a link efficiency of 44%.

VI.3 Circuit Design

A block diagram of the power transfer circuit is shown in Fig. VI.5. Unlike previous links reported in literature, it has LC tanks to implement RIC: a series LC tank to boost current in the transmitter and a parallel LC tank to boost voltage in the receiver. Two different rectifier circuits are implemented. The typical diode-connected rectifier is made as a benchmark circuit, and a cross-coupled rectifier is proposed for higher performance. Both circuits operate at 3.5GHz and use RIC. The transmitter is implemented with a discrete capacitor and wire-wound spiral coil tuned to 3.5GHz, and mounted on a probe station to control its position precisely over the receiver. This demonstrates powering a receiver IC in a wireless testing environment. Simulation results are presented for a transmitter IC using a matched planar spiral for stacked die applications.

Synchronous rectifiers using comparators or DLLs have been proposed to account for the small received voltage in SIC links, but at frequencies limited to less than 1GHz, so they are not suitable for RIC frequencies [64]. Because of the Q^2 times boost in received

voltage from RIC, even a diode rectifier combined with RIC exceeds the performance of these designs.

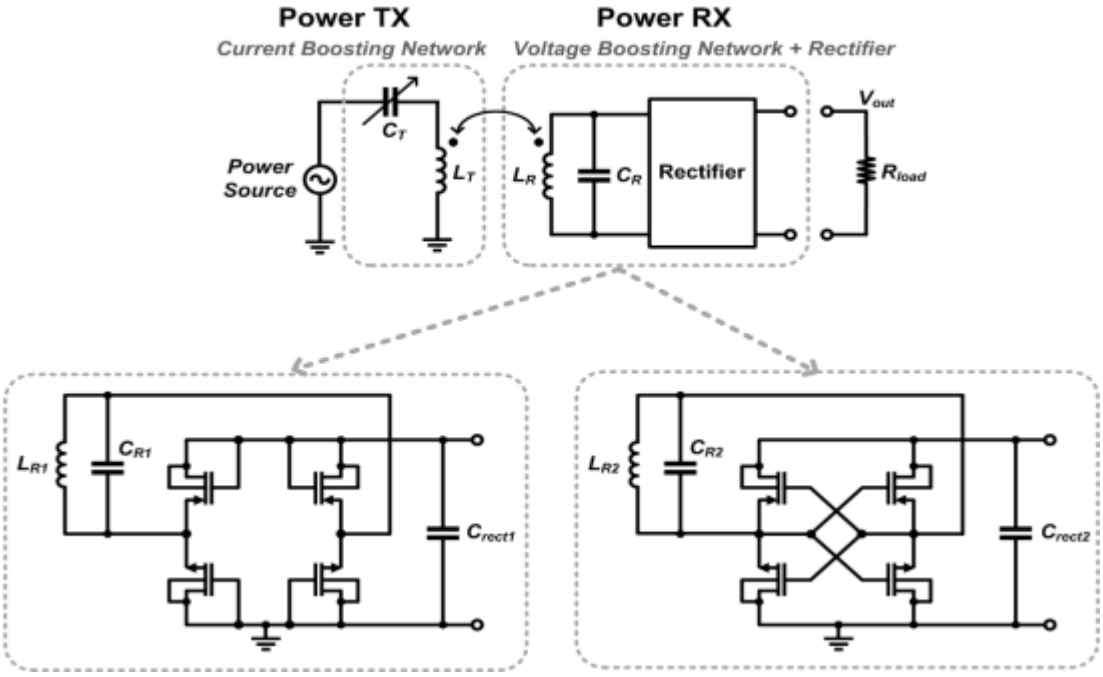


Fig. VI.5. Schematic of the wireless inductive power link with resonant inductive coupling.

Fig. VI.6 shows the advantage of the boosted voltage in terms of the current flow. With standard inductive coupling, the nMOS and pMOS channels are weakly depleted, which limits the rectified current. In a diode-connected rectifier with RIC; however, the high voltage enhances not only the channel current but also PN junction forward current. The total current is more than 8 times compared to SIC. Finally, the proposed cross-coupled rectifier further increases V_{GS}, increasing the channel current. This results in a 30% improvement compared to a diode-connected rectifier with RIC and overall 9 times improvement compared to SIC.

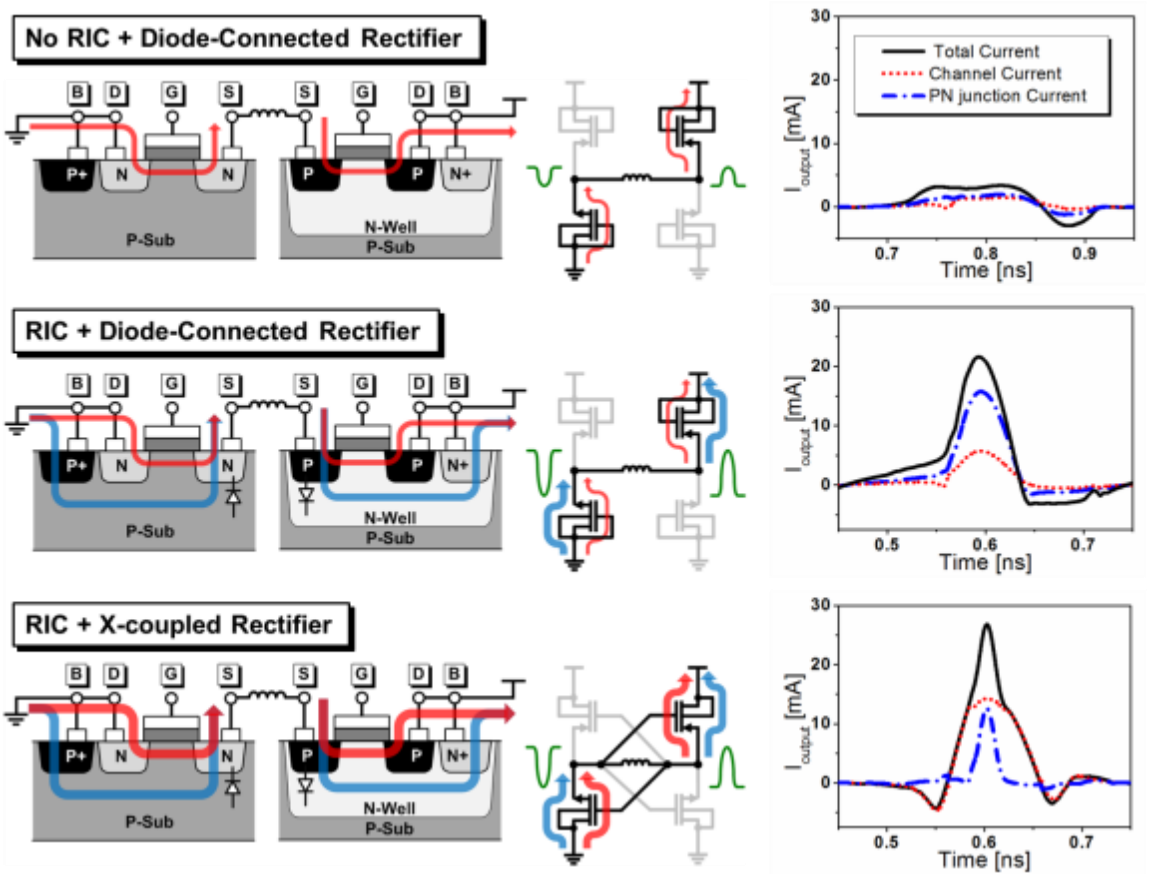


Fig. VI.6. Current breakdown of the rectifier topologies with and without resonant inductive coupling.

Three different circuits are fabricated in TSMC 65nm CMOS process with ultra-thick metal and MIM-cap options. All circuits use the same inductor design, with a size of 120 x 120μm^2. The rectifier circuits are implemented adjacent to, rather than underneath, the receiving coils, to prevent a decrease in the inductor *Q*. The rectifiers add an additional area of 0.008mm^2. Their die photo is shown in Fig. VI.7.

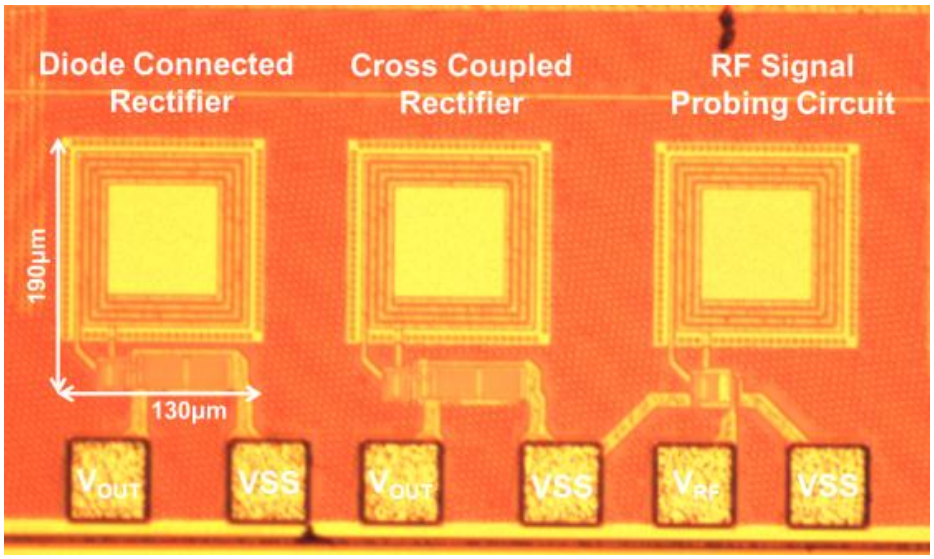


Fig. VI.7. Die photo

VI.4 Measurement

The inductive power links are tested on a probe station as shown in Fig. VI.8. The power is externally supplied to the transmitter by a signal generator. A transmitter is implemented with the series connection of a surface mounded device (SMD)-type capacitor and a wire-wound spiral coil. The coil size is around 200μm and has 3 hand-wound turns with 80μm-thick wire. The resonant frequency of the *L* and *C* is 3.5GHz, which is tuned to the same frequency as the receiver coil for implementing RIC. The transmitter is mounted on the probe station so that its position in the x, y, and z-axes can be controlled precisely to overlap the coils each receiver circuit. This transmitter demonstrates wirelessly powering the circuit for e.g. wireless testing. Fig. VI.9 shows photos of transmitting coils over three receiving circuits and measurement results of the transmitting coil.

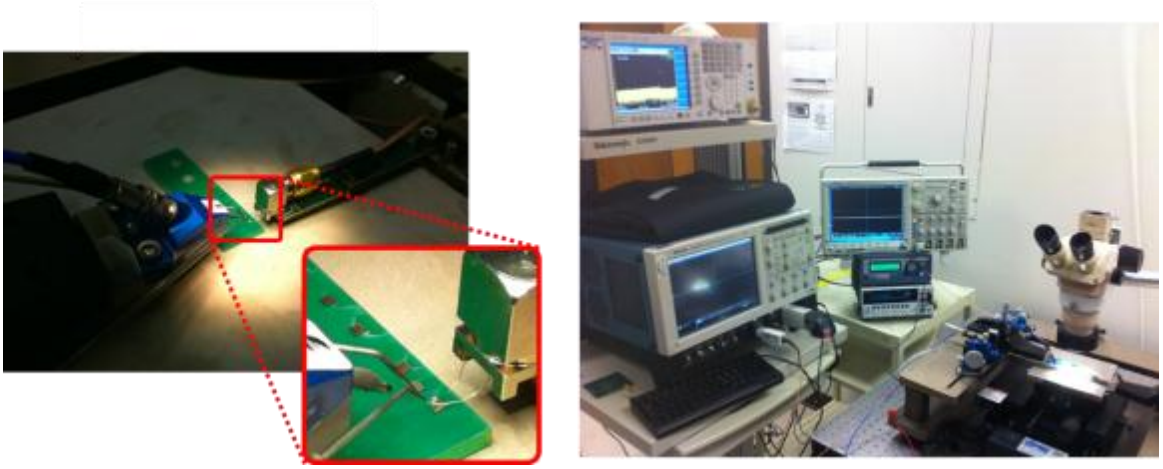


Fig. VI.8. Measurement Setup

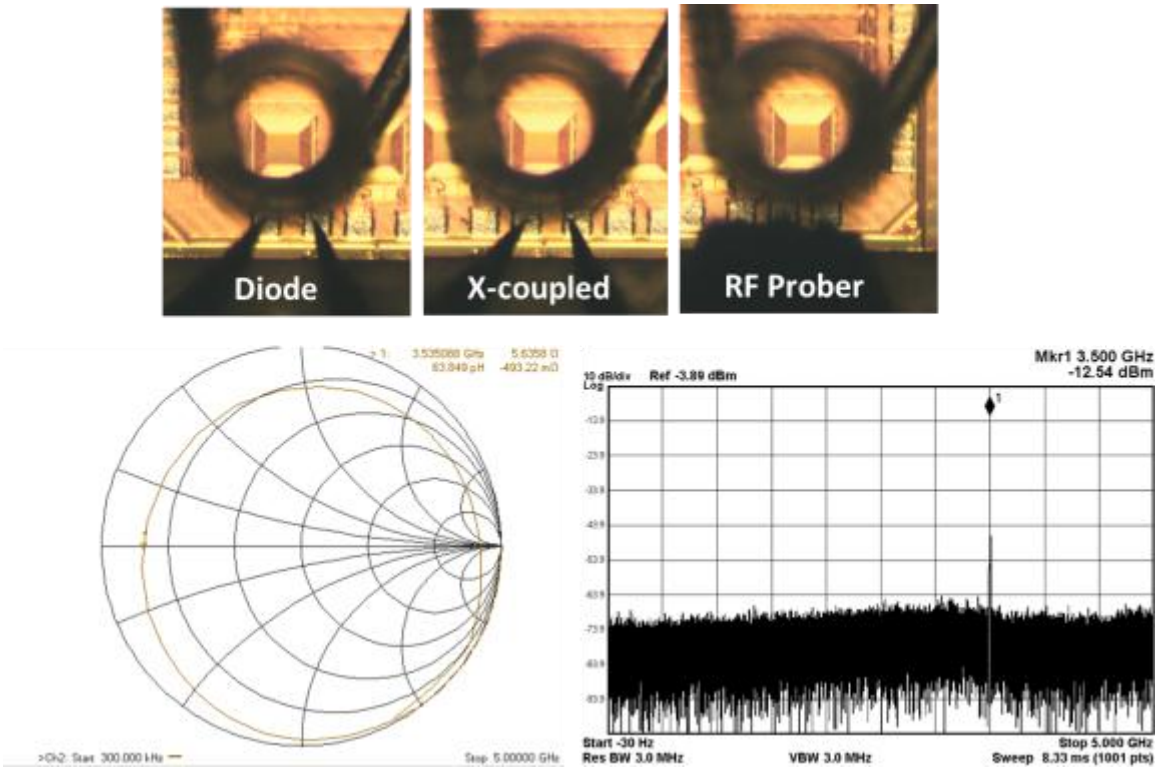


Fig. VI.9. Aligned transmitting coils and the measurement results.

The improvement due to RIC is measured by comparing to a benchmark circuit on the same chip, which has the same LC tank and a high frequency buffer. Fig. VI.10 shows the measurement result of the RIC improvement over a half-SIC link. Because all circuits share the off-chip transmitter, the half-SIC also uses the LC tank in the transmitter, but does not implement a resonant tank in the receiver. RIC shows a more than 3x larger voltage peak at the resonant frequency than the half-SIC link.

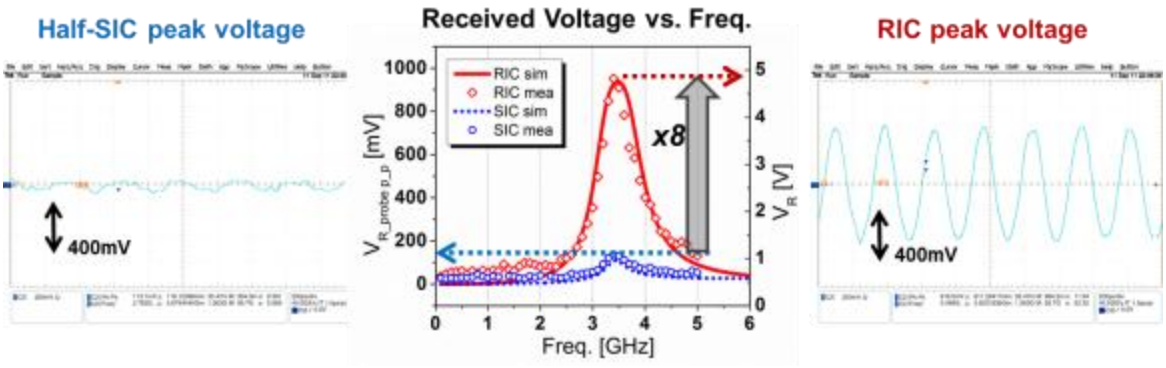


Fig. VI.10. Benefit of resonant inductive coupling with simulation and measurement results.

For both rectifiers, the maximum power is achieved at the resonant frequency of 3.5GHz and a load resistance of 310Ω, as depicted in Fig. VI.11. The maximum power of the cross-coupled rectifier is 15mW, resulting in a power density of 1.04W/mm^2 considering the coil area alone, and 0.61W/mm^2 including the rectifier circuit. The diode rectifier achieves 13.7mW, and both use RIC in the transmitter and receiver. Fig. VI.12 show a performance summary of this work. Compared to previous publications, this prototype achieved an 4x power density and an 4x aspect ratio.

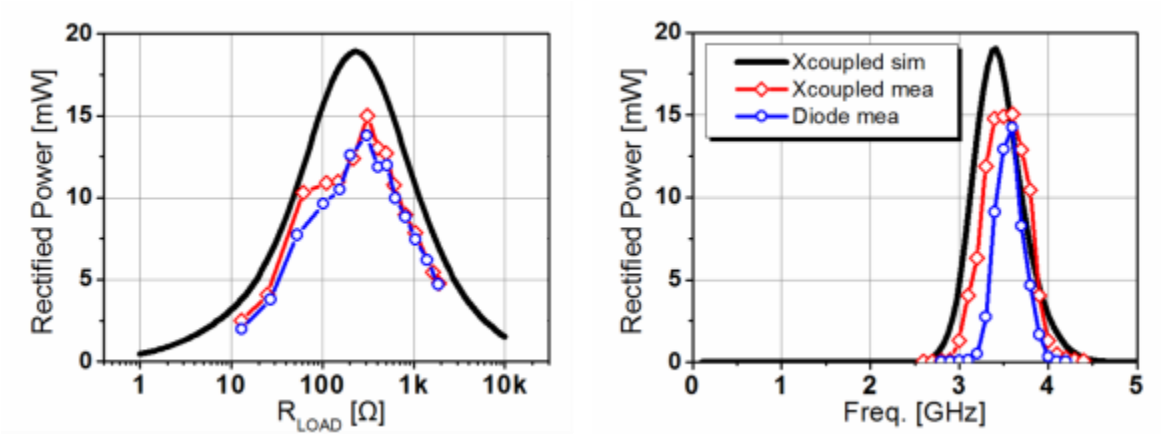


Fig. VI.11. Measurement results depending on load resistance and frequency.

Table XII. Performance Comparison

	This Work	Onizuka CICC '06	Yuan VLSI '09	Yuan VLSI '10	Radecki ISSCC '11
Received Power	15mW	2.5mW	14mW	10mW	6W
Coil Size	0.12x0.12mm^2	0.7x0.7mm^2	2x2mm^2	0.7x0.7mm^2	5x5mm2
Distance	50µm	n/a (<20µm)	200µm	20µm	50~320µm
Aspect Ratio (Distance/Coil Size)	**0.42**	<0.029	0.1	0.029	<0.064
Power Density	**1.04W/mm^2 (Coil only) 607mW/mm^2 (All Circuits)**	5.1mW/mm^2	2.5mW/mm^2	20mW/mm^2	240mW/mm^2
Power Efficiency	19%	-	4.1%	10.2%	17%
Carrier Frequency	3.5GHz	150~350MHz	250MHz	-	150MHz
Technology	65nm CMOS	0.35µm CMOS	0.18µm CMOS	65nm CMOS	0.18µm CMOS

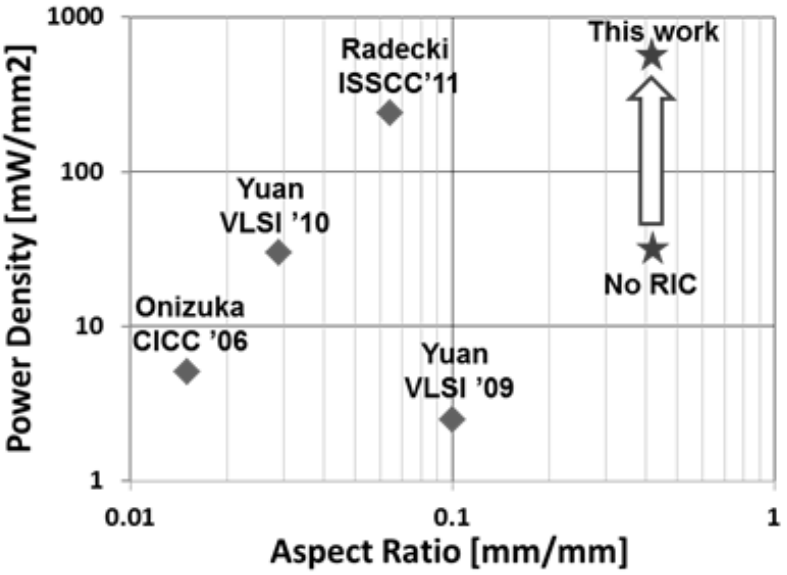


Fig. VI.12. Performance Comparison.

Chapter VII.
Conclusion

VII.1 Summary

As the demands on high performance and multi-function systems increase, vertically stacked 3DICs have the advantages of a small form-factor and short communication distance between chips, leading to high data rate and low power consumption. Several wired and wireless approaches for interconnect between 3DICs have been proposed. Among them, wireless interconnect using inductive-coupling and wired interconnect using TSVs are very promising since they have achieved low power, high performance with small size, and operate across heterogeneous ICs and technologies. This thesis has characterized the TSV proximity effect due to thermal stress and investigated ways to improve a wireless inductive coupling link by achieving higher aspect ratio with low power consumption.

The proximity effect of Tungsten-filled TSVs on the threshold voltage change and mobility shift of CMOS devices due to mismatch in thermal expansion coefficients is modeled and verified with measurements. Test structures fabricated in a 2-layer 130nm CMOS 3DIC process are measured and compared with 3D FEM simulations. The impact of a single TSV on active devices with different channel widths and lengths and different distances to a TSV is evaluated. No shift was observed in V_{TH} or electron mobility,

however hole mobility increases for channels oriented tangential to the TSV. Results indicate threshold voltage is not affected by TSVs, while mobility is affected by as much as 10% for devices placed within 4μm of a TSV. A keep-away-zone of 4μm should be considered for minimal impact on device performance.

The performance of inductive links can be improved by using RIC over SIC. RIC can increase the received voltage by a factor of Q^2 in the weakly coupled regime and $2Q$ in strongly coupled regime compared to SIC. Therefore, RIC can be exploited for wireless links with small k to extend the communication distance between coils without increasing the coil size or power consumption. The first prototype of wireless communication links was fabricated to demonstrate RIC using a Global foundry 130nm CMOS process. The system is a 2-by-2-by-4 router over four layers, and each layer has a 2-by-2 coil array. The prototype achieves 1Gbps data rate and 2pJ/b with coils of 30μm-diameter.

RIC can be used for wireless power transfer to increase the power density and aspect ratio. When an inductive power transfer system operates at resonance, the amount of magnetic flux linked between the coils is increased, and this enhances the power transfer efficiency. In addition, considering both of delivered power amount and substrate loss depending the operating frequency, the optimal point to maximize the total available power exists. The prototype fabricated in TSMC 65nm CMOS process shows a power density of 0.61W/mm^2 and an aspect ratio of 0.42 are achieved.

Finally, a new signal boosting scheme for wireless inductive interconnects in 3DICs is proposed. It enables longer distance communication through multiple-stacked layers without increasing coil size by using in-phase resonant inductive coupling and

regenerative oscillation. A second prototype of an inductive data link was fabricated in an IBM SOI 45nm CMOS process to demonstrate the multi-layer signal boosting scheme. It achieves a data rate of 807Mbps at a distance of 162μm across 4 IC layers with coils whose diameter is 60μm. This is a x4.5 higher aspect ratio compared to other inductive data link targeting multiple stacks.

VII.2 Future work

In the future, this work can be developed into two different directions.

- Highly integrated 3DICs. The inductive data link using MLSB can be exploited in 3D multi-core system with multiple access scheme discussed in Appendix. B. When the inductive data links are used as parallel vertical buses, the crosstalk should be analyzed. An inductive link also can be applied to very small integrated system such as cubic mm. If both of power and data are transmitted using inductive coupling, all of the wirebonding pads on the perimeter of each die can be removed, and the whole system can be a perfectly cube-shaped. The size of coils for power transfer should be maximized in order to increase power efficiency. This can be achieved by increasing the power coil almost as large as the die size and locating the data coils inside of the power coil. The data should be transmitted differentially to cancel the common magnetic flux from the power coil.
- Bio applications. Eventually when TSVs become as ubiquitous as the planar CMOS processes, it is difficult for wireless interconnect methods to compete with TSV technology except in very limited applications such as Information Tethered Micro Automated Rotary Stages (ITMARS) [94]. However, inductive coupling links can be

used extensively in biomedical applications instead of in 3DICs. Since magnetic fields have less impact on a human body compared to electric fields, inductive coupling can be used for short-range non-contact communication or power delivery. Moreover, off-chip inductors with very high *Q*-factor will extend the range of communication or power transfer even with small *k* using RIC and MLSB. Even though very high *Q* factor can degrade the data rate, it is no significant issue for bio application.

Appendix A.
Tezzaron Process

Appendix A. 1 Tezzaron 3D Process Description

A 3DIC using wireless interconnect requires no additional fabrication process, but it also needs special post processing such as dicing, thinning and stacking after the fabrication. The thinning process is necessary to reduce the communication distance, and stacking with precise alignment is important for wireless interconnect as well. While such post processing is common at the wafer level in industry [88], it is not easy to achieve at the single die level, and the handling of thin die could lead to failures in the chip. Therefore, this first prototype was implemented in a Tezzaron Multi-Project Wafer (MPW) process, which uses Global foundry CMOS 130nm technology plus a TSV technology. Because this process includes wafer-level thinning with the thickness of 12μm and stacking with less very fine alignment (≤1μm), it provides a very good opportunity for implementing and testing the wireless interconnect. In addition, TSVs are used as signal paths for testing.

The Tezzaron process has 1 polysilicon layer, and 6 metal layers (1P6M), however the last metal layer is reserved for wafer-to-wafer connections. Therefore, only five metal layers are available for design and all of them are thin metal layers intended for digital routing. The thickness of the back-end-of-line (BEOL) is typically 6μm. The silicon

substrate thickness is originally more than 700μm but is thinned to 6μm to expose TSVs to the back side of the wafer. As a result, the total thickness of one layer becomes 12μm. One layer is connected face-to-face to another layer via copper thermal bonding using the top metal layers. This forms a face-to-face two-layer stack. This stack is then connected to another face-to-face stack using exposed the TSVs and copper thermal bonding between TSVs. This is a back-to-back stacking of two two-layer stacks and results in a total four-layer stack. Fig. A.1 visualizes the Tezzaron process and four-layer stacking structure. Coupled inductors and transceiver circuits were designed within this metallization option.

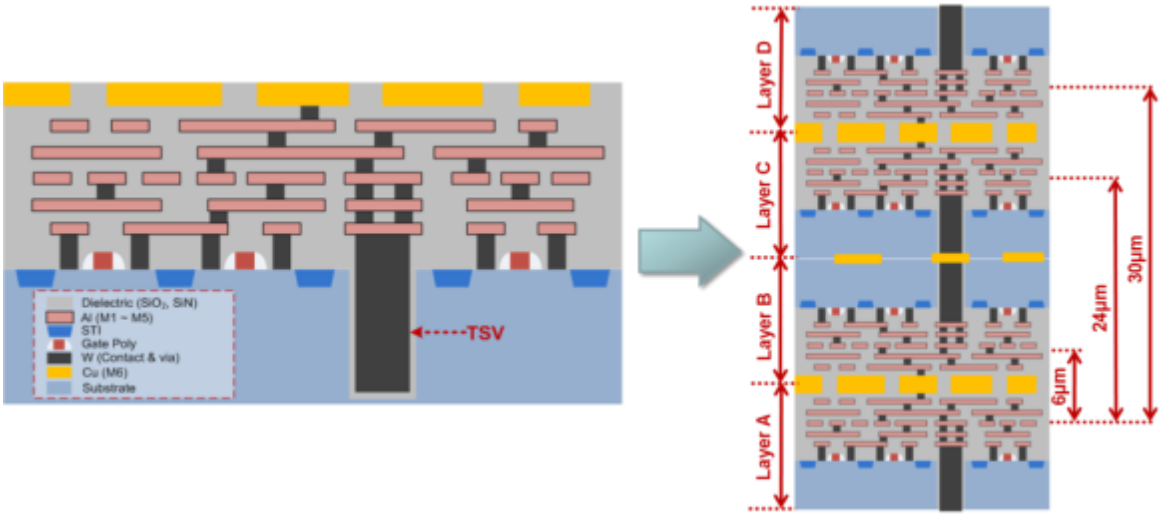


Fig. A.1. Cross-section of Tezzaron TSV Process and 4-layer stacking.

Appendix A. 2 3D LVS

The verification of 3DICs using TSVs requires a new design flow for the design rule check (DRC) and Layout-Versus-Schematic (LVS), which is different from conventional planar CMOS processes. In the case of DRC, it is not a significant change because in this

case the 3DIC can be treated as a combination of multiple planar dies, and every planar die could be checked separately using the conventional design rules except for the TSV-related design rules. The design rules for the TSV would nominally be provided by TSV manufactures and be fully compatible with conventional computer aid design (CAD) tools such as Calibre DRC. Unlike DRC, LVS cannot be performed with an individual layer-based method. Because all layers are electrically connected together, the schematic of the whole system should be compared across all layers of the system at the same time. In other words, three dimensional LVS (3D LVS) is necessary. However, the conventional CAD tools are unable to support three dimensional LVS, and new tools for 3DIC design are not mature yet.

For the prototype IC designed in the Tezzaron process, several 3D LVS methods were proposed. All of them are using the conventional CAD tools Calibre LVS, rather than new 3DIC design tools. The most intuitive way is to add labels on the vertical connections. In the Tezzaron process, every die has a pattern of uniformly distributed micro metal points (Supercontact^{TM}) on both sides of the top and bottom layers for wafer-bonding. When two layers are stacked, all of the metal points on one layer are connected to the matching metal points on the other layer. All vertical connections are through these metal points, and TSVs should be positioned on the metal points. By adding labels on all metal points of one layer and adding the same labels on all metal points of the other layer, 3D LVS can be performed on side-by-side layouts since Calibre LVS recognizes the two nets having the same net name as one connected net in the layout. There are, however, too many metal points in a design, approximately 1,000 points across an area of 1mm x

1mm. For a large design, it is impossible to add labels on every metal point manually or by using scripts due to limited time and memory of machines. To alleviate this, a method of finding the metal points with actual electrical connections and adding labels only on them only is proposed.

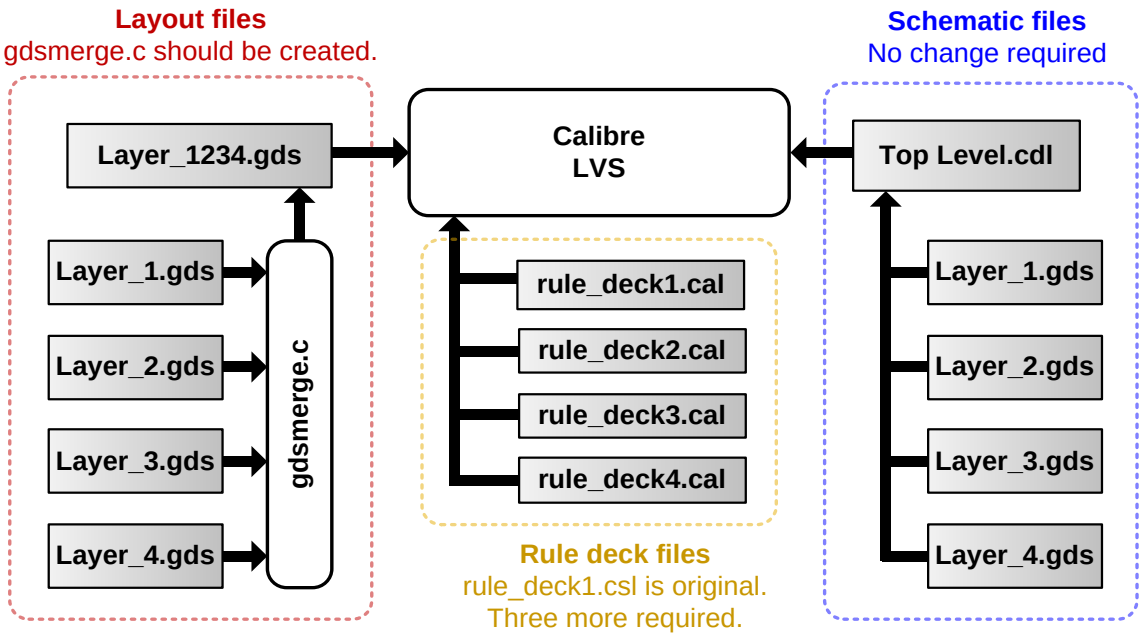


Fig. A.2. Flow of proposed LVS.

However, the partial labeling method still takes significant time and resources for large designs. Moreover, the labels should be generated again when the position of any vertical interconnection is modified. To resolve this problem, a 3D LVS method comparing one merged layout to the schematic is proposed. This method uses C programs to merge multiple streams of files into one integrated gds file as visualized in Fig. A.2. When Calibre LVS compares this merged gds file with the top level schematic, it requires the same number of rule deck files as layers. rule_deck1.cal is the original rule deck file of a conventional planar process, and it has the information on electrical connections

inside layer 1. Other rule deck files are modified versions based on the original rule deck file. They have the information on not only connections inside their corresponding layers but also electrical connections to adjacent layers.

Fig. A.3 shows how to merge gds files into a single gds file. The multiple C programs are used sequentially, and *n-1* different C programs are necessary for *n*-layers. Any intermediate gds file (e.g. Layer_12.gds, Layer_123.gds) could be used for partial LVS.

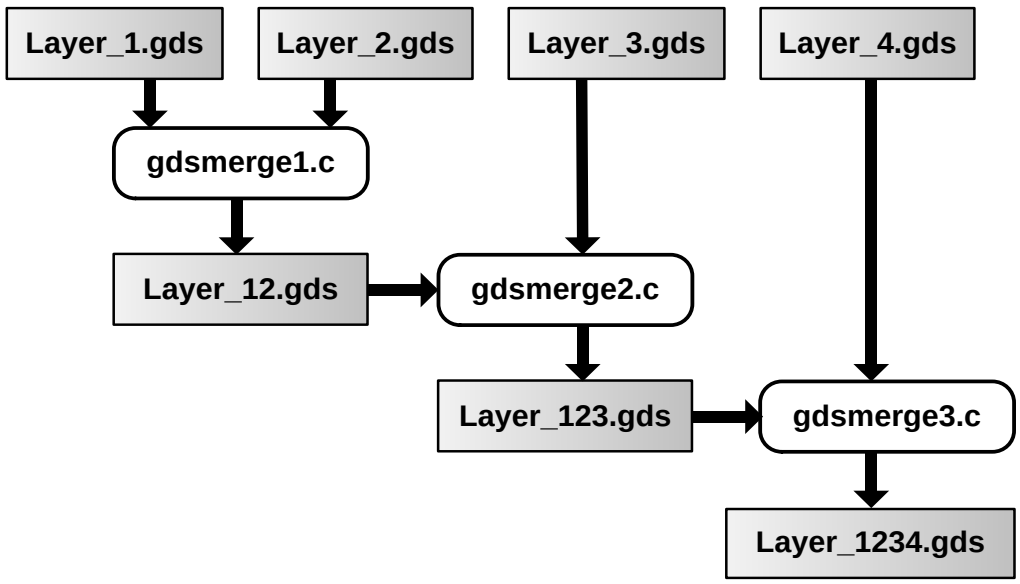


Fig. A.3. Flow of combining gds files.

Appendix B.
Multiple Access using MLSB

Appendix B. 1 Motivation

The inductive coupling channels proposed in Chapter V can be used in a multiple stacked system as shown in Fig. B.1. Each layer has a core, caches, and several vertical wireless inductive links. Every core can access any cache on the other layers via parallel inductive data channels. All cores share one vertical wireless channel to control data channels. However, more than two cores might access the shared control channel simultaneously, and a collision will occur. A proper multiple access scheme is required to avoid collisions among cores and improve the performance of a many-core system.

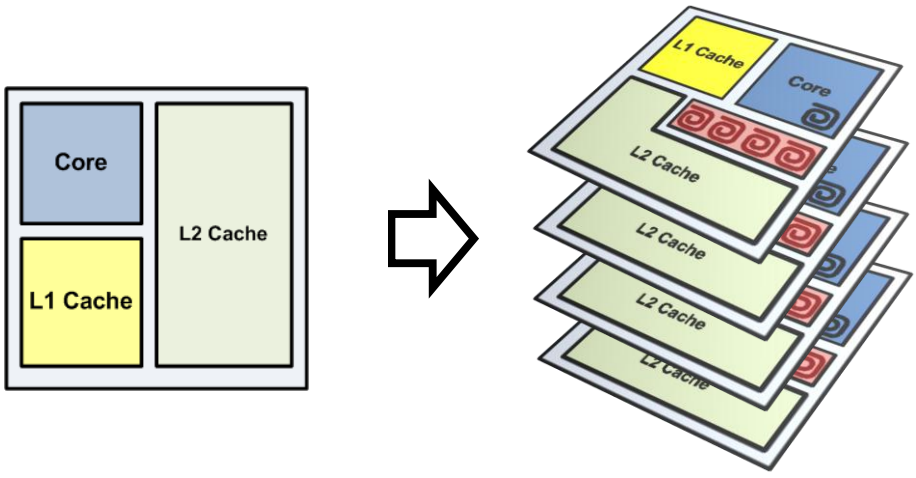


Fig. B.1. Motivation of multiple access in stacked dies.

In order to choose an appropriate multiple access scheme, the features of the proposed inductive data links should be considered. First of all, every terminal is a transceiver, which means it can operate either as a transmitter or receiver. Next, only half duplex communication is possible. While code division multiple access (CDMA) or frequency division multiple access (FDMA) enables full duplex communication, they will increase circuit complexity significantly. Therefore, in a vertical communication channel, only one transmitter can send data at any given time. Because the terminal is unable to detect data while it is transmitting a signal, it is difficult for the terminals to notice a collision. In order to avoid collisions, a time slot when only the designated terminal can send data should be assigned fairly. Time division multiple access (TDMA) satisfies this condition, but it could be inefficient when a few terminals access the channel intensively. Another candidate is carrier sense multiple access (CSMA). However, it should be modified to be combined with inductive coupling links.

Appendix B. 2 Study of Conventional Multiple Access Methods

Fig. B.2 shows how a typical carrier sense multiple access / collision avoidance (CSMA/CA) works with random back-off time. There are five stations sharing a channel. Each station desiring to transmit will generate a random back-off period before transmitting. After that step, all stations should check if the channel is idle. If the previous transmission was correctly completed, all stations see an acknowledge (ACK) frame. Once received ACK, they have to hold during distributed inter frame space (DIFS). If the previous transmission was not successful, stations see no ACK frame. Then, they

must hold during extended inter frame space (EIFS) since the last successful frame. When either of two conditions is satisfied, all stations determine the channel is no in use. If the channel is idle, a station to transmit must wait for the previously generated back-off time further. The back-off time is generated randomly between 0 and contention window (CW) time. In the case of no communication activity in the channel, the back-off timer will decrease by one. If the channel is busy, the timer does not decrease. When the back-off timer reaches 0, the station can transmit a frame.

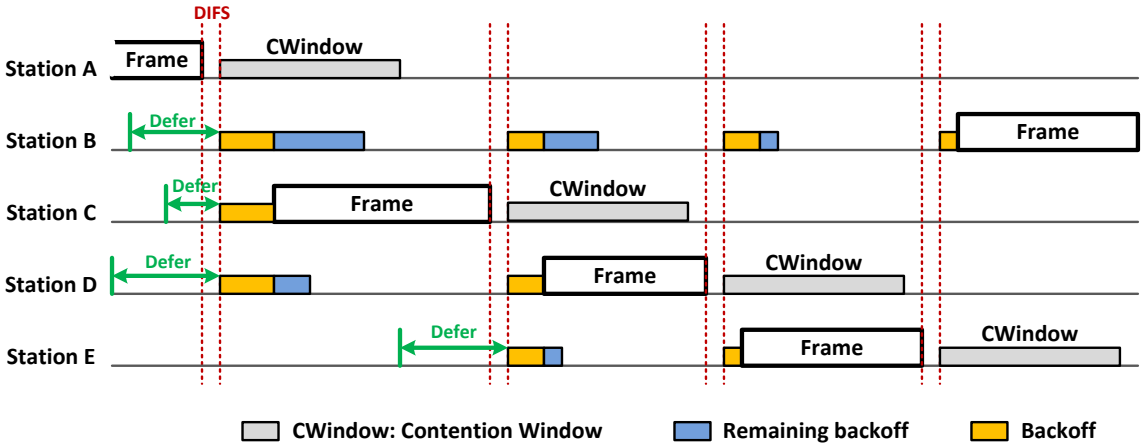


Fig. B.2. Conventional CSMA/CA protocol.

The value of CW is not fixed, but being changed during the procedure. Its initial value is aCWmin. Every unsuccessful attempt to transmit frame will increase CW until CW reaches aCWmax as shown in Fig. B.3. Every successful attempt resets CW to aCWmin. This is the algorithm called exponential back-off, and it can reduce collisions even with high traffic.

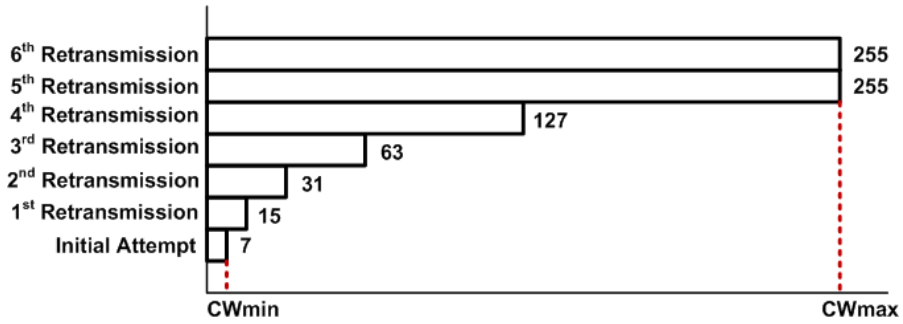


Fig. B.3. Exponential backoff of CSMA/CA.

Appendix B. 3 Modified CSMA/CA

For the inductive data link, the conventional CSMA/CA should be modified. Since the inductive data link is a half-duplex, a core is unable to detect signal or collision during transmitting. In order to sense a collision, a core should send a request-to-send frame (RTS) to all cores and receive a clear-to-send frame (CTS) from the destination core. If the core receives no CTS frame from any cores after a RTS frame, it means that multiple cores tried to access the channel, and a collision occurred. If the source core receives a CTS signal normally, it means the communication session is established. After the destination core receives the data the source core sent, it will send an ACK frame to close the session, and all cores will prepare the next communication session. This protocol is illustrated in Fig. B.4.

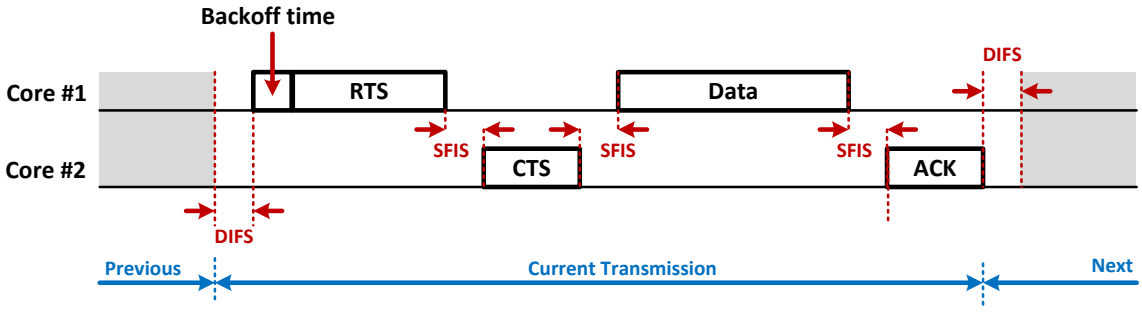


Fig. B.4. Modified CSMA/CA protocol.

At the above-stated protocol, the DIFS and short inter frame space (SIFS) are one clock cycle. It is assumed that it takes one clock cycle for the inductive coupling transceiver to switch between receiver mode and transmitter mode. During this time, the transceiver processes the received data and prepares to transmit as shown in Fig. B.5.

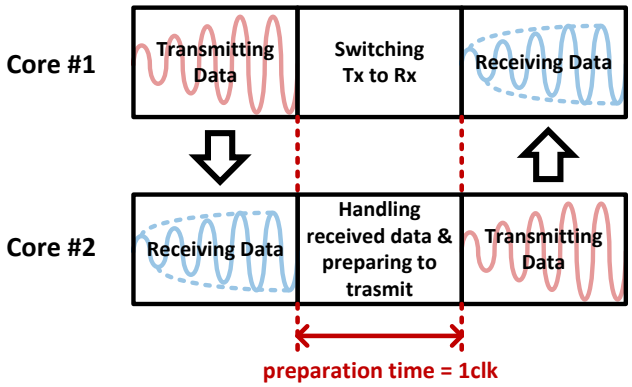


Fig. B.5. Switching of transmitting and receiving in modified CSMA/CA.

Fig. B.6 shows how the modified CSMA/CA operates. If there was no collision at the previous transmission, all cores will have back-off time of 0. If any collision was observed, the cores will have a predefined back-off time. For instance, core #*n* has back-off time of *n-1* clock cycles. This hardwired back-off time guarantees it will be collision-free when retransmitting.

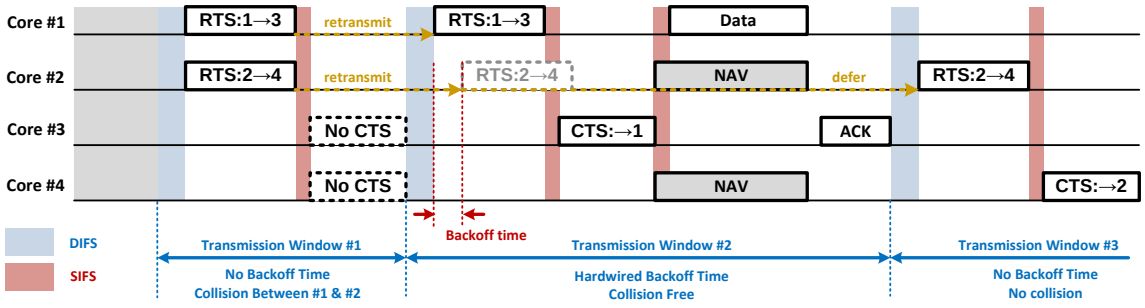


Fig. B.6. Modified CSMA/CA.

Fig. B.7 shows the definitions of frames used in the modified CSMA/CA. It is assumed that four cores share the channel. A data frame contains 16-bit data to control the data channels on other layers. *Ch_addr* means the address of a data channel on each die. A maximum of 16 data channels are supported. *TRx_mode* indicates which circuit inside a transceiver will be controlled by the following control data. 10-bits are assigned for the control data. A RTS frame has a 1-bit header whose value is '1' to indicate the channel is busy. *Tx_addr* refers to the source address and uses hot encoding so that receivers can detect a collision. *Rx_addr*, which is the destination address, is 2-bits since hot encoding is not necessary. When *Tx_addr* is identical to *Rx_addr*, this means the transmission will be a broadcast to all nodes. A CTS frame consists of a 2-bit destination address (its own address) and a 1-bit header to distinguish address 00 from no ACK.

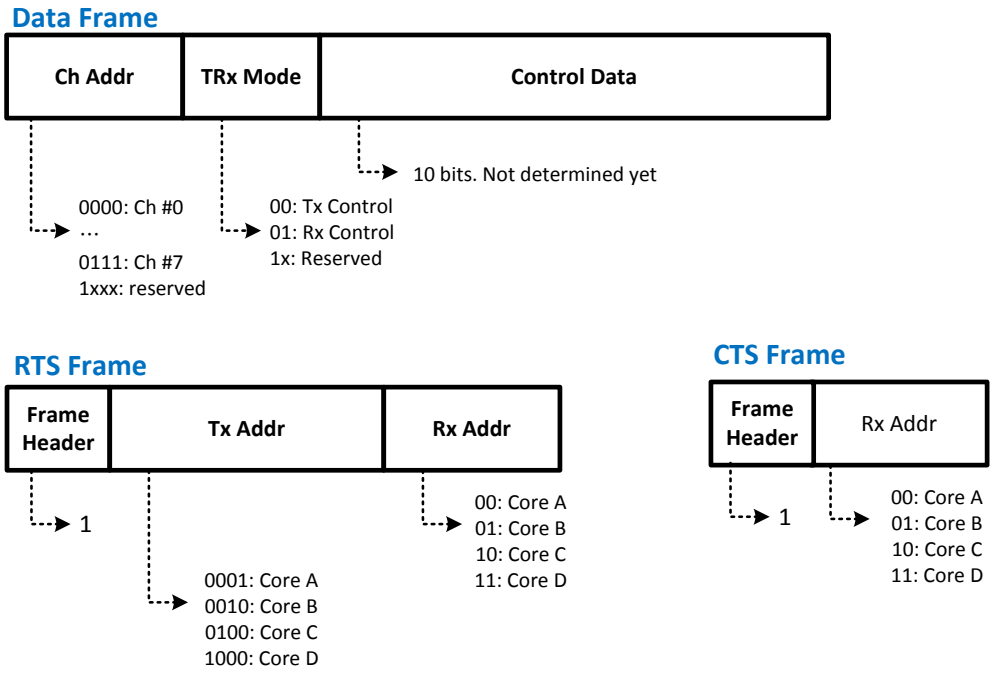


Fig. B.7. Frame definition of Modified CSMA/CA.

Appendix B. 4 CSMA/CF

If a core knows when it can send a frame, no collision will occur. This is the main concept of CSMA/CF (Collision Free). In order to eliminate any possible collisions, all cores have a priority to access the channel, and the priority is based on TDMA. Any core desiring to transmit data should wait for its priority time slot. During its time slot, the core can initiate the window by transmitting a header. Other cores should be in a network allocation vector (NAV) state and wait until the transmission is completed. The length of the transmission is predefined. Since there will be no contention, neither an RTS nor CTS frame is required. Fig. B.8 explains how CSMA/CF works.

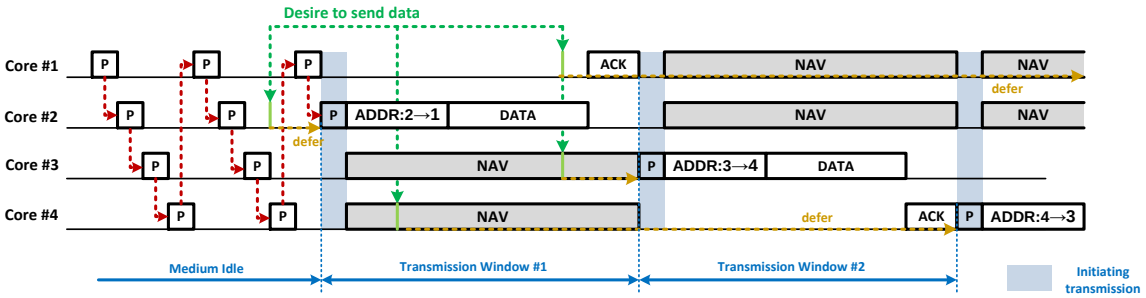


Fig. B.8. CSMA/CF protocol.

The frame definition is shown in Fig. B.9. A data frame is the same on that of CSMA/CA. In an address frame, two bits are assigned for both of source and destination address since hot encoding is not necessary. When the source address is identical to the destination address, this means a broadcasting transmission.

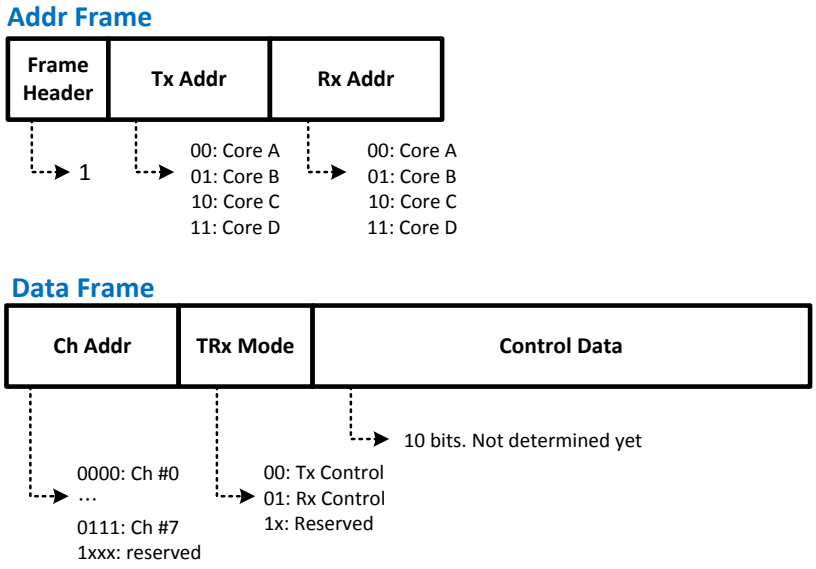


Fig. B.9. Frame definition of CSMA/CF.

Appendix B. 5 Performance Analysis

Fig. B.10 shows the performance comparison of CSMA/CA, CSMA/CF, and TDMA. Due to overheads, CSMA/CA shows the worst frame utilization. However, CSMA has small delay, which means a core might be able to send data whenever it desires to send. The average throughput of CSMA is similar to that of TDMA when the frame generate rate is not high. In a multi-core application, the frequent reconfiguration of core-cache is not required, but the latency is more important. Therefore CSMA/CF is a better choice than TDMA for the control bus of a multi-core system.

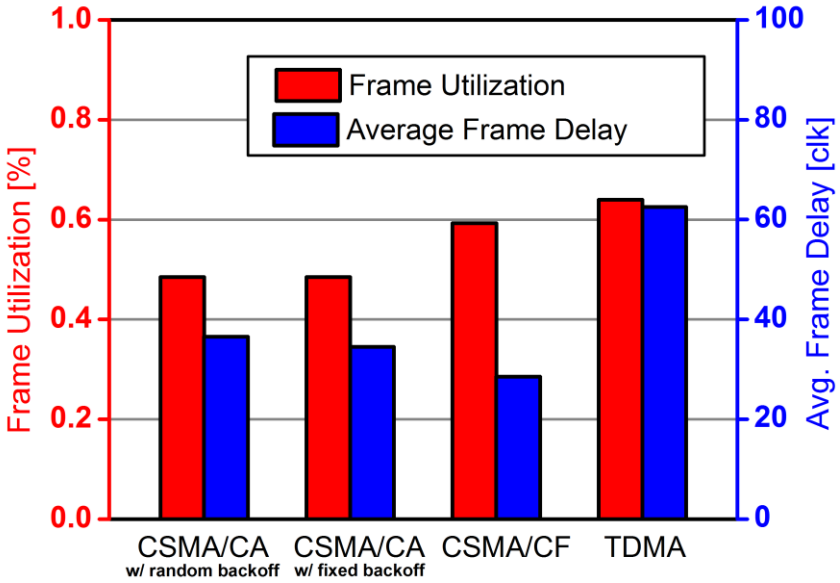


Fig. B.10. Performance comparison.

BIBLIOGRAPHY

[1] J. S. Young, "Greatest Technology Stories," John Wiley and Sons, 1998, pp. 118. ISBN 0471243744.

[2] N. Rosenberg and W. E. Steinmueller, "The Economic Implications of the VLSI Revolution," Futures, Vol. 12, Issue 5, pp. 358-369, Oct. 1980.

[3] S. Waser, "Survey of VLSI for Digital Signal Processing," IEEE International Conference on Acoustics, Speech, and Signal Processing, pp. 376-379, Apr. 1980.

[4] E. A. Vittoz, "The Design of High-Performance Analog Circuits on Digital CMOS Chips," IEEE Journal of Solid-State Circuits, Vol. 20, Issue 3, pp. 657-665, Jun. 1985.

[5] R. W. Brodersen and P. R. Gray, "The role of analog circuits in future VLSI technologies," European Solid-State Circuits Conference, pp. 105-110, Sep. 1983.

[6] Samsung, "Application Processors," [Online] Available:

http://www.samsung.com/global/business/semiconductor/productList.do?fmly_id=844&xFmly_id=229#

[7] Texas Instruments, "Digital Signal Processors (DSP) and ARM Microprocessors (MPUs) Platforms," [Online] Available:

http://www.ti.com/lsds/ti/dsp/platform/device.page

[8] nVidia, "Tegra 2 and Tegra 3 Super Ship Processors," [Online] Available:

http://www.nvidia.com/object/tegra-superchip.html

[9] Qualcomm, "The all-in-one mobile processor," [Online] Available:

http://www.qualcomm.com/snapdragon/processors

[10] J. Ryckaert, S. Brebels, B. Come, W. Diels, D. Hauspie, S. Stoukatch, K. Vaesen, W. D. Raedt, St. Donnay, "Single-package 5GHz WLAN RF Module with Embedded Patch antenna and 20dBm Power Amplifier," IEEE MTT-S Microwave Symposium Digest, Vol. 2, pp. 1037-1040, Jun. 2003

[11] J. Balagia, "Packaging Provides Viable Alternative to SoC," Semiconductor International, pp. 169-181, Jul. 2000.

[12] J. B. Brinton, "SOC Isn't Cutting It Yet. Is Multi-Chip Package a Better Answer Today?" Semiconductor Business News, Jan. 2008.

[13] "Elpida Achieves 4-Layer 0.8mm Mobile RAM Package Using New Ultra-Thin DARM Manufacturing Technology," Elpida, Jun. 2011. Available:

http://www.elpida.com/en/news/2011/06-22.html

[14] "Package-on-package is killer app for handsets," EETimes, Jul. 2008. Available:

http://www.eetimes.com/design/programmable-logic/4005769/Viewpoint-Package-on-package-is-killer-app-for-handsets

[15] G. G. Harman, "Wire bonding in Microelectronics: Materials, Processes, Reliability, and Yield," McGraw-Hill, 1997. ISBN 0-07-032619-3.

[16] S. R. Vempati, N. Su, C. H Khong, Y. Y. Lim, K. Vaidyanathan, J. H. Jau, B. P. Liew, K. Y. Au, S. Tarary, A. Fenner, R. Erich, J. Milla, "Development of 3-D Silicon Die Stacked Package using Flip Chip Technology with Micro Bump Interconnects," IEEE Electronic Components and Technology Conference, pp. 980-987, May 2009.

[17] E. Beyne, "3D System Integration Technologies," IEEE International Symposium on VLSI Technology, Systems, and Applications, pp. 1-9, Apr. 2006.

[18] A. C. Fischer, "Wafer-Level Integration of NiTi Shape Memory Alloy Wires for the Fabrication of Microactuators using Standard Wire Bonding Technology," IEEE International Conference on Micro Electro Mechanical Systems, pp. 348-351, Jan. 2001.

[19] T. Ezaki, K. Kondo, H. Ozaki, N. Sasaki, H. Yonemura, M. Kitano, T. Hirayama, "A 160Gb/s Interface Design Configuration for Multichip LSI," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Vol.1, pp.140-141, Feb. 2004.

[20] G. E. Moore, "Cramming More Components onto Integrated Circuits," Electronics, Vol. 38, No 8, Apr., 1965.

[21] J. D. Meindl, "Interconnect Opportunities for Gigascale Integration," IEEE Micro, Vol. 23, No. 3, pp. 28-35, May/Jun. 2003.

[22] W. Dally, "Stream Processors: Programmability with Efficiency", ACM Queue, Vol. 2, No. 1, pp. 52-62, Mar. 2004.

[23] B. T. Mark, "Interconnect Scaling- The Real Limiter to High Performance ULSI," Proceedings of the IEEE International Electron Devices Meeting, pp. 241-242, Dec. 1995.

[24] A. W. Topol, "Three-Dimensional Integrated Circuits," IBM Journal of Research and Development, Vol. 50, Issue 4.5, Jul. 2006.

[25] J. Goldberger, "Silicon Vertically Integrated Nanowire Field Effect Transistors," Nano Letters, Vol. 6, No. 5, pp. 973-977, Mar. 2006.

[26] G. Rosaz, "Vertically Integrated Silicon-Germanium Nanowire Field-Effect Transistor," Applied Physics Letters, 99, 193107, Oct. 2011.

[27] S. Bobba, "Performance Analysis of 3-D Monolithic Integrated Circuit," IEEE International 3D Systems Integration Conference, Nov. 2010.

[28] S. Bansal, J. C. Rey, A. Yang, M. Jang, L. C. Lu, P. Magarshack, M. Pol, R. Radojcic, "3-D stacked die: Now or future?" ACM/IEEE Design Automation Conference, pp. 298-299, Jun. 2010.

[29] J. Burns, "3D Integration – A Server Perspective," IEEE International 3D Systems Integration Conference, Nov. 2010.

[30] K. Ohsawa, H. Odaira, M. Ohsawa, S. Hirade, T. Lijima, S. G. Pierce, "3-D Assembly Interposer Technology for Next-Generation Integrated Systems," IEEE International Solid-State Circuits Conference, Digest of Technical. Papers, pp. 272-273, Feb. 2001.

[31] "Mentor Graphics Works with Tezzaron and MOSIS on 3DIC Prototyping Service," Mentor Graphics. Available:

http://www.mentor.com/products/ic_nanometer_design/news/mentor-works-with-tezzaron-and-mosis-on-3DIC-prototyping-service

[32] "EV Group and CEA/Leti Partner to accelerate adoption of TSV and 3D Integration Technology," EVG. Available:

http://www.evgroup.com/en/about/news/0409_cealeti_en/

[33] "ZyCube 3D Technology," ZyCube. Avaiable:

http://www.zy-cube.com/e/technology/ZyCube%203D/3dtechnology.html

[34] "Interconnect and 3D reliability-imec," IMEC. Available:

http://www2.imec.be/be_en/education/phd/process-technology/interconnect-and-3d-reliability/legal.html

[35] "Samsung Demos 32GB RDIMM with Through Silicon Via Packaging," xbitlabs, Aug. 2011. Available:

http://www.xbitlabs.com/news/memory/display/20110817171001_Samsung_Demos_32GB_RDIMM_with_Through_Silicon_Via_Packaging.html

[36] L. Luo, et al, "3Gb/s AC-Coupled Chip-to-Chip Communication using a Low-Swing Pulse Receiver," IEEE International Solid-State Circuits Conference, Digest of Tech. Papers, Vol. 1, pp. 522-523, Feb. 2005.

[37] D. Mizoguchi, M. Inoue, T. Sakurai, T. Kuroda. "1.2Gb/s/pin Wireless Superconnect Based on Inductive Inter-Chip Signaling (IIS)," IEEE International Solid-State Circuits Conference, Digest of Technical. Papers, pp. 142-143, Feb. 2004.

[38] Qun, G., Z. Xu, J. Ko, M. F. Chang, "Two 10Gb/s/pin Low-Power Interconnect Methods for 3D ICs," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 448-449, Feb. 2007.

[39] M. Daito, Y. Nakata, S. Sasaki, H. Gomyo, H. Kusamitsu, Y. Komoto, K. Iizuka, K. Ikeuchi, G. S. Kim, M. Takamiya, T. Sakurai, "Capacitively Coupled Non-Contact Probing Circuits for Membrane-Based Wafer-Level Simultaneous Testing," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 144-145, Feb. 2010.

[40] M. Daito, Y. Nakata, S. Sasaki, H. Gomyo, H. Kusamitsu, Y. Komoto, K. Iizuka, K. Ikeuchi, G. S. Kim, M. Takamiya, T. Sakurai, "Capacitively Coupled Non-Contact Probing Circuits for Membrane-Based Wafer-Level Simultaneous Testing," IEEE Journal of Solid-State Circuits, Vol. 46, Issue 10, pp. 2386-2395, Feb. 2011.

[41] W. R. Mann, F. L. Taber, P. W. Seitzer, J. J. Broz, "The Leading Edge of Production Wafer Probe Test Technology," IEEE International Test Conference, Proceeding, pp. 1168-1195, Oct. 2004.

[42] D. Y Lee, D. D. Wentzloff, J. P. Hayes, "Wireless Wafer-Level Testing of Integrated Circuits via Capacitively-Coupled Channel," IEEE International Symposium on Design and Diagnostics of Electronic Circuits & Systems, pp. 99-104, Apr. 2011.

[43] N. Miura, D. Mizoguchi, T. Sakurai, T. Kuroda, "Analysis and Design of Inductive Coupling and Transceiver Circuit for Inductive Inter-Chip Wireless Superconnect," IEEE Journal of Solid-State Circuits, Vol. 40, No. 4, Apr., 2005.

[44] L. Hannakam, "Berechnung der Gegeninduktivität achsenparalleler Zylinderspulen," Archiv fur Elektrotechnik, Vol. 51, pp. 141-154, May 1967.

[45] E. S. Hochmair, "Geomaetric Approach for Coupling Enhancement of Magnetically Coupled Coils," IEEE Transactions on Biomedical Engineering, Vol. 43, Issue 7, pp. 708-714, Jul. 1996.

[46] N. Miura, D. Mizoguchi, M. Inoue, T. Sakurai, T. Kuroda, "A 195-Gb/s 1.2-W Inductive Inter-Chip Wireless Superconnect With Transmit Power Control Scheme for 3-D-Stacked System in a Package," IEEE Journal of Solid-State Circuits, Vol. 41, No. 1, Jan., 2006.

[47] N. Miura, D. Mizoguchi, M. Inoue, K. Niitsu, Y. Nakagawa, M. Tago, M. Fukaishi, T. Sakurai, T. Kuroda, "A 1 Tb/s 3 W Inductive-Coupling Transceiver for 3D-Stacked Inter-Chip Clock and Data Link," IEEE Journal of Solid-State Circuits, Vol. 42, No. 1, Jan. 2007.

[48] N. Miura, H. Ishikuro, K. Niitsu, T. Sakurai, T. Kuroda, "A 0.14pJ/b Inductive-Coupling Transceiver with Digitally-Controlled Precise Pulse Shaping, IEEE Journal of Solid-State Circuits," Vol. 43, No. 1, Jan., 2008.

[49] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, T. Kuroda, "An 11Gb/s Inductive-Coupling Link with Burst Transmission," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 298-299, Feb 2008.

[50] N. Miura, T. Sakurai, T. Kuroda, "Crosstalk Countermeasures for High-Density Inductive-Coupling Channel Array," IEEE Journal of Solid-State Circuits, Vol., 42, No. 2, Feb., 2007.

[51] K. Niitsu, Y. Shimazaki, Y. Sugimori, Y. Kohama, K. Kasuga, I. Nonomura, M. Saen, S. Komatsu, K. Osada, N. Irie, T. Hattori, A. Hasegawa, T. Kuroda, "An Inductive-Coupling Link for 3D Integration of a 90nm CMOS Processor and a 65nm CMOS SRAM", IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 480-481, Feb 2009.

[52] Y. Yuan, N. Miura, S. Imai, H. Ochi, T. Kuroda, "Digital Rosetta Stone: A Sealed Permanent Memory with Inductive-Coupling Power and Data Link", IEEE Symposium on VLSI Circuits, pp.26-27, Jun. 2009.

[53] Y. Yuan, A. Radeki, N. Miura, I. Aikawa, Y. Take, H. Ishikuro, T. Kuroda, "Simultaneous 6Gb/s Data and 10mW Power Transmission using Nested Clover Coils for Non-Contact Memory Card," IEEE Symposium on VLSI Circuits, pp.199-200, Jun. 2010.

[54] P. V. Nikitin, V. S. Rao, S. Lazar, "An Overview of Near Field UHF RFID," IEEE International Conference on RFID, pp. 167-174, Mar. 2007.

[55] C. Capps, "Near Field or Far Field," EDN, pp. 95-102, Aug. 2001.

[56] J. Krause, "Antennas," McGraw Hill, New York, NY, 1950.

[57] D. White, "EMI Control Methods and Techniques," Vol. 1~5. Don White Consultants, Gainesville, VA.

[58] "Measurement of Electromagnetic Interference Characteristics," Department of Defense, MIL-STD 449, Jul. 1967.

[59] B. Berkowitz, "Basic Microwaves," Hayden, New York, NY, 1966.

[60] M. Mardiguian, "Interference Control in Computer and Microprocessor-Based Equipment," Don White Consultants, Gainesville, VA, 1984.

[61] "Measurement of Electromagnetic Interference Characteristics," Department of Defense, MIL-STD 462, Jul. 1967.

[62] B. Keiser, "Principles of Electromagnetic Compatibility," Artech House, Norwood, MA.

[63] K. Finkenzeller, "RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identifications," Wiley, May 2003.

[64] A. Radecki, H. Chung, Y. Yoshida, N. Miura, T. Shidei, H. Ishikuro, T. Kuroda, "6W/25mm^2 Inductive Power Transfer for Non-Contact Wafer-Level Testing," IEEE

International Solid-State Circuits Conference, Digest of Technical Papers, pp.230-231, Feb. 2011.

[65] A. Kurs A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, M. Soljcic, "Wireless Power Transfer via Strongly Coupled Magnetic Resonances", Science Vol. 317, 83, 2007.

[66] N. Miura, Y. Take, M. Saito, Y. Yoshida, T. Kuroda, "A 2.7Gb/s/mm2 0.9pJ/b/Chip 1Coil/Channel ThruChipInterface with Coupled-Resonator-Based CDR for NAND Flash Memory Stacking," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 490-491, Feb. 2011.

[67] Y. Sugimori, Y. Kohama, M. Saito, Y. Yoshida, N. Miura, H. Ishikuro, T. Sakurai, T. Kuroda, "A 2Gb/s 15pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 244-245, Feb. 2009.

[68] M. Saito, N. Miura, T. Kuroda, "A 2Gb/s 1.8pJ/b/chip Inductive-Coupling through Chip Bus for 128-Die NAND-Flash Memory Stacking," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp.330-441, Feb. 2010.

[69] N. Miura, Y. Take, M. Saito, Y. Yoshida, T. Kuroda, "A 2.7Gb/s/mm2 0.9pJ/b/chip 1 coil/channel Thru Chip interface with coupled-resonator-based CDR for NAND Flash memory stack," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp.490-492, Feb. 2011.

[70] M. J. E. Golay, "Normalized Equations of the Regenerative Oscillator -Noise, Phase-Locking, and Pulling," Proceedings of IEEE, Vol. 52, No. 11, pp. 1313-1330, Nov. 1964.

[71] J. L. Bohorquez, J. L. Dawson, A. P. Chandrakasan, "A 350μW CMOS MSK Transmitter and 400μW OOK Super-Regenerative Receiver for Medical Implant Communications," IEEE Symposium on VLSI, pp. 32-33, Jun. 2008.

[72] B. Otis, Y. H. Chee, J. Rabaey, "A 400μW-RX, 1.6mW-TX Super-Regenerative Transceiver for Wireless Sensor Networks," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 396-397, Feb. 2005.

[73] A. Yu, J. H. Lau, S. W. Ho, A. Kumar, W. Y. Hnin, W. S. Lee, M, C, Jong, V. N. Sekhar, V. Kripesh, D. Pinjala, S. Chen, C. Chan, C Chao, C, Chiu, C. Huang, C. Chen, "Fabracation of High Aspect Ratio TSV and Assembly with Fine Pitch Low-Cost Solder Microbump for Si Interposer Technology with High-Density Interconnects," IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 1, Issue 9, pp. 1336-1344, Sep. 2011.

[74] M. W. Newman, S. Muthukumar, M. Schuelein, T. Dambruskas, P. A. Dunaway, J. M. Jordan, S. Kulkarni, C. D. Linde, T. A. Opheim, R. A. Stingel, W. Worwag, L. A. Topic, J. M. Swan, "Fabrication and Electrical Characterization of 3D Vertical Interconnects," IEEE Electronic Components and Technology Conference 2006, pp. 394-398.

[75] J. Van Olmen, A. Mercha, G. Katti, C. Huyghebaert, J. Van Aelst, E. Seppala, Z. Chao, S. Armini, J. Vaes, R. C. Teixeira, M. Van Cauwenberghe, P. Verfonck, K. Verhemeldonck, A. Jourdain, W. Ruythooren, M. Broeck, A. Opdebeeck, T. Chiarella, B. Parvais, I. Debusschere, T. Y. Hoffmann, B. De Wachter, W. Dehaene, M. Stucchi, M. Rakiwski, P. Soussan, R. Cartuyvels, E. Beyne, S. Biesemans, B. Swinnen, "3D Stacked IC demonstration using a Through Silicon Via First Approach," IEEE International Electron Devices Meeting, pp. 603-606, Dec. 2008.

[76] Y. Yang, G. Katti, R. Babie, Y. Travaly, B. Verlinden, I. De Wolf, "Electrical Evaluation of 130-nm MOSFETs with TSV proximity in 3D-SIC Structure," IEEE International Interconnect Technology Conference, pp. 1-3, Jun. 2010.

[77] G. Van der Plas, P. Limaye, A. Mercha, H. Oprins, C. Torregiani, S. Thijs, D. Linten, M. Stucchi, K. Guruprasad, D. Velenis, D. Shinichi, V. Cherman, B. Vandevelde, V. Simons, I. De Wolf, R. Labie, D. Perry, S. Bronckers, N. Minas, M. Cupac, W. Ruythooren, J. Van Olmen, A. Phommahaxay, M. de Potter de ten Broeck, A. Opdebeeck, M. Rakowski, B. De Wachter, M. Dehan, M. Nelis, R. Agarwal, W. Dehaene, Y. Travaly, P. Marchal, E. Beyne , "Design Issues and Considerations for Low Coast 3D TSV IC Technology," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 148-149, Feb. 2010.

[78] "3D Super-Via for Memory Applictions," available:

http://www.tezzaron.com/about/papers/Sangki_2007.pdf

[79] G. Ghibaudo, "New Method for the Extraction of MOSFET parameters," Electron Letter, Vol. 24, No. 9, pp. 543-545, Apr. 1998.

[80] J. Gambino, D. Vanslette, B. Webb, C. Lube, T. Ueda, T. Ichigaki, K. Kang, W. S. Yoo, "Stress Characterization of Tungsten-filled Through Silicon Via Arrays using Very High Resolution Multi-Wavelength Raman Spectroscopy," Electrochemical Society Transaction Vol. 35, Issue 2 May 2011, pp. 105-115.

[81] K. Matsuda, K. Suzuki, K. Yamamura, Y. Kanda, "Nonlinear Piezoresistance Effects in Silicon," Journal of Applied Physics Vol. 73, No. 4, pp. 1838-1846, Feb 1993.

[82] M. A. Hopcroft, W. D. Nix, T. W. Kenny, "What is the Young's Modulus of Silicon?" Journal of Microelectromechanical Systems, Vol.19, No.2, Apr. 2010.

[83] P. Ruther, J. Bartholomeyczik, S. Trautman, M. Wandt, O. Pual, W. Dominicus, R. Roth, K. Seitz, W. Strauss, "Novel 3D piezoresistive silicon force sensor for dimensional metrology of micro components," IEEE Sensors 2005.

[84] F. Bufler, A. Erlebach, M. Oulmane, "Hole mobility model with silicon inversion layer symmetry and stress-dependent piezoconductance coefficients," IEEE Electron Device Letter, Vol.30, no.9, pp. 996-998, Sep. 2009.

[85] C. S. Smith, "Piezroresistance Effect in Germanium and Silicon," Physical Review, Vol. 94, No. 1, pp 42-49, Apr. 1954.

[86] J. C. Suhling, R. C. Jaeger, "Silicon Piezoresistive Stress Sensors and Their Application in Electronic Packaging," IEEE Sensors Journal, Vol. 1, No. 1, pp. 14-30, Jun. 2001.

[87] A. T. Pham, C. Jungemann, B. Menerzhagen, "Modeling of Piezoresistice Coefficients in Si Hole Inversion Layers," IEEE Internation Conference on Ultimate Integration of Silicon, pp. 121-124, Mar. 2009.

[88] H. Sangki, et al., "3D Super-Via for Memory Applications," MicroSystems Packaging Initiative Packaging Workshop 2007.

[89] A. Jourdain, T. Buisson, A. Phommahaxay, A. Redolfi, S. Thangaraju, Y. Travaly, E. Beyne, B. Swinnen, "Integration of TSVs, Wafer Thinning and Backside Passivation on Full 300mm CMOS Wafers for 3D Application," IEEE Electronic Components and Technology Conference, pp. 1122-1125, May 2011.

[90] J. Lee, Y. Chen, Y. Huang, "A Low-Power Low-Cost Fully-Integrated 60-GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly", IEEE Journal of Solid-State Circuits, Vol. 45, Issue 2, pp. 264-275, Feb. 2010.

[91] J. Chen, M. Flynn, J. P. Hayes, "A Fully Integrated Auto-Calibrated Super-regenerative Receiver in 0.13um CMOS", IEEE Journal of Solid-State Circuits, Vol. 42, Issue 9, pp. 1976-1985, Sep. 2007.

[92] S. Han, D. D. Wentzloff, "Wireless Power Transfer Using Resonant Inductive Coupling for 3D Integrated ICs," IEEE 3D System Integration Conference, pp. 1-5, Nov. 2010

[93] U. Karthaus, M. Fischer, "Fully Integrated Passive UHF RFID Transponder IC With 16.7-μW Minimum RF Input Power," IEEE Journal of Solid-State Circuits, Vol. 38, Issue 10, Oct. 2003

[94] Information Tethered Micro Automated Rotary Stages (ITMARS), DARPR MTO BAA 08-74 [Online]