A Crystal-Less BLE Transmitter With Clock Recovery From GFSK-Modulated BLE Packets

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***Abstract*— In this article, we present a crystal-less Bluetooth low-energy (BLE) transmitter using RF reference recovery directly from GFSK-modulated BLE packets. In order to achieve fast frequency calibration from modulated signals and reduce interference from other BLE users, the transceiver consists of a back-channel wake-up receiver, a clock-recovery receiver, a transmitter, and a dual-all-digital phase-locked loop (ADPLL) frequency synthesizer for system wake-up, clock-recovery, packet transmission, and frequency calibration. An embedded averaging processing unit in the loop filter of the ADPLL is proposed to retrieve accurate frequency information from GFSK-modulated signals. A prototype chip is fabricated in 40-nm CMOS for verification. The crystal-less transmitter with clock recovery meets all BLE requirements for SIR, making this a robust solution for removing the crystal even in densely populated networks.**

***Index Terms*— All-digital phase-locked loop (ADPLL), back-channel, Bluetooth low-energy (BLE), crystal oscillator (XO), frequency calibration, receiver, reference recovery, transmitter.**

I. Introduction

THERE has been an increasing interest in removing the crystal oscillator (XO) in standard-compliant wireless devices to reduce the power consumption, size, and cost of the overall system. State-of-the-art XOs operating in the MHz-range will consume at least tens of microwatts [1]–[4] and have to be duty-cycled to save energy. However, the startup of an XO generally consumes much more power than in the steady state and it could take milliseconds for the XO to settle, so the startup energy from duty-cycling becomes prohibitive. The XO is also one of the bulkiest and expensive off-chip components. Thus, removing the XO from certain radios is very attractive, although it has proved to be very challenging. Whether the XO can be removed from specific radio designs mainly depends on the phase noise (PN) requirement and necessary frequency calibration methods. For example, it is almost impossible to remove the XO in high-performance mmWave radios for 5G applications, while some pulse-modulated radios can easily operate without an XO since their PN is rarely a concern. Bluetooth low-energy (BLE) stands right on the edge. On one hand, the PN requirement for BLE is quite relaxed compared to other mainstream standards such as WiFi and LTE, and an open-loop *LC* oscillator could offer sufficient noise performance during packet transmission [5]. Thus, solely from the noise point of view, PLL and XO are not necessary. On the other hand, the local oscillator (LO)'s frequency in a BLE radio has to be calibrated and controlled for channel selection. So from the FCC certification perspective, the PLL and XO are necessary.

In many recent BLE designs [6]–[8], instead of having the PLL locked all the time, the LO chooses to use a "calibration and open-loop" scheme where once the oscillator is locked to the right channel by the PLL controller, it will be set to open-loop with a much simpler direct modulation for packet transmission. This frequency calibration scheme in BLE designs not only saves power and reduces modulation complexity, but it also offers a chance to remove the high-frequency XO as the PLL reference. Yuan *et al.* [9] replace the high-frequency XO with a 32-kHz real-time clock (RTC) in its all-digital phase-locked loop (ADPLL) design for BLE applications. By using a two-point FM modulation, it overcomes a narrow PLL bandwidth due to the 32-kHz reference clock and achieves instantaneous channel selection. It saves a significant amount of power by removing the high-frequency XO, but the RTC generally comes from a low-frequency XO as well, so it is not strictly XO-less. Although relaxation oscillators could serve as a low-frequency clock for many digital applications, their relatively high PN's impact on PLL calibration frequency accuracy still remains unclear. Wiser *et al.* [10] use an FBAR resonator as the crystal reference replacement that can meet the frequency accuracy requirement for BLE, but it needs a special fabrication process and might cost even more than an XO for mass production. Maksimovic *et al.* [11] reports a BLE and IEEE 802.15.4 compatible XO-less transceiver by using a network-based frequency compensation from a Zigbee transmitter. It completely removes the XO in the edge node. However, it takes hundreds of milliseconds to do frequency calibration, and in order for the edge node to transmit BLE

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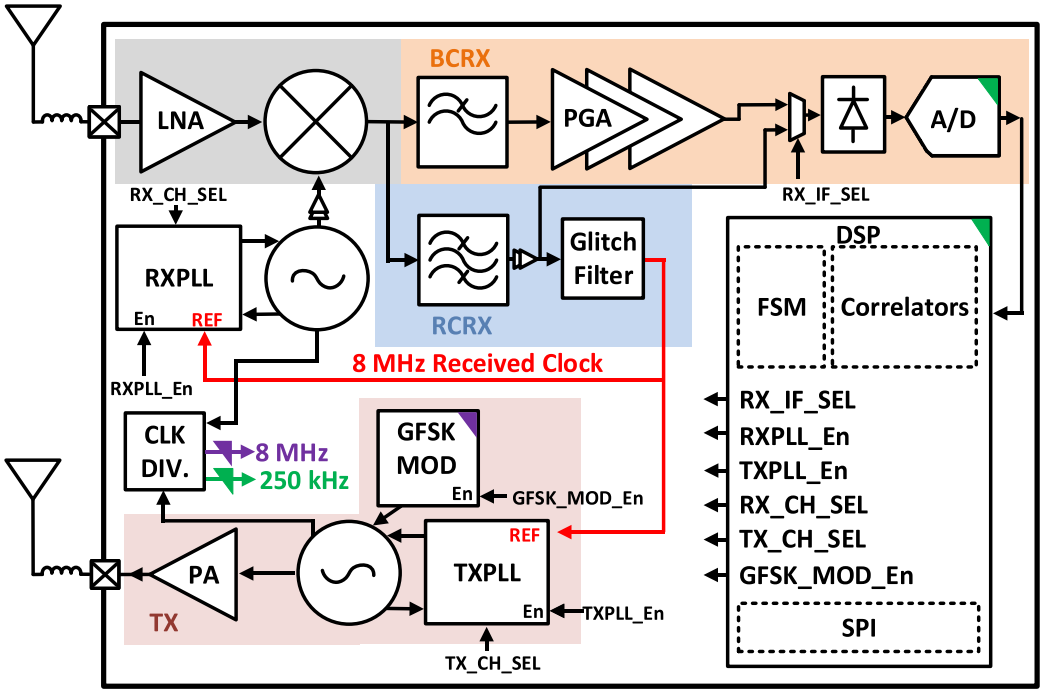

Fig. 1. Block diagram of the proposed crystal-less BLE transceiver with BLE BCRX, RCRX, TX, and dual-ADPLL frequency synthesizer.

packets, its corresponding base station needs to transmit a Zigbee signal.

In this article, we propose an asymmetric XO-less BLE transceiver with over-the-air reference clock-recovery compliant with the BLE standard [20] to address the above issues. The proposed design is based on RF clock recovery that completely removes the XO, and is capable of doing frequency calibration with GFSK-modulated BLE packets. It achieves fast locking and frequency calibration through a dual-ADPLL frequency synthesizer within a single BLE packet once the reference clock-recovery receiver (RCRX) is enabled. The ultralow-power transmitter is then enabled to transmit BLE packets everytime the frequency is calibrated. Furthermore, a back-channel wake-up receiver (BCRX) is added to the main RCRX for system wake-up and potential interference filtering in the time domain to guarantee robust frequency calibration and XO-less operation in densely populated networks.

This article is an extension of [12] and it is organized as follows. Section II covers the system design considerations including system architecture, RF reference recovery from GFSK-modulated BLE packets, and data transmission using the calibrated LO. It also discusses the key ADPLL design tradeoffs to carry out frequency calibration from a frequency-modulated reference. Section III discusses detailed circuit implementation and Section IV presents measurement results. Finally, Section V draws the conclusion.

II. System Design Considerations

In order to achieve fast wake-up and calibration from standard BLE packets, several techniques are used to enable RF reference recovery from a GFSK-modulated signal with interference resilience: 1) an architecture with two ADPLLs and selective baseband filter to recover a reference clock from a received packet and then transmit a GFSK-modulated BLE packet on any channel; 2) an ADPLL with an embedded averaging processing unit (APU) in the loop filter to recover a stable reference from a GFSK-modulated signal, and 3) a BCRX [13] to detect advertising (ADV) events from a broadcaster while rejecting interference. The block diagram of the proposed crystal-less BLE transmitter with an RF reference recovery receiver is shown in Fig. 1. The receiver consists of two RX signal paths mixed down by the first LO: a BCRX direct conversion path for detecting ADV events, and an RF reference clock-recovery path with an intermediate frequency of 8 MHz producing the reference for the two PLLs. The PLLs are identical but use different frequency control words (FCW) to ensure accurate frequency calibration and data transmission at any channel. The PLL is a divider-less ADPLL with an embedded APU in the loop filter to retrieve accurate frequency information from a GFSK-modulated signal. The transmitter takes the output of the second LO with an open-loop GFSK modulator after frequency calibration. A Class-D digital power amplifier is used for TX transmission.

A. System Operation

Fig. 2 shows the concept of the system operation and frequency plan for both the TX and RX LO at different states. Initial one-time calibration would be performed for each chip to compensate process variations. The process begins with the BCRX path enabled first, scanning the three BLE ADV channels for a predefined channel hopping pattern and the packet length. These channels are CH37, CH38, and CH39 at 2402, 2426, and 2480 MHz, respectively. The RXLO is an open loop and hops among different channels to oversample and detect the energy of ADV packets. Once the BCRX demodulator detects the intended ADV event by correlating

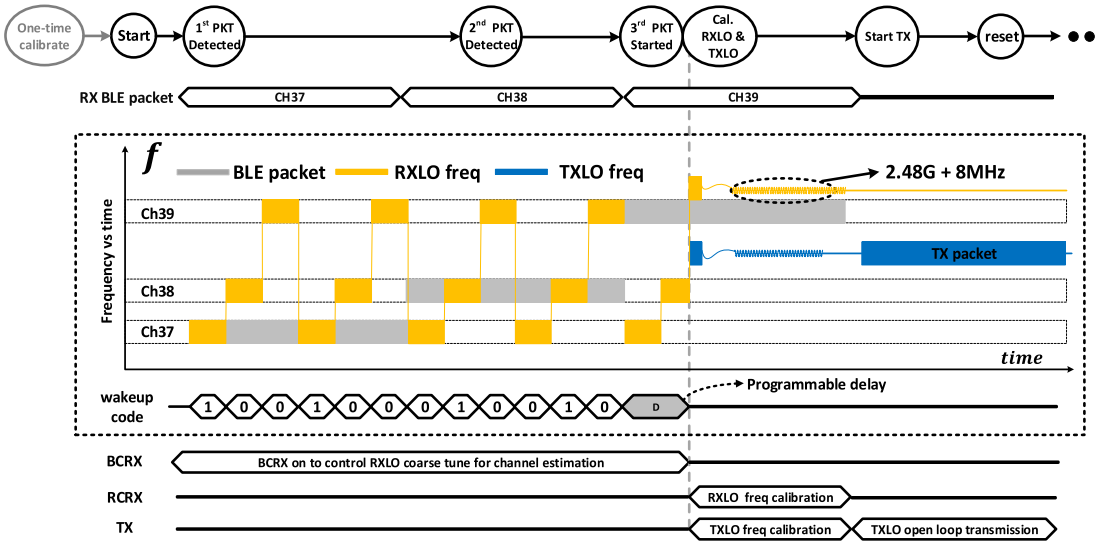

Fig. 2. System operation state diagram and conceptual frequency plan for the TX and RX LO.

the digitized signal with programmable templates, the receiver switches to reference clock-recovery mode and the dual-ADPLL frequency synthesizer is turned on for both the RCRX path and the TX path. The RX LO at this time is coarsely set to 8 MHz above 2.48 GHz and the TX LO is set close to the target channel for transmission. Once the frequency calibration is done for both paths, the TX LO is released for open-loop GFSK modulation and single packet transmission in the target channel.

B. BLE BCRX

The BLE BCRX [13] is designed to detect the patterns of existing BLE packets in the ADV channels as illustrated in Fig. 2, and its block diagram is shown in Fig. 1. The BCRX serves two purposes during channel acquisition. First, it works as a wake-up receiver for the whole system to look for the pre-programmed pattern from incoming ADV events. Second, since the pattern is pre-programmed, once the BCRX finds the first part of the pattern, the LO will be tuned to the target channel for further frequency calibration through the RCRX. This ensures that neither of the two PLLs is enabled until a valid ADV event is detected, eliminating false wake-ups and erroneous frequency calibrations. In this design, the frequency hopping of the RX LO is from Ch.37 to Ch.38 and then to Ch. 39, with a hopping clock rate of 20 kHz. As shown in Fig. 2, when the incoming BLE packet is in Ch. 37, the BCRX will generate a code of "100." If the BCRX detects the first two packets in channel 37 and 38 (100-100-010-010), the RX LO will tune the frequency to 2.488 GHz after some programmable delays for reference clock recovery from an expected packet in channel 39 at 2.48 GHz. When there is a delay between two packets, the LO will continue hopping but the decoded data will be "chopped" once two consecutive "channel codes" are found. The programmable delay is corresponding to the delays between packets in the predefined wake-up pattern.

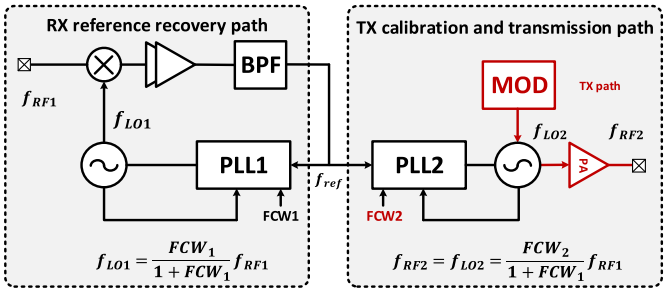

Fig. 3. Simplified block diagram of the reference recovery RX and TX path with frequency relationship among TX, RX, and the two LO.

C. RF RCRX

The RCRX will be turned on once the expected wake-up pattern is found through the BCRX. Fig. 3 shows the simplified block diagram of the reference recovery path and the TX transmission path with two PLLs controlled by different FCWs. The incoming RF signal at 2.48 GHz will be first mixed down to around 8 MHz from the RX LO where the initial frequency is set by the coarse tune from the BCRX. It then passes through a bandpass filter designed at 8 MHz with a 2-MHz bandwidth and 50-dB gain.

The down-converted signal will serve as the reference for the two PLLs. The RX PLL will be fed back to the mixer to further adjust the reference frequency. The TX PLL's output will also track this reference. In steady state, the relationship of the incoming RF signal and the two LOs is as follows:

$$f_{\mathrm{LO1}} = \frac{\mathrm{FCW}_1}{\mathrm{FCW}_1 \pm 1} f_{\mathrm{RF1}} \tag{1}$$

$$f_{\mathrm{RF2}} = f_{\mathrm{LO2}} = \frac{\mathrm{FCW}_2}{\mathrm{FCW}_1 \pm 1} f_{\mathrm{RF1}} \tag{2}$$

where $\mathrm{FCW}_{1,2}$ are the FCWs for the two PLLs. FCW_1 sets the frequency of the LO to 2.488 GHz while FCW_2 sets the frequency of the TX LO to the target transmission channel. During the uncertain IF down-conversion, the RX LO will be tuned close to 2.488 GHz for an 8-MHz IF signal. Although

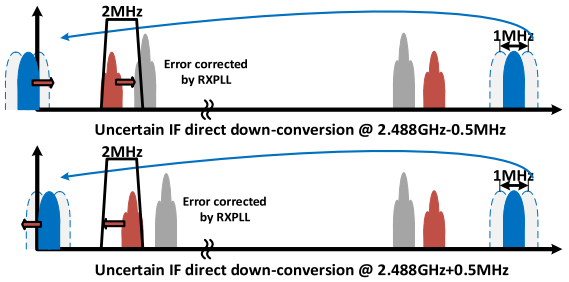

Fig. 4. Uncertain IF down-conversion and bandpass filtering for the RCRX.

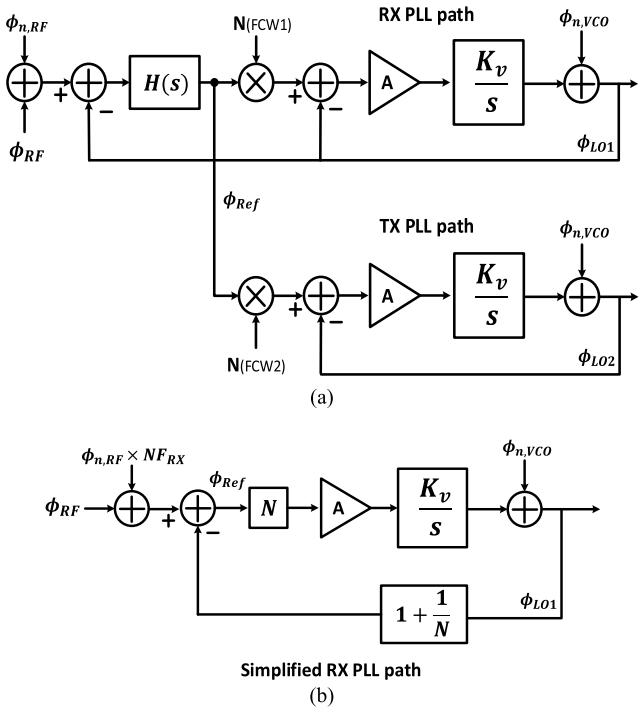

Fig. 5. (a) Behavior model for the reference recovery RX PLL path and TX PLL path highlighting RF noise and VCO noise. (b) Simplified RX PLL path noise model.

2.472 GHz would also satisfy (1), the higher frequency LO does not need to worry about image signals in other BLE channels such as data channels close to 2.464 GHz for the low-frequency LO case. Overall, 2.488 GHz is a better choice as 2.464 GHz is more crowded compared to 2.496 GHz. Considering the LO uncertainty (<1 MHz) when it is initially set by the BCRX in coarse tune, the error could always be recovered by the PLL within the 2-MHz bandpass filter bandwidth as shown in Fig. 4. The adjacent channel blocker at 2.78 GHz, if there exists one at the same time, will not affect the calibration.

The stability of the reference recovery path after it settles in steady state is analyzed through a linear model. Fig. 5(a) shows the system block diagram of the RX PLL path and the TX PLL path. The two PLLs are type I divider-less ADPLLs with only a gain stage as the loop filter. $H(s)$ stands for the gain and filtering for the incoming RF signal. Since its bandwidth is much larger than the PLL bandwidth (10 times), it can be simplified as an additional noise source added to the RF signal from the LNA, mixer, and the bandpass filter, which is equivalent to the noise figure (NF) of the receiver. The reference phase is then generated from the mixed down signal. In a divider-less PLL, the reference phase is virtually multiplied by the divide ratio N for phase comparison. In the RX PLL case, $N = \mathrm{FCW}_1$ and in the TX PLL case, $N = \mathrm{FCW}_2$. For simplicity, we all denote it as "N," and only the RF noise from the incoming BLE packet and the VCO noise are illustrated as they are the dominant noise sources in this design.

The RX PLL's block diagram could be simplified as Fig. 5(b) and the transfer function from RF input noise $\phi_{n,\mathrm{RF}}$ to LO output phase ϕ_{LO1} is

$$\frac{\phi_{\mathrm{LO1}}}{\phi_{n,\mathrm{RF}}} = \frac{\frac{\mathrm{NAK_v}}{s}}{1+\frac{(N+1)\mathrm{AK_v}}{s}} \times \mathrm{NF_{RX}} \approx \frac{G(s)}{1+G(s)} \times \mathrm{NF_{RX}} \quad (3)$$

where $G(s) = \mathrm{NAK_v}/s$, A is the loop filter gain, K_v is the VCO gain, and $\mathrm{NF_{RX}}$ is the NF of the receiver path. As N is much greater than 1, it can be seen that the noise from the RF packet will not be upconverted by the multiplication ratio N in the RX PLL path even though it is mixed down by the LO and it will only suffer from the loss of receiver NF. Similarly, the transfer function from VCO noise $\phi_{n,\mathrm{VCO}}$ to output is

$$\frac{\phi_{\mathrm{LO1}}}{\phi_{n,\mathrm{VCO}}} = \frac{1}{1+G(s)}. \quad (4)$$

And the down-converted reference phase is

$$\phi_{\mathrm{Ref}} = \phi_{n,\mathrm{RF}} \times \mathrm{NF_{RX}} - \phi_{\mathrm{LO1}} = \frac{\mathrm{NF_{RX}}}{1+G(s)} \times \phi_{n,\mathrm{RF}}. \quad (5)$$

Equation (5) shows that the recovered reference signal at 8 MHz is high pass filtered by the RX PLL with additional noise from the RX NF. As the reference for the TX PLL, unlike the RX PLL, its noise will be upconverted by the frequency divider ratio. This noise could be the dominant noise source for the TX PLL at the PLL bandwidth. As the reference noise will be low pass filtered again in the TX PLL, a smaller TX PLL bandwidth could help reduce this noise. Fig. 6 shows the noise contribution of both the RX and TX PLL path. In this setup, the RX PLL bandwidth is set to ~100 kHz and the TX PLL bandwidth is set to ~50 kHz. The extra noise added to the TX PLL loop could be filtered by the proposed embedded APU, as will be illustrated in Section II-D.

D. ADPLL With Embedded APU

As discussed in Section III-C, the RX PLL's noise profile is the superposition of RX degraded RF noise from the packets with low pass filtering and the VCO noise with high pass filtering without noise up-conversion from the frequency multiplication ratio. But in the TX PLL, the reference noise plays a bigger role. It will be raised by $20\log(N)$ although it is high pass filtered by the RX PLL and low pass filtered by the TX PLL. Thus, there will be a noise bump located where the frequency offset is below the PLL bandwidth if the noise is high in the incoming BLE packet. Additionally, for both TX and RX PLLs, the incoming RF signal is GFSK-modulated, thus, noise from the RF source will always be high. In order to deal with these noise "bumps" at various frequency offsets, we propose an APU embedded in the loop filter of the PLL.

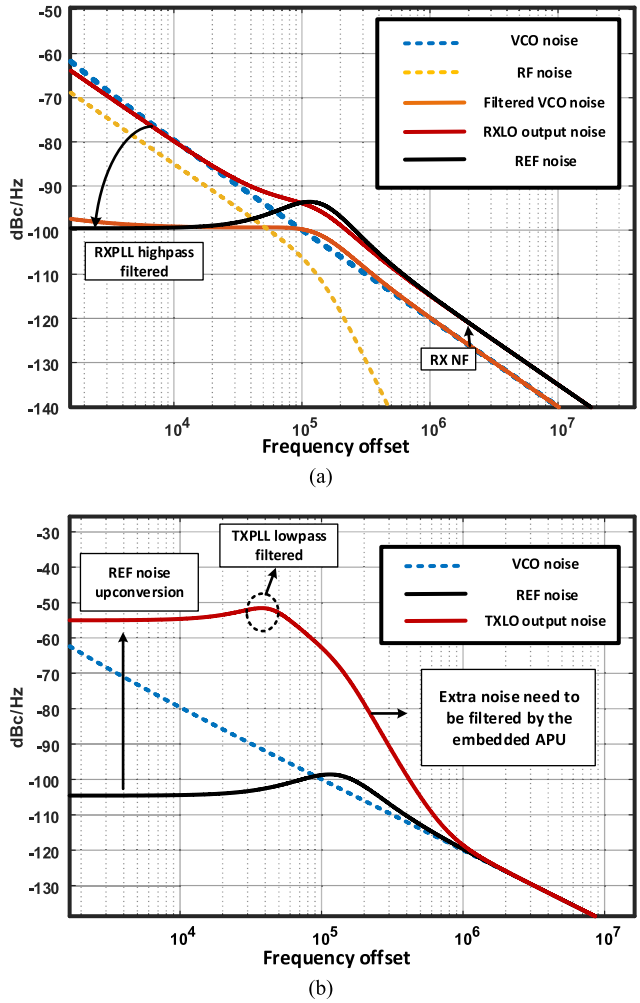

Fig. 6. Major noise contribution of the (a) RX PLL path and (b) TX PLL path.

With enough averaging time, the APU will remove all the noise's impact on frequency accuracy until it hits the flicker noise corner from the RF reference regardless of modulation, and noise bumps in frequency offsets higher than the flicker noise corner [14].

Fig. 7 shows the block diagram of the proposed ADPLL with embedded APU. It is based on the traditional type I divider-less ADPLL [21] and the APU is embedded in the digital loop filter and performs a windowed averaging algorithm of the digital control word (DCW). The APU is designed with two stages and a programmable length controller. The first stage consists of several average units (AUs) with different average time windows controlled by the programmable delays. The second stage controls the total time for average processing according to the flicker noise corner of the reference. The APU is designed to accommodate different reference types for accurate frequency prediction. The two-stage design with programmable AU lengths could help avoid the APU from sampling repetitive patterns due to low-frequency spurs. In this design, since the BLE packet is already whitened and data 1s and 0s are approximately equal in a packet, only the total averaging time will affect the frequency accuracy after calibration.

The DCW is the phase error difference between the reference phase and the output phase with one loop delay in the PLL and multiplied with a gain factor. Thus, it corresponds to the period jitter of the system and the instantaneous frequency variation (IFV) sampled at every reference cycle. An average of the DCW over a certain period of time represents the N-period average jitter (NPAJ). Using the same method as in [15]–[18], we can derive period jitter and NPAJ's relationship to PN

$$\sigma_f^2 = f_0^4\sigma_{\tau_{\rm pr}}^2 = \frac{2f_0^2}{\pi^2}\int_0^\infty \mathcal{L}(f)\sin^2\left(\frac{\pi f}{f_0}\right)df \tag{6}$$

$$\sigma_{f_{\rm AVE}}^2 = f_0^4\sigma_{\tau_{\rm prAVE}}^2 = \frac{2f_0^2}{\pi^2N^2}\int_0^\infty \mathcal{L}(f)\sin^2\left(\frac{\pi fN}{f_0}\right)df \tag{7}$$

where σ_f^2 is the IFV, $\sigma_{\tau_{\rm pr}}^2$ is the period jitter, and $\mathcal{L}(f)$ is the PN of the PLL. For (7) $\sigma_{f_{\rm AVE}}^2$ is the averaged frequency variation (AFV) over N periods averaging time and $\sigma_{\tau_{\rm prAVE}}^2$ is the NPAJ. In the typical "calibrate and open-loop" scheme, the DCW and the IFV in real-time are random processes normally following a Gaussian distribution. After frequency calibration of the PLL, the "releasing frequency" could be anywhere within $\pm 3\sigma_f$ of the carrier frequency with a specific DCW controlling the VCO. With the APU, the VCO is controlled by the $\rm DCW_{AV}$ following a new Gaussian distribution whose standard deviation is $\sigma_{\rm f_{AVE}}$. If with a certain amount of average processing time the $\sigma_{f_{\rm AVE}}$ can be significantly smaller than σ_f, then the APU embedded in the ADPLL will provide a more accurate "releasing frequency" for the TX to do the open-loop transmission. In frequency domain, the APU can be viewed as a digital lowpass filter that processes the DCW with the following transfer function:

$$H_{\rm APU}(f) = \frac{\sin(N\pi f)}{N\sin(\pi f)}. \tag{8}$$

But since the APU's operation in filtering noise associated with the DCW is not real time, we will still use the time domain analysis to evaluate the effectiveness of the APU in this article.

Previous study [14] shows that different PN profiles have a different impact on the frequency averaging effect. We can simplify the PN profile of the PLL to be superpositions of three kinds of noises: 1) the flat PN profile; 2) the white PN profile whose value follows $1/f^2$; and 3) the flicker PN profile whose value follows $1/f^3$. The AFV's relation to PN under these conditions are

$$\sigma_{f_{\rm AVE}}^2 \approx \begin{cases} \dfrac{f_0^2\mathcal{L}_0}{\pi^2N^2}\left[f_{\rm BW} - \dfrac{\sin\left(\frac{2\pi f_{\rm BW}N}{f_0}\right)}{\frac{2\pi N}{f_0}}\right] (1) \\ \dfrac{\mathcal{L}_s f_0 f_s^2}{N} (2) \\ \mathcal{L}_s f_s^3\left[3 - 2\gamma - 2\ln\left(\dfrac{2\pi Nf_{\min}}{f_0}\right) + o\left(f^2\right)\right] (3) \end{cases} \tag{9}$$

where $\mathcal{L}_0$ is the noise floor for flat PN, f_0 is the carrier frequency, $\mathcal{L}_s$ is the sampled PN at f_s offset, $f_{\rm BW}$ is the system bandwidth, $f_{\min}$ is the lower integration boundary for flicker noise, $\gamma \approx 0.5772$ is the Euler-Mascheroni constant, and $o\left(f^2\right)$ means higher order terms which could be neglected.

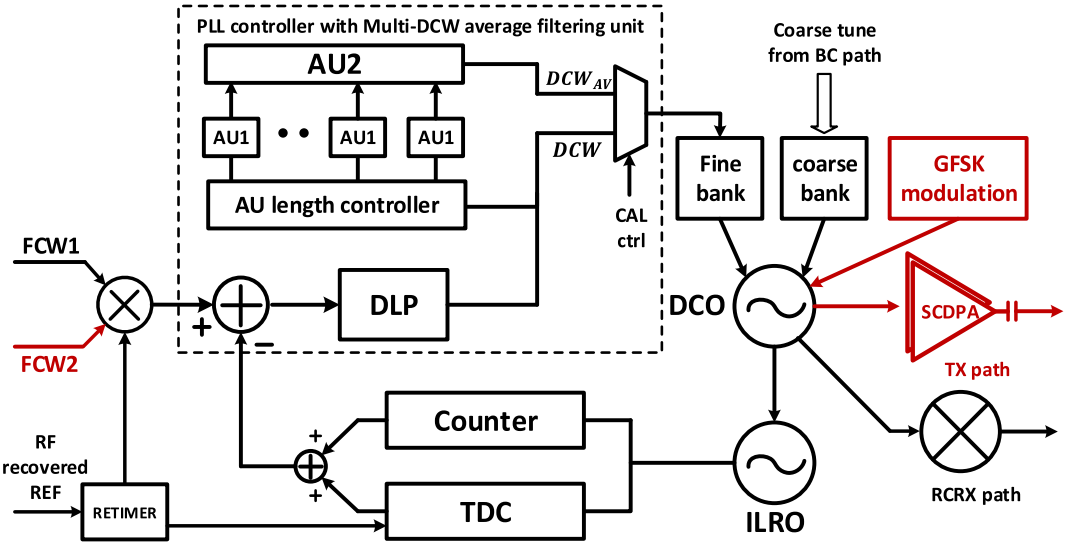

Fig. 7. Block diagram of the proposed ADPLL with embedded APU.

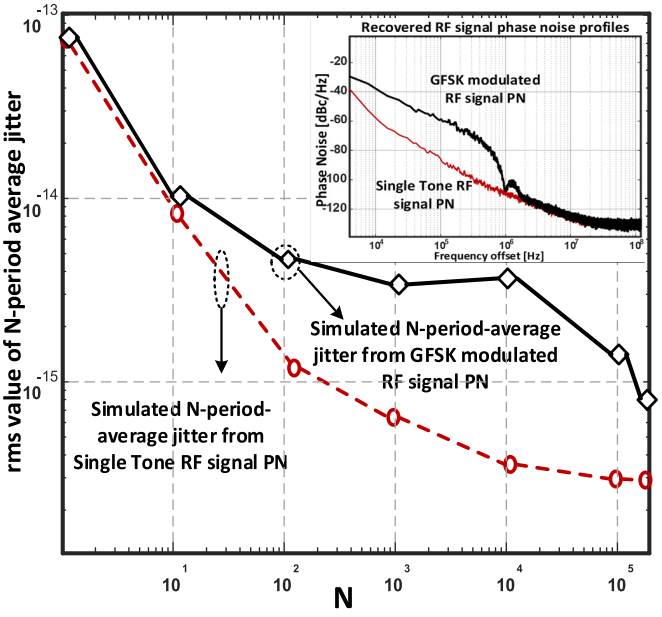

Fig. 8. Simulated frequency averaging effect with different noise profiles.

Equation (9) shows that the AFV scales down with N^2 for flat PN and scales down with N for white PN. It only scales down with $\ln(1/N)$ for flicker PN, basically unchanged over time.

For the PLL in steady state, it is the flicker noise from the reference that eventually dominates the averaged frequency accuracy for when the VCO is set to open loop. All other noise sources in various formats could be averaged out providing enough processing time. In this sense, the frequency modulation's effect on the RF reference could be canceled to some extent as shown in Fig. 8, as long as two conditions are satisfied: 1) the probability of 1s and 0s are approximately equal and 2) there is enough processing time for the APU.

Two RF reference sources are modeled in the simulation. One reference is a single tone RF signal (in red) directly coming from an open-loop *LC* oscillator at 2.4 GHz while the other is GFSK-modulated (in black) to represent a general BLE packet's PN profile. It has a 1 Mbps data rate and a 500-kHz frequency deviation with randomly generated bits. As shown in Fig. 8, with different lengths of averaging time N, the AFV changes dramatically. For the single tone case with small Ns where the noise profile is flat, the AFV reduces with N^2, and when in the white PN region, the AFV changes with N. At the time associated with the flicker noise corner, the AFV changes very slowly. As the PN for both the single-tone and GFSK-modulated cases is eventually converging, the AFV plot also follows that convergence when the averaging time N is large enough.

In this design, the APU's averaging time is limited to the BLE packet length and the PLL's settling time. The ADPLL's bandwidth is programmable, ranging between 20 and 100 kHz. A smaller PLL bandwidth will reduce the RF reference's noise impact (especially for the TX PLL), but would also increase the settling time within that 300-μs frame. The minimum PLL bandwidth is defined by the total of PLL settling time and APU averaging time, while the maximum PLL bandwidth is defined by the fine DAC tuning range of the LCVCO. As for the incoming BLE packet for frequency calibration, the available calibration time is around 300 μs and the APU averaging time is at least tens of μs according to the flicker noise corner of the reference.

The ADPLL uses a 12-phase injection-locking ring oscillator (RO) as the TDC so that no further normalization in calculating frequency error is needed. Since the PLL is designed for low bandwidth and the noise from the RF reference is higher than a typical MHz XO, the in-band PN is dominated by the reference even though the TDC is only 3.5 b and the LCVCO's quantization noise would not affect the PLL's overall performance either.

Fig. 9 shows the time domain waveform comparing the IFV and AFV with a histogram plot of the APU's effect with different averaging times. When the single tone RF reference is used, the improvements of frequency accuracy

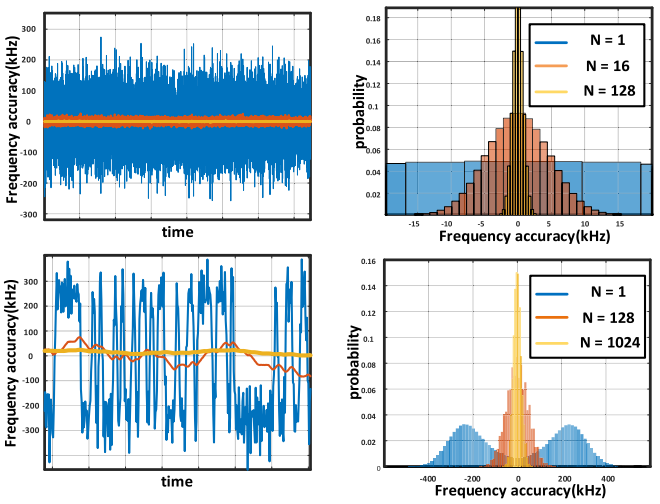

Fig. 9. Simulated frequency averaging effect of the APU with different types of reference in the time domain and corresponding histogram.

is significant even if the averaging time is small. However, if the reference is modulated, with practical averaging time, the improvements are not as effective as with the single tone input as demonstrated in Fig. 8. When $N = 1024$ with the 8-MHz reference frequency in this design, the necessary averaging time is 128 μs, and the frequency can be easily calibrated into the $\pm$150-kHz frequency offset required for the BLE standard in packet transmission. When the averaging time is 16 μs with $N = 128$, there will be around a 3% chance that the frequency offset will be larger than required. In order to achieve $6\sigma < \pm 150$ kHz with at least 99% possibility using a GFSK-modulated reference, the APU averaging time should be at least 256 cycles (32 μs with the 8-MHz recovered reference) after locking. Together with a 20-kHz TX PLL bandwidth, the total frequency calibration time can be controlled within 100 μs.

E. ULP BLE TX

The ultralow-power BLE TX is turned on at the same time as the reference recovery RX, to avoid further frequency fluctuation caused by pulling between the TX and the RX. It uses an open-loop direct GFSK modulation. The modulator is clocked by the divided clock of the TX VCO after calibration and is good enough for the baseband clock. The overall design of the TX is similar to [5], using a class-D switched capacitor digital PA with a high impedance matching for high PA efficiency targeted at -10-dBm output power.

III. Circuit Implementation

As discussed in Section II, the NF of the receiver path will add up to the PN of the RF reference, thus, the typical LNA first architecture is used for both receivers. The BCRX uses a zero IF architecture and the reference recovery RX uses a low IF architecture. Fig. 10(a) shows the schematic of the narrowband LNA and the passive mixer used in this design. After being mixed down, the signal passes through a third-order low pass filter with a bandwidth of 1 MHz and

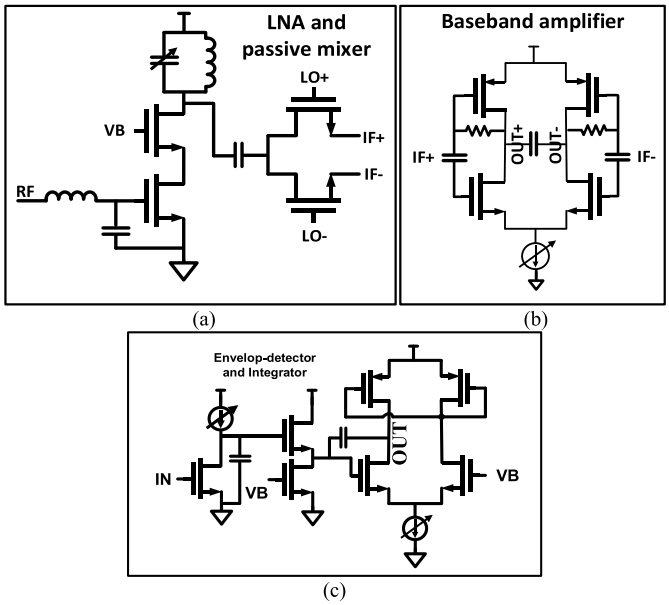

Fig. 10. Circuit design for the BCRX path. (a) LNA and mixer. (b) Baseband amplifier. (c) Envelope detector and integrator.

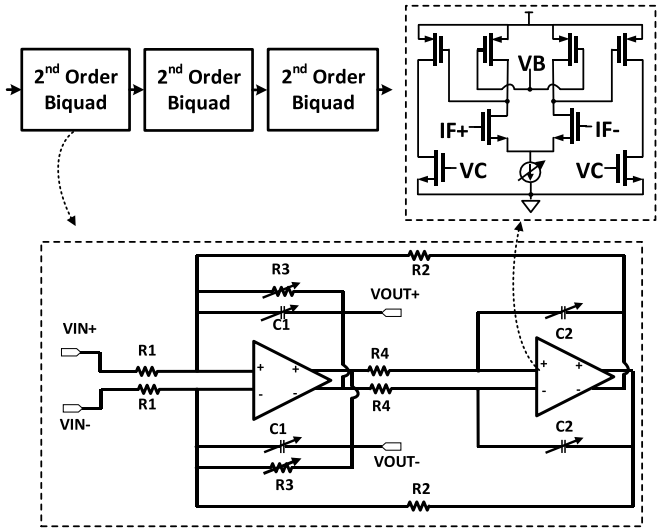

Fig. 11. Sixth-order bandpass filter block diagram and schematic.

is then amplified by a baseband gain stage. Fig. 10(b) shows the schematic of the baseband gain stage and the envelope detector for the BCRX. The baseband amplifier is designed with three stages that provide up to 70-dB gain. The baseband amplifier is ac coupled to remove the dc offset. An envelope detector followed by an integrator is then used to rectify and integrate the signal, as shown in Fig. 10(c). Finally, the signal is digitized using a one-bit comparator clocked at 250 kHz. This 250-kHz clock is divided from the RX VCO when it is in open loop status.

The reference recovery RX shares the same LNA and mixer as the RF front end, but instead of using a 1-MHz low pass filter, it utilizes a 6th-order bandpass filter at 8 MHz with 2-MHz bandwidth in order to remove adjacent channel blocks. Fig. 11 shows the block diagram and schematic of the bandpass filter. It uses a cascade of three 2nd-order biquad to offer a sharp filtering [22].

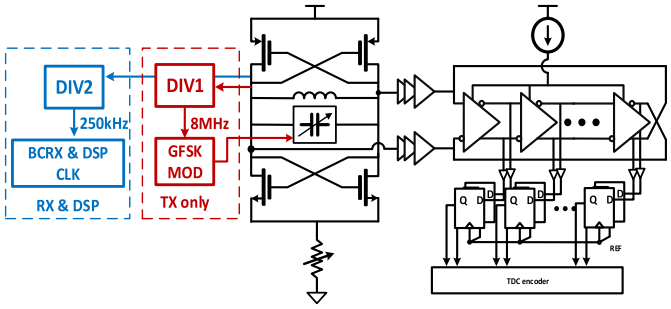

Fig. 12. Design of the LCVCO with the injection-locked RO TDC with different control for TX path and RX path.

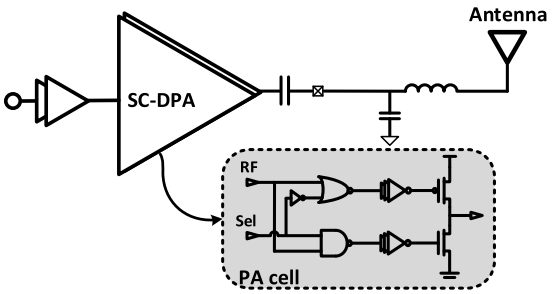

Fig. 13. Switched-capacitor digital PA for TX.

Fig. 12 shows the schematic of the LCVCO used for both RX and TX PLLs, together with a simplified block diagram of the RO-based injection locking TDC. The LCVCO is using a typical CMOS architecture with both NMOS and PMOS cross-coupled pairs as the negative resistance stage and a digitally tuned resistor tail. The tail resistor helps prevent the transistors from entering the triode region and the tank from seeing a low impedance path, which improves the PN performance [23]. Although it wastes some voltage headroom compared to LCVCOs with degenerated *LC* tanks, the switchable resistor in the source of the transistor saves a significant amount of area. Compared to the degenerated current source, it also saves an extra bias control. For the TX VCO, it is divided to 8 MHz for the GFSK modulator, while for the RX VCO, it is divided to 250 kHz as a baseband clock for both the BCRX comparator and the DSP. The injection-locking RO TDC is also shown in Fig. 12. It has six pseudo-differential RO cells providing 12 TDC phases, which results in roughly −80 dBc/Hz in-band PN with an 8-MHz reference clock.

The PA for the ULP BLE TX is shown in Fig. 13. It uses a class-D switch-capacitor architecture due to its robustness, low cost, and great performance in efficiency. Compared to other switching power amplifiers, it is more robust and less susceptible to driving transistor parasitics, PVT variations and matching and it can benefit from advances in technology scaling with better switches. A high impedance is used to achieve high PA efficiency in low output power levels. The SCDPA is thermometer coded with 8-bit cells and is optimized for the highest efficiency for −10-dBm operation.

IV. Measurement Results

The asymmetric BLE transceiver was fabricated in a 40-nm CMOS process. Fig. 14 shows the full measured waveforms for the transient operation of the transceiver detecting an ADV event, recovering the 8-MHz reference, then transmitting a packet. In this measurement, three consecutive BLE packets (Ch.37 → Ch.38 → Ch.39) are sent to the test chip, and the incoming packets are highlighted in light blue, as shown in Fig. 14. The packet length is 300 μs. Once the BCRX detects the wake-up code from the first two packets (100-100-010-010), the RCRX is turned on after some delays. In the RCRX, the BLE packet is down-converted to 8 MHz using uncertain IF down-conversion with $6\sigma_f = 1$ MHz worst case uncertainty. It is then filtered by a 6th order bandpass filter at 8 MHz with a bandwidth of 2 MHz, removing interferers on adjacent channels. A glitch filter removes short pulses that might exist, e.g., from noise. This signal then becomes the reference for the two PLLs. The clock signal will also be muxed through to the comparator in the BCRX, and the demodulator generates a constant output until the end of the 3rd BLE packet. This servers as a flag signal to see if the reference is generated with enough amplitude. An 8-MHz reference could offer enough PLL bandwidth required for necessary lock time, and it also relaxes the required quality factor for the 2-MHz filter bandwidth. During the whole reference recovery state, the RX PLL remains locked after it settles while the TX PLL will start the embedded APU in the background to collect information for the changing DCW with 10-μs guard time after locking detect. This will ensure that the APU starts from a steady state. For this demonstration, the APU averaging time is set to 256 reference cycles in 32 μs. As shown in Fig. 14, the "releasing" frequency after calibration using the embedded APU settles in the middle even when the recovered reference is frequency-modulated. After a programmed delay, the TX transmits a valid BLE packet using direct modulation with the divided-down signal by itself as the baseband clock. Using two LOs allows for receiving and transmitting on different BLE channels and for optimizing each PLL controller.

Fig. 15 shows the measured frequency drift of the LCVCO when open loop in the TX transmission states for 1 s under room temperature and 16 h in the temperature chamber. The measured frequency drift is less than ±17.5 KHz which is within the required ±50 kHz from the BLE standard. Fig. 16 shows the measured LO frequency drift over temperature and bandpass filter's temperature performance including its center frequency and bandwidth. The open-loop TXLO will drift for more than 10 000ppm across temperature, but the TXLO will always be calibrated through RCRX before any transmission, this drift is tolerable. For the bandpass filter, the center frequency drift due to temperature change can also be calibrated through capacitor tunings, as illustrated in Fig. 16(b) and (c).

The measured sensitivity is −94 dBm for the BCRX [Fig. 17(a)] and −86 dBm for the RCRX using BER approximation [Fig. 17(b)], thus, the whole transceiver's sensitivity is set by the RCRX. The measurement is based on energy detection while the recovered reference clock signal is muxed to the comparator in the BCRX path. This is to approximate the real RCRX sensitivity while it can generate a valid rail-to-rail clock signal for the PLL in the digital domain. The digital V_{DD} in this test is 0.9 V and the comparator threshold is set

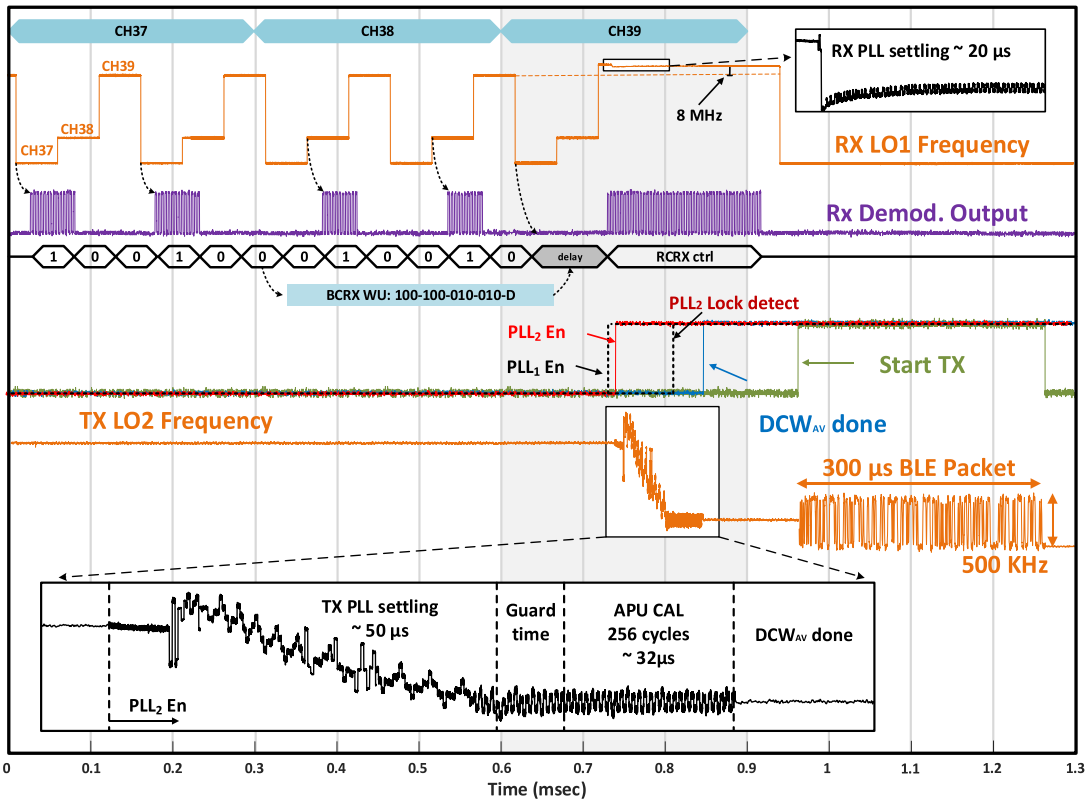

Fig. 14. Measured transient waveforms of the system operation and TX/RX LOs frequencies in calibration and transmission.

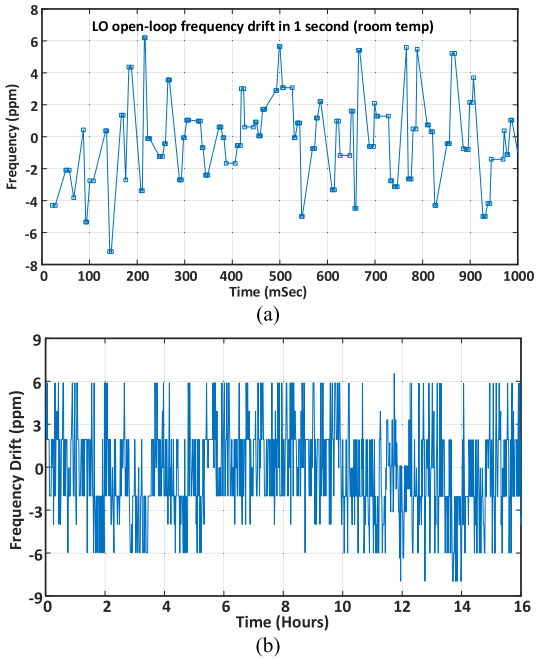

Fig. 15. TXLO open-loop measured drift for (a) 1 s in room temperature and (b) 16 h in temperature chamber.

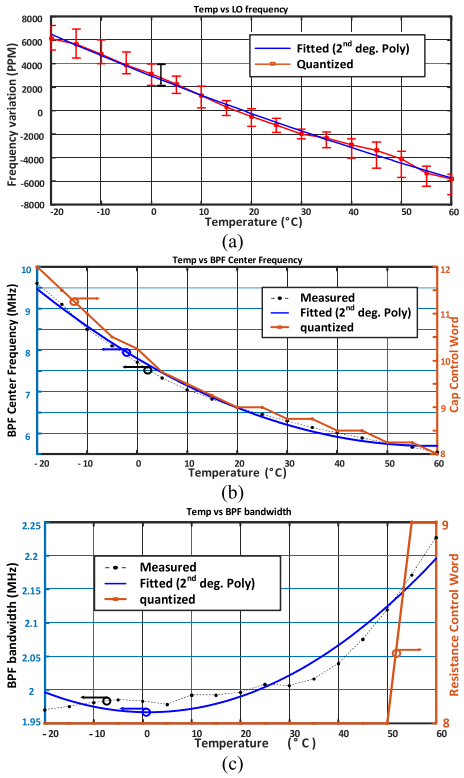

Fig. 16. Temperature performance of the LO and BPF. (a) Frequency variation versus temperature. (b) BPF center frequency versus temperature. (c) BPF bandwidth versus temperature.

to above 0.5 V considering there are extra glitch filters and buffers for the clock. In the measurement of the transceiver functionality, system failure is observed at around −86 dBm as well when the recovered clock is not valid for the ADPLLs. Simulation result based on numerical models of the whole system shows a close to −90-dBm sensitivity when NPAJ is compared to BLE standard and the APU averaging time is set to 256 [Fig. 17(c)]. The adjacent channel rejection (ACR) when receiving back-channel messages [Fig. 17(d)] was measured to be −18, −51, and < -60 dB for the 1st, 5th, and 10th

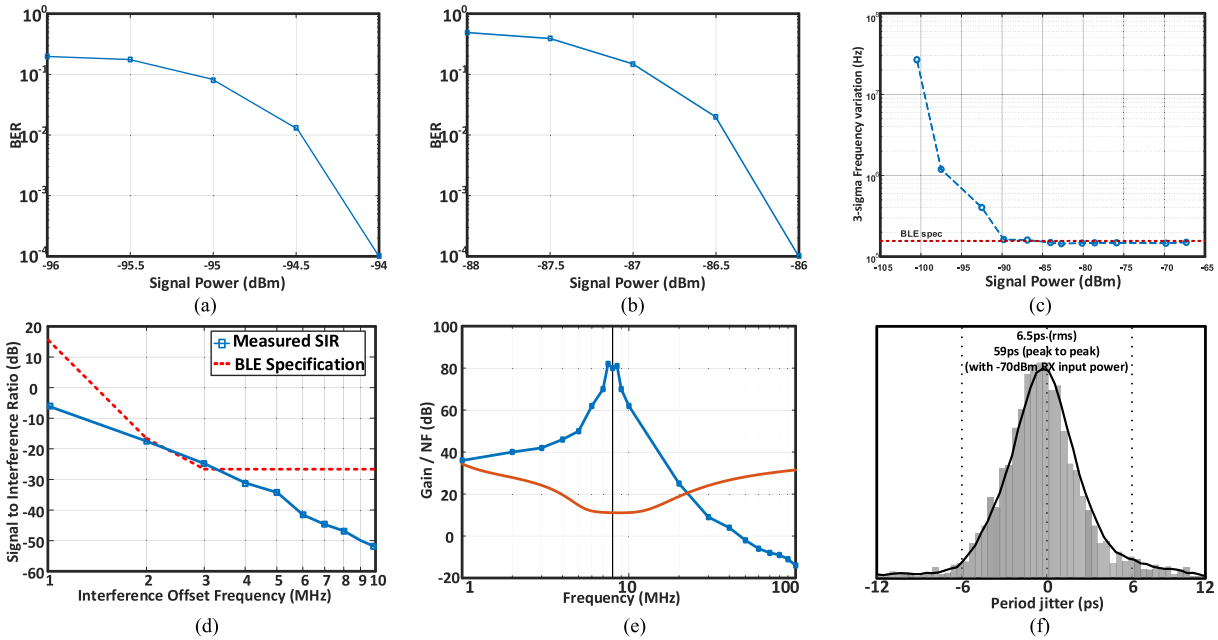

Fig. 17. RX measurement results. (a) BCRX BER versus signal power. (b) RCRX BER versus signal power. (c) Simulated NPAJ versus signal power for RCRX using numerical model. (d) Signal-to interference ratio versus interference offset frequency for BCRX. (e) RCRX RF front-end gain and NF. (f) Received 8-MHz clock jitter.

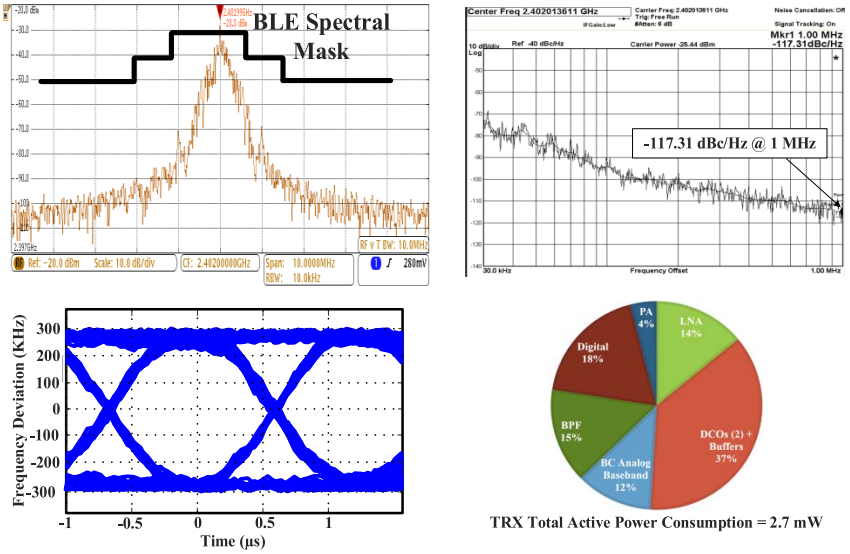

Fig. 18. Measurement results: TX output spectrum, eye diagram, phase noise, and transceiver power breakdown.

adjacent channels, respectively. The ACR when recovering a reference clock is −20 dB and <−60 dB for the 1st and 2nd adjacent channels, respectively [Fig. 17(e)]. The NF of the clock-recovery path is less than 12 dB. This is critical to minimize rms jitter in the recovered clock, which is measured at 6.5 ps when the RX signal power is −70 dBm [Fig. 17(f)].

The GFSK TX output spectrum is shown in Fig. 18 along with the BLE spectral mask. The measured eye diagram of the TX output packet is shown in Fig. 18, where the clock driving the GFSK modulator is divided down from open-loop RX LO1. The free-running LCVCO archives −117-dBc/Hz PN at 1-MHz offset. The overall power breakdown of the TRX shows that the RF LOs and buffers consume the highest power percentage (37%) of the total active power of 2.7 mW.

Table I shows a comparison between this work and state of the art. This is the first reported crystal-less transceiver, where both the received and transmitted messages are compliant with the same communication standard (BLE). This work has the fastest reported frequency calibration time of all crystal-less radios. It outperforms previous designs in interference rejection through high-Q filtering and by enabling PLLs only after detecting a valid ADV event when a BLE packet is known to be present. Fig. 19 shows the die photo of the chip, which has an area of 1.33 mm^2.

TABLE I
COMPARISON TO THE STATE OF THE ART

		This Work		VLSI 2019 [11]	VLSI 2019 [10]	TCAS-I 2012 [19]	JSSC 2018[9]**
		TX	RX				
Active Power [mW]	Analog	0.6	1.6	1.9	3.9	20.4	0.92**
	Digital	0.5					
RF Frequency [MHz]		2402-2480	2402-2480*	2400	2400	2400	2100-2500
Voltage Supply [V]		0.6/1		1.5	1.3-1.6	1.8	<0.45
Sensitivity [dBm]		N/A	-86***	-83.5	N/A	-65	NA
Modulation		GFSK	BC-FSK	GFSK(TX)/ OQPSK(RX)	GFSK	QPSK	GFSK
Die Area [mm^2]		1.33		3.06	N/A	2.7	0.24
Adjacent Channel SIR (dB) @ 2/3MHz		N/A	-18/-24****	N/A	N/A	N/A	N/A
Channel Selectivity		Yes*	Yes	Yes	N/A	No	Yes
Technology [nm]		40		65	65	180	16 FinFET
Frequency Calibration Method		Received BLE Packet		Received 802.15.4 Packet	FBAR	Received QPSK Signal	On-chip RTC
PLL Locking Time [µs]		50	15	N/A	N/A	90	0.1
Comm. Standard (TX/RX)		BLE/ BC-BLE		BLE/ 802.15.4	BLE/ N/A	No/ N/A	N/A**
Additional Components required		TX Matching network		None	FBAR	RF filter	N/A**

*preset with FCW for single transmission after each calibration. ** only PLL is presented in this design. *** set by RCRX and measured based on BER approximation
**** Measured based on BER

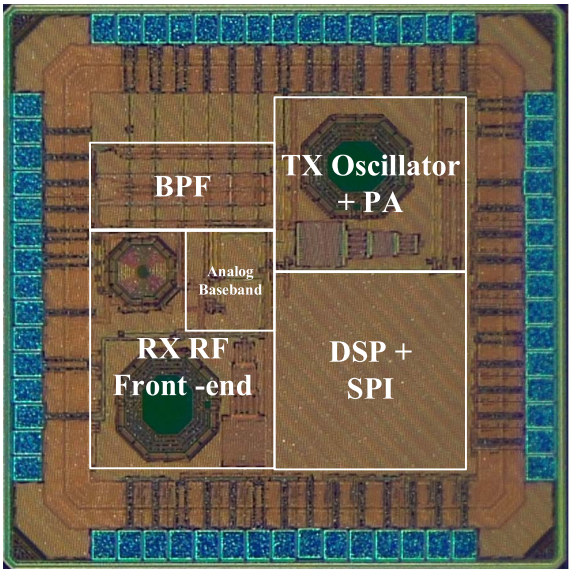

Fig. 19. Die photo of the proposed XO-less BLE transceiver.

V. CONCLUSION

This article presents an asymmetric crystal-less BLE transceiver with over-the-air clock recovery that is compliant with the BLE standard. The dual-ADPLL architecture for separate RX and TX paths enables all-channel transmission capabilities while recovering a clock from patterned ADV channel packets. The BCRX wakes up the system and prevents false frequency locking from potential interference, and the embedded APU in the ADPLL enables the RX to recover a clock from GFSK-modulated signals within one BLE packet time. Compared to other state-of-the-art designs, this prototype fully removes the crystal by using RF reference recovery and achieves the fastest frequency calibration when using only BLE compliant messages.

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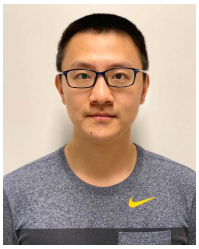

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