# An 85 nW IoT Node-Controlling SoC for MELs Power-Mode Management and Phantom Energy Reduction

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***Abstract*—This paper presents an ultra-low power (ULP) node-controlling system-on-chip (SoC) used for power-mode management and phantom energy reduction of miscellaneous electric loads (MELs). The SoC is powered from a single 2.5 V voltage supply enabled by the integrated power management unit (PMU) and can control up to 16 MELs due to the on-chip 16-channel correlator and the 32b RISC-V microprocessor. To further reduce the system power consumption, two clock domains have been adopted for the correlator and the processor separately. Fabricated in 65-nm CMOS, the measured minimum power consumption of the proposed SoC is only 85 nW at 0.45 V voltage supply and 1 kHz clock frequency. The measured maximum operating frequency can go up to 148 kHz with a 0.55 V supply. An application experiment successfully demonstrates that the SoC controls the power modes of MELs from wake-up to cut-off to save the average power and phantom energy.**

***Keywords—ultra-low-power, system-on-chip, miscellaneous electric loads, wake-up, power-mode management, phantom energy reduction.***

## I. Introduction

Miscellaneous electric loads (MELs) are electric appliances that plug into outlets, like coffee makers, printers, televisions, etc. The power consumption of MELs is significant, accounting for 30% of total electricity consumption in residential buildings and 36% in commercial buildings according to the U.S. Department of Energy (DoE) [1]. More importantly, those MELs still consume watt-level power even if they are turned off, which is called phantom energy by the DoE. These loads are projected to increase over the next decade, and the next generation of MELs require zero energy consumption when they are off and wireless communication to manage active, standby, and non-active modes to save power further. However, a large portion of the MELs are comprised of consumer electronic devices, which are traditionally not focused on reducing energy consumption at the device-level.

This work aims to provide a solution to effectively control the power modes of MELs when they are being used and eliminate their phantom energy when they are turned off. As shown in Fig. 1, a wireless wake-up and control system, which includes a wake-up receiver (WuRX), a node controller (this work), and a duty-cycled RF transceiver, can be used to cut the power line of the MELs directly from the outlet power and reconnect them when they are needed by users, detected through sensors or mobiles. After power line connection, the control system should be able to manage the power modes of MELs according to different use cases.

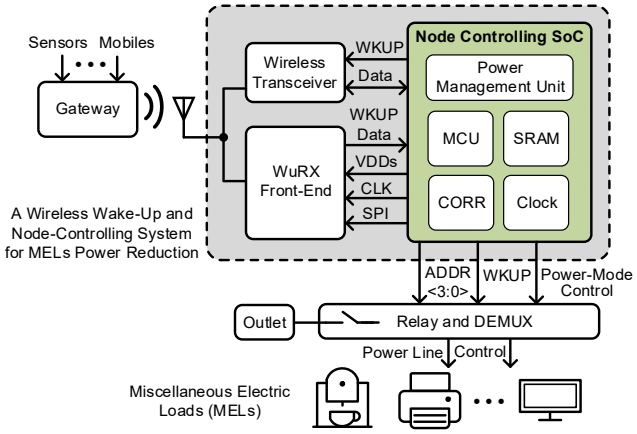


Fig. 1. Block diagram of a wireless wake-up and node-controlling system and its application to reduce power consumption of MELs.

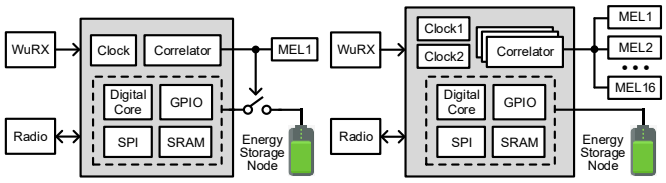


Fig. 2. A traditional duty-cycled controller vs. proposed always-on controller with a multi-channel correlator and dual clock domains.

This application imposes several requirements for the node-controlling system. First, to wake up multiple MELs, the system should have a multi-channel digital baseband, such as correlators, and an address generator to receive the serial data signals from the WuRX and wake up a specific MEL. Second, as an always-on system, the power consumption of the controller should be optimized to be as little as possible to meet the system power budget. Third, for a real deployment, the whole wake-up and controlling system should be powered from a single voltage supply, so internal voltage regulators should power both the controller and WuRX. Previous controlling systems either consume too much power [2] or do not include any correlators for the wake-up control [3] [4], which are not suitable for this application.

In this paper, we present a node-controlling system-on-chip (SoC), which is specifically designed for MEL power reduction. Fabricated in 65-nm CMOS, the system minimum power consumption is only 85 nW at 0.45 V and 1 kHz, and it can control up to 16 MELs with the multi-channel correlator and the on-chip microprocessor. An example application is presented, showing that the system can successfully control the power modes of MELs and reduce their power consumption.

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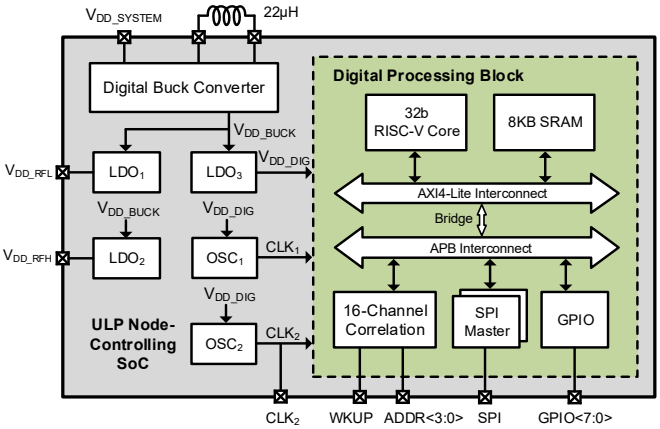



Fig. 3. System block diagram of the proposed node-controlling SoC.

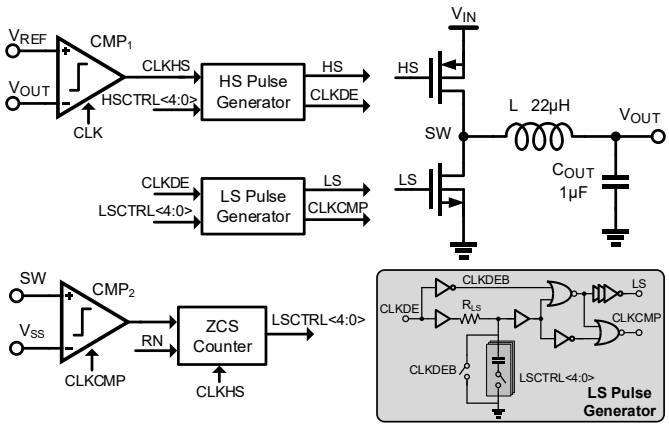



Fig. 4. Block diagram of the digital buck converter.

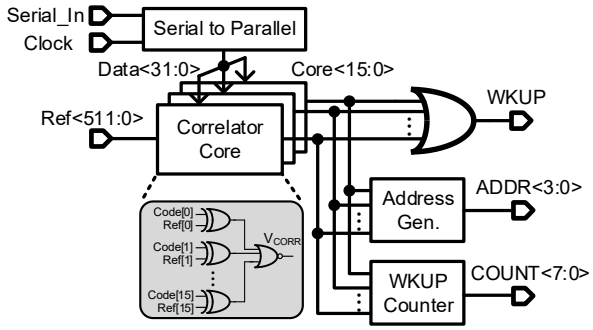



Fig. 5. Block diagram of the 16-channel correlation block.

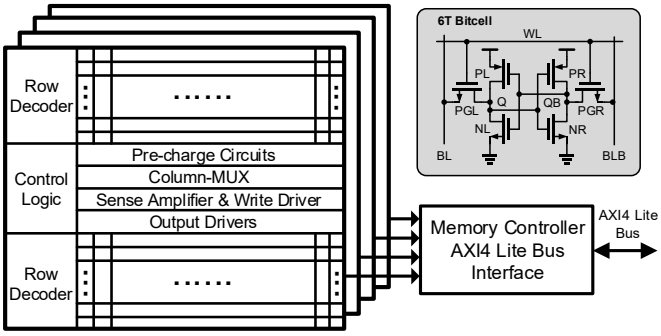



Fig. 6. Block diagram of the 6T SRAM.

## II. Architecture of the Node-Controlling SoC

Figure 2 shows the architecture of the traditional node controller, which is duty-cycled to save energy and can be woken up from a WuRX. A traditional single-channel digital baseband is not suitable for the multiple appliance wake-up and management application. In this work, we improve the traditional architecture through the following four aspects. First, by making the digital circuits and SRAM work in the subthreshold (sub-$V_T$) region, a nW-level digital processing block, including a MCU and a correlation block, has been achieved. With such low power, we can make the controller work in an always-on mode and eliminate the need to wake up the MCU, which otherwise may consume significant energy and time to restore SRAM data when it powers on after being duty cycled off. Second, instead of one correlator, we integrate a 16-channel correlator to control up to 16 MELs and generate the address signals. Third, two clock domains have been adopted for the correlator and MCU separately to save more power since the correlator clock frequency needs to match the WuRX baseband frequency, which could be much higher than the digital processing frequency of the MCU for the MEL control application. Fourth, to easily integrate with a WuRX, the proposed SoC generates the voltage supplies, clocks, and Serial Peripheral Interface (SPI) for the WuRX eliminating the need of extra components to make the WuRX work.

Figure 3 shows the system block diagram of the proposed node-controlling SoC, which includes a 32b RISC-V core and IOs, an 8 KB SRAM, a correlation block, two ring oscillators, three low-dropout regulators (LDOs), and a digital buck converter. The two clocks adopt the current-starved ring oscillator structure to increase the power efficiency.

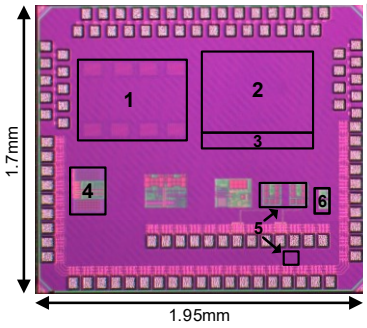
## III. Components Design

### A. Microprocessor and Peripherals

The main controller on the SoC is a BottleRocket 32-bit RISC-V microcontroller class processor core, which is a customized microarchitecture built from components of the Free Chips Project Rocket core [5]. It utilizes a basic 3-stage pipeline and implements the RV32IMC Instruction Set Architecture (ISA). It interfaces to a custom ARM AMBA AXI4-Lite interconnect, which then interfaces to the 8 KB SRAM and an ARM AMBA APB interconnect to support peripherals. The peripherals include an 8-bit General Purpose Input Output (GPIO) interface, 2 SPIs, and a 16-channel correlator. The microprocessor and its peripherals are designed to operate at 0.45 V in the sub-$V_T$ region and use standard cells with high-$V_T$ devices to minimize the leakage and total power consumption.

### B. Power Management Unit

To power the SoC from a single voltage supply, a power management unit (PMU) is designed including a digital buck converter and three LDOs. The buck converter converts the 2.5 V system voltage supply to 1 V to power the three LDOs. $LDO_1$ and $LDO_2$ are used to power the WuRX with an output voltage from 0.2 to 0.7 V. $LDO_3$ generates the voltage supply




| Components | Area ($mm^2$) |
|---|---|
| 1. SRAM | 0.29 |
| 2. Digital core and IOs | 0.36 |
| 3. Correlation | 0.045 |
| 4. Buck converter | 0.05 |
| 5. LDOs | 0.044 |
| 6. Clocks | 0.007 |
| Total | 0.796 |

Fig. 7. Chip micrograph and area breakdown.

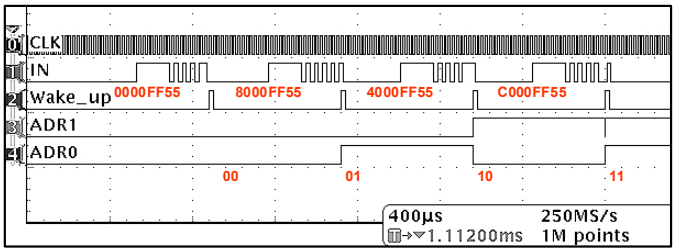



Fig. 9. Measured wake-up signals for the first 4 channels of the correlator.

for the digital processing block and the two clocks. The LDOs adopt an amplifier-based analog structure to minimize the output ripple and noise.

Figure 4 shows the block diagram of the buck converter, which adopts a hysteresis control scheme with discontinuous conduction mode (DCM). The two strongARM comparators, $CMP_1$ and $CMP_2$, regulate the output voltage and perform zero-current detection, respectively. A digital zero-current detector [6] has been adopted with a 5-bit tuning ability. Whenever the $V_{REF}$ is lower than $V_{OUT}$, it triggers the two comparators and generates two pulse signals, HS and LS, to control the power transistor. This buck has a low design complexity and can achieve low quiescent current with a simulated value of 2.5 nA, which is suitable for powering ultra-low-power (ULP) loading circuits.

### C. Correlation Block

The schematic of the correlation block is shown in Fig. 5, which includes a 16-channel correlator core, a serial-to-parallel block, an address generator, and a wake-up counter. Each correlator core has 32 comparison bits. The output of the correlation system connects to the system bus, so the wake-up information can be directly processed by the MCU. The correlator clock frequency is determined by the data rate and oversampling rate of the wake-up system, so it is separated from the MCU to save power. The wake-up counter can count the total number of wake-up signals during a selected time period for each address.

### D. SRAM

The block diagram of the SRAM is shown in Fig. 6. The memory-mapped 8 KB SRAM in the system serves as both the instruction and data memory. The memory is custom-designed for self-powered systems with a high-$V_T$ 6T bitcell offering substantial power savings. The SRAM includes four 2 KB

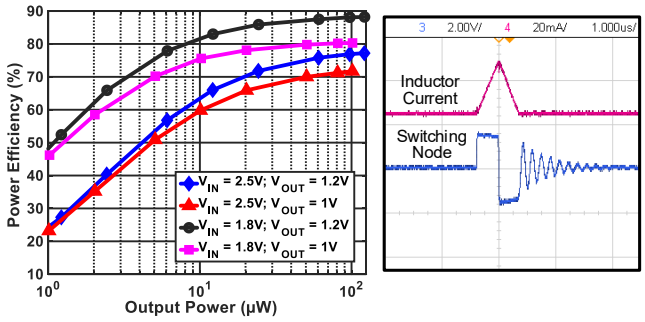



Fig. 8. Measured buck converter power efficiency and transient waveform on the switching node.

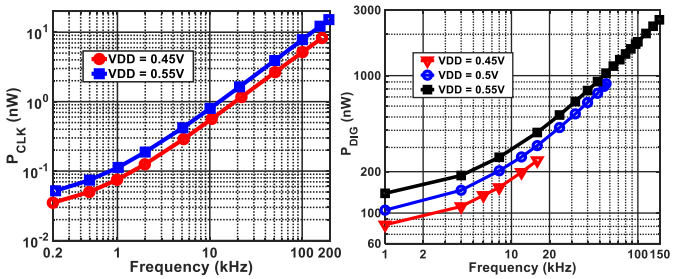



Fig. 10. Measured clock power vs. frequency and measured digital processing block power vs. frequency.

TABLE I: MEASURED POWER BREAKDOWN OF THE SOC

| | RISC-V Core + IO | SRAM | Correlators | 2 Clocks | 3 LDOs | Total |
|---|---|---|---|---|---|---|
| Power (nW) | 33.7 | 41.1 | 7.4 | 0.15 | 2.65 | 85 |
| | @ $V_{DD}$ = 0.45 V, $F_{CLK}$ = 1 kHz | | | | @ $V_{IN}$ = 1 V $V_{OUT}$ = 0.45 V | |

banks and each bank includes 2 sub-banks. Each of the sub-banks shares the same peripheral circuitry, offering improvements in speed, area, and leakage. The memory interacts with the microprocessor through the embedded memory controller that implements the AMBA AXI-4 lite bus protocol. The interface supports partial data transactions. The built-in control logic enables a modular memory interface supporting the majority of the bus protocols, including the ARM Cortex and the RISC-V processors.

## IV. EXPERIMENTAL RESULTS

The node-controlling SoC is fabricated in a bulk 65-nm CMOS process with an active area of 0.8 mm2, which is shown in Fig. 7. First, we show the performance measurements of each component in the SoC, and then we use the SoC to demonstrate an application that controls the power modes of a MEL to reduce its power consumption.

### A. Performance Measurements

The measured power efficiency of the buck converter and the transient waveform of the switching node is shown in Fig. 8. When $V_{IN}$ = 2.5 V, $V_{OUT}$ = 1 V, and clock frequency is 2.6 MHz, the maximum power efficiency is 71.7%, and when $V_{IN}$ = 1.8 V, $V_{OUT}$ = 1.2 V, and the clock frequency is 2.8 MHz, the maximum power efficiency is up to 88.2%. The power loss is mainly due to switching losses at low output power. The measured current consumption of the LDOs is about 0.88 nA per LDO, and they have a dropout voltage of about 300 mV.

TABLE II: COMPARISON WITH STATE-OF-THE-ART ULP SOCS

| | This work | [4] VLSI'17 | [3] ISSCC'15 | [2] ISSCC'15 |
|---|---|---|---|---|
| Technology (nm) | 65 | 130 | 65 | 130 |
| Controller Architecure | RISC-V | N/R | ARM Cortex M0+ | MSP430 |
| Regulated Voltages (V) | 0.2 - 0.7 | 1.8, 1, 0.5 | 0.25 - 1.2 | 0.5, 1.2 |
| Operating Frequency (kHz) | 1 - 148 | 32 | 29 - 66000 | 187.5 - 500 |
| On-Chip SRAM | 8KB | 4KB | 24KB | 12KB |
| On-Chip Correlator | 16-channel | No | No | No |
| Total Power (nW) | 85 @0.45V, 1kHz | 507 @N/R | 850 @0.25V, 16kHz | 2270 @0.5/1.2V, 200kHz |
| Components Included in the Total Power | MCU + Correlator + IO + SRAM + LDO + Clock | MCU + SPI + IO + Timer + GPIO + RI | MCU | MCU + IO + SPI + FIR |

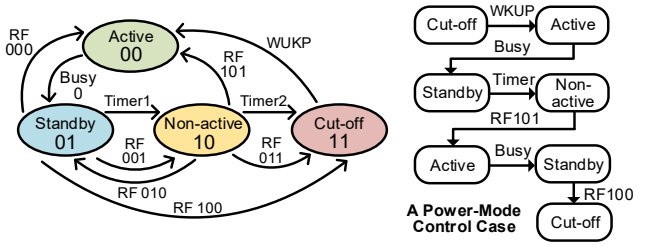



Fig. 12. State transition diagram of the power-mode control and a power-mode control case for demonstration.

Figure 9 shows the measured wake-up waveform for the correlator, where four groups of wake-up codes at the input cause four wake-ups at the output, spanning the binary addresses from 00 to 11. Fig. 10 shows the measured power of the clock and the digital processing block, including the RISC-V core and IOs, the SRAM, and the correlator. The clock has a frequency range up to 200 kHz with a lowest power of only 35 pA at 0.45 V and 200 Hz, which is very power efficient. The measured power consumption of the digital processing block is 82.1 nW at 0.45 V and 1 kHz for the MEL control application. Table I shows the measured power distribution of the node controlling SoC including the quiescent current of the three LDOs. The comparison with state-of-the-art node-controlling SoCs is shown in Table II. Our SoC achieves 85 nW power, which is 5.96× lower than the work in [3], and previous work does not have any correlators, making it unsuitable for wake-up control and phantom energy reduction of MELs.

### B. *Application Demonstration*

To show the proposed SoC can be integrated into a wireless system and work successfully with a WuRX, we connect the SoC with a WiFi-based WuRX chip, whose set-up is shown in Fig. 11. The two LDOs provide 0.2 V and 0.4 V for the WuRX, and the clock frequency of the correlator is set to be 50 kHz. The WuRX is fully powered by the controller including the voltage supplies, the clock, and the SPI for control-bit configuration. A wake-up signal is shown in Fig. 11, which proves that the SoC can fully integrate with a WuRX.

The final goal of this work is to use the on-chip correlator and MCU to wake up the MELs, to control their different power modes, and to cut off the power line when the MELs are turned-off. Fig. 12 shows a state transition diagram of the control program running on the MCU. When there is a wake-up signal, it wakes up the MEL to make it to work in active mode, and then go to the standby mode indicated by the busy signal. There is a 3-bit input from the RF transceiver to change

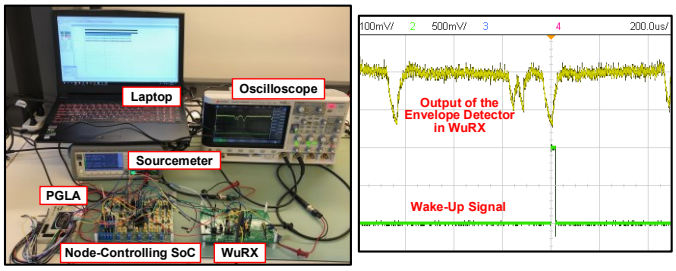



Fig. 11. Experimental set-up of the controlling SoC with a WuRX and measured wake-up signal for the wake-up and controlling system.

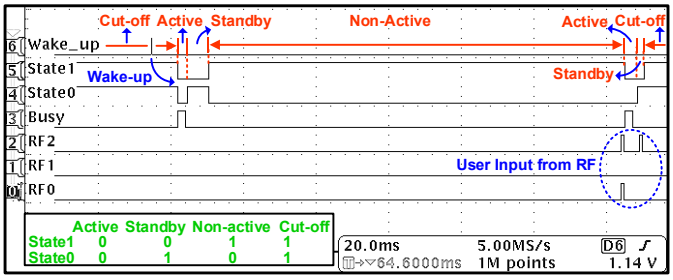



Fig. 13. Measured transient waveform showing the MEL power-mode control.

the power mode of the MEL based on the user need. If there is no input, then the MEL goes from standby, to non-active, and finally to cut-off mode after two timers.

To demonstrate this function, we use a Link Instruments IO3200 pattern generator to simulate the input from RF transceiver and wake-up data from WRX in the experimental set-up. Fig. 12 shows a power-mode control case, where a MEL wakes up from the correlator and finally goes back to the cut-off mode. The measured control waveform from GPIOs is shown in Fig. 13, where state1 and state0 are the two outputs of GPIOs to control the MEL power modes. After a wake-up is detected for the MEL, the MEL state changes from cut-off to active, and the busy indicator is on. After finishing all the tasks, the MEL goes to cut-off again. This application demonstration successfully shows that the node-controlling SoC can control the power modes of the MEL to reduce average power and eliminate its phantom energy.

## V. CONCLUSIONS

To reduce the power consumption of MELs and eliminate their phantom energy, we present an ULP node-controlling SoC that can wake up MELs from cut-off mode and control the power modes using an on-chip MCU and correlators. The measurement results show the minimum power of the system is only 85 nW at 0.45 V and 1 kHz. Two experimental results show that, first, the SoC can be easily integrated with a WuRX, second, the SoC can successfully control the different power modes of the MELs to reduce their average power consumption and the phantom energy.


## ACKNOWLEDGMENT

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## REFERENCES


[1] U.S. Energy Information Administration, AEO2015 Report, https://www.eia.gov/outlooks/archive/aeo15/

[2] A. Klinefelter et al., "A 6.45µW self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2015, pp. 1-3.

[3] J. Myers et al., "An 80nW retention 11.7pJ/cycle active subthreshold ARM Cortex-M0+ subsystem in 65nm CMOS for WSN applications," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2015, pp. 1-3.

[4] F. Yahya et al., "A battery-less 507nW SoC with integrated platform power manager and SiP interfaces," in *Proc. IEEE Symp. VLSI Circuits*, 2017, pp. C338-C339.

[5] K. Asanovic´ et al., "The Rocket Chip Generator," EECS Department, University of California, Berkeley, CA, USA, Technical Report No. UCB/EECS-2016-17, Apr. 2016.

[6] A. Paidimarri and A. P. Chandrakasan, "A Wide Dynamic Range Buck Converter With Sub-nW Quiescent Power," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3119-3131, Dec. 2017.