

# Ultra-Low Power Receivers for IoT Applications: A Review

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**Abstract**— Efficient wireless connectivity is an important requirement for IoT applications and has attracted a lot of research interest recently. The receivers designed for such applications need to be low power while still supporting sufficient communication range and co-existing with other receivers that share the same frequency band. In addition, supporting adopted communication standards is key for ubiquitous integration with the existing infrastructure. This paper presents a review of the recent design trends and techniques in ultra-low power receivers for IoT applications.

**Index Terms**—Low power receivers, Receiver design trade-offs, RF energy detection, mixer-first wake-up receiver, backchannel receivers.

## I. INTRODUCTION

With the coming of age of the Internet of Things (IoT), demand on ultra-low power (ULP) receivers will continue to boost tremendously. Innovations in both the system architecture and circuits implementation are essential for the design of truly ubiquitous receivers for IoT applications. RF interference will increase since the limited bandwidth is shared with a rapidly growing number of IoT devices using multiple heterogeneous wireless communication standards. Integrated solutions for interference rejection pose a real challenge in ULP receiver design since they typically require high power and will increase the receiver total power significantly, especially with narrowband channels [1, 2]. The design challenge in receivers for IoT applications is to minimize the power consumption with an adequate sensitivity level in a congested frequency spectrum using highly integrated solutions while still being compatible with an adopted communication standard [3, 4].

Multiple approaches to reduce the receiver's power consumption have been reported recently [5–10]. These primarily tackle the most power hungry blocks, such as the RF local oscillator (LO) and RF low noise amplifiers (LNAs). For example, RF energy detection is used to convert the incoming RF signal to DC without using any RF local oscillators, which leads to significant power reduction but at the expense of sensitivity. In addition, removing active RF gain will lower the power further [11]. Mixer-first architectures avoid using RF gain but still use an RF LO to down-convert the signal to baseband. This efficiently enhances the receiver's sensitivity and

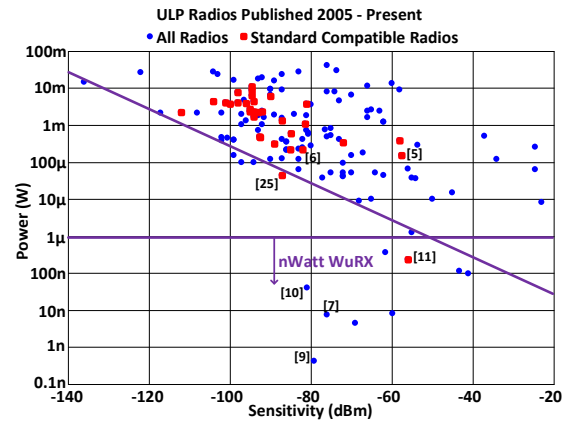


Fig.1. Ultra-low power radio survey: sensitivity vs. power

selectivity compared to RF energy detection since the gain and filtering is done at baseband [5, 6, 12–16].

This paper includes a survey of the recent literature in ULP receiver design. The low power design trends and techniques published recently are discussed in Section II. To address the power and performance tradeoffs in standard compatible receivers, two design approaches are presented in sections III and IV. The first is a BLE compatible back-channel receiver in which the message is embedded in a standard compliant packet and can be received by an ULP receiver. The second is a Wi-Fi wake-up receiver compliant with the wake-up mode defined by the IEEE 802.11ba standard. Finally, conclusions are drawn in Section V.

## II. ULTRA-LOW POWER RECEIVERS DESIGN TRENDS

A survey of ULP receivers published in top tier circuits journals and conferences is done to identify the research directions in their design and its limitations [17]. Fig.1 shows the power vs sensitivity (range) trade-off for the recent 179 published ULP receivers. With the exception of nanowatt wake-up receivers, an empirical line with a slope of  $-1$  decade/20dB bounds the performance. This implies the power will increase by a factor of 10x for a 10x increase in the receiver range (assuming a path-loss coefficient of 2). When the sensitivity is normalized to the data rate (Fig.2), however, the power vs sensitivity trade-off becomes more settled since nanowatt receiver have relatively low data rates. In both figures, standard compliant receivers clearly

tend to be higher power. This is expected since most standards nowadays have stringent requirements on sensitivity, interference rejection and frequency accuracy. To achieve these specifications, high power receiver blocks might become required such as LNAs, active filters with sharp frequency response, and phase locked loops (PLLs) with accurate crystal frequency references.

The signal to interference rejection (SIR) performance of ULP receivers is shown in Fig.3. The trade-off can be clearly observed where only a few standard complaint ULP receivers report their selectivity performance, and they consume  $>100\mu\text{W}$ . This can be attributed to RF down-conversion and active filtering for interference rejection, requiring high power to synthesize a high Q filter response, which is done traditionally by cascading multiple active filter stages. On the other hand, off chip passive filtering is possible but will mean lower system integration and increased cost. For example in [18, 19], off-chip RF MEMS are used to enhance the selectivity performance of the receiver. Network level solutions, such as hopping the frequency to avoid collisions, can boost the effective blocker rejection performance as will be discussed in section III.

The modulation scheme plays an important role in the specifications of the receiver and hence its power consumption [2]. As seen in Fig.4, coherent communication (e.g. BPSK, OFDM, QAM) requires significantly higher power to demodulate. This is because the carrier phase is needed for coherent detection which necessitates using a PLL in the receiver.

The following design trends are observed in recent publications:

#### A. Nanowatt wake-up receivers:

By utilizing an all passive RF front-end, the RX power can be reduced significantly to the nanowatt level. This is achieved using an RF envelope detector to convert the incoming signal to DC (Fig.5). However, an RF envelope detector has a large bandwidth which limits the sensitivity of such architecture to worse than  $-60\text{ dBm}$  [11] due to the high noise bandwidth. The sensitivity can be further improved by  $\sim 20\text{dB}$  by using a high Q transformer at the front-end which provides passive gain and filtering [7, 10] (Fig.5). With this architecture, the integrated interference mitigation techniques used are mostly limited to continuous wave interferes (CW) which can be characterized as an additional DC offset for the comparator [18]. This assumption is not valid for all wireless channels since they experience some level of signal fading which makes these techniques less effective in a real environment. Another limitation of this architecture is it does not support high frequencies due to the large shunt capacitance in RF detectors [20]. Fig.6 shows that all receivers consuming less than  $10\mu\text{W}$  operate at a frequency lower than  $3\text{ GHz}$ . Subthreshold analog and digital logic are common to

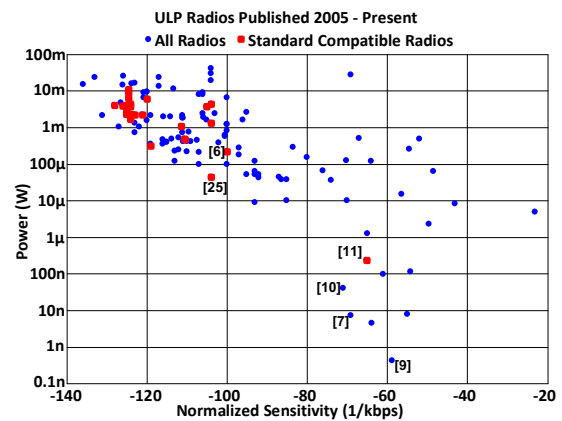


Fig.2 Ultra-low power radio survey: normalized sensitivity vs. power.

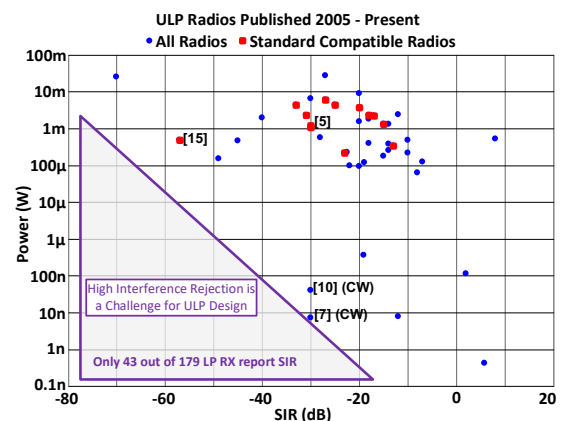


Fig.3 Ultra-low power radio survey: SIR vs. power.

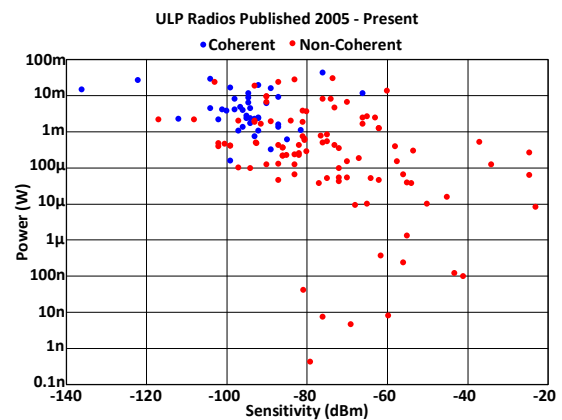


Fig.4 Ultra-low power radio survey: sensitivity vs. power for coherent and non-coherent modulation.

achieve sub  $1\mu\text{W}$  power levels [11]. For very low data rates, bit-level duty cycling have been reported [18]. This allows for improved sensitivity levels with low average power at the expense of very low data rate.

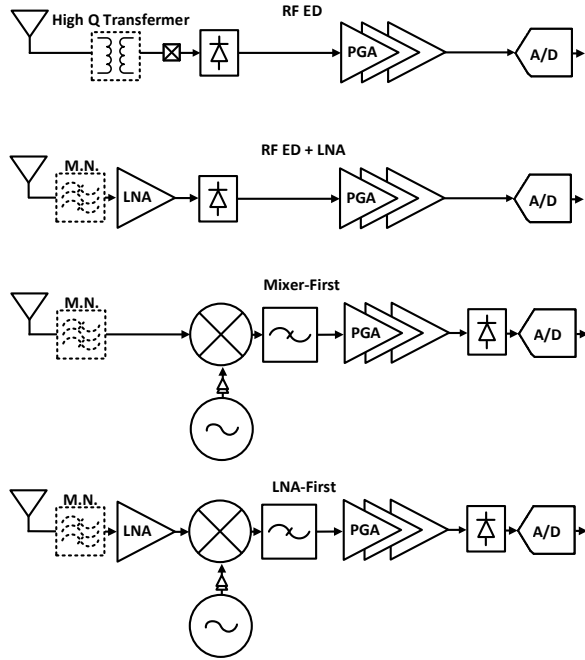


Fig.5 Low power radio architectures.

#### B. Mixer-first receivers for selectivity:

Another design trend to save power is to avoid using active RF gain (LNA) while using a mixer as a first stage instead [21–25] (Fig.5). Since the first RX stage dominates its noise performance, mixer-first receivers suffer from higher noise figure (NF), when optimized for low power consumption, which degrades their sensitivity (range). Nevertheless, this architecture can still achieve decent selectivity levels with a sub-mW power budget [26]. In so-called mixer-first receivers, the dominant block in terms of power consumption is the local oscillator and its buffers. In order to reduce the LO power, the conventional LC oscillator can be replaced with a ring oscillator (RO) especially in more advanced CMOS nodes [27]. However, ROs have worse frequency stability making it harder to design the receiver without a significant performance degradation in its sensitivity and/or selectivity [5]. Alternatively, an LC oscillator can have its inductor off-chip to overcome the limited quality factor for on-chip inductors resulting in a significant power reduction by up to 75% compared with fully on-chip LC oscillators [13]. Although these off-chip inductors can be found in very small form factors, it is not a fully integrated solution, which might not suit some IoT applications.

#### C. LNA-first receivers for long range:

Long range applications require sensitivity levels beyond -100dBm. To achieve this, a LNA-first topology is usually used. Similar to RF ED based wake-up receivers; bit-level duty cycling was applied also in LNA-first receivers [28] to reduce the average power. In addition,

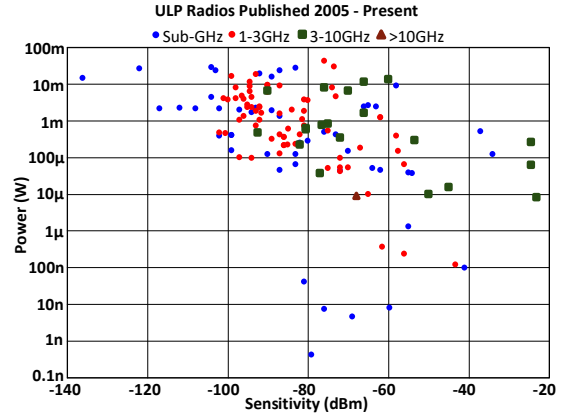


Fig.6 Low power radio survey: sensitivity vs. power for coherent and non-coherent modulation.

lower supply voltages have been used to improve the power efficiency of LNAs [29]. In [30], a low voltage quadrature LNA was adopted in a current-reuse topology resulting in a power consumption of 600 $\mu$ W for the RF front-end, transimpedance amplifier and baseband filter. In addition, [31] presents a direct-conversion BLE receiver using a subthreshold current-reuse LNA.

#### D. Standard compatibility for widespread adoption:

Given the clear power and performance trade-off discussed in this section, one of the challenges in ULP design is to still be able to communicate through an existing adopted standard. The next two sections will present two designs using two approaches to overcome the power and performance trade-off. The first relies on embedding a back-channel message in standard compliant BLE packets [5, 32]. The RX can detect the sequence of BLE advertising channels are used and the timing gaps between them to encode data. The second approach utilizes the wakeup messaging in the IEEE 802.11ba standard to relax the receiver specifications while still being able to receive messages from standard complaint Wi-Fi transmitters [6].

### III. BLE BACK-CHANNEL RECEIVER WITH ENHANCED INTERFERENCE REJECTION

The BLE standard provides a low power solution to connect IoT nodes with mobile devices, however, the power of maintaining a connection with a reasonable latency remains the limiting factor in defining the lifetime of event-driven BLE devices. BLE receiver power consumption is in the milliwatt range [3, 33, 34] and can be duty-cycled for average powers around 30 $\mu$ W, but at the expense of long latency. A recent work presents the concept of BLE back-channel (BC) communication as a wakeup mechanism that bridges the gap between ULP and standard compliant BLE receivers [11]. This provides a low-power receive mode without compromising on latency but it is also susceptible to interference in the crowded 2.4 GHz

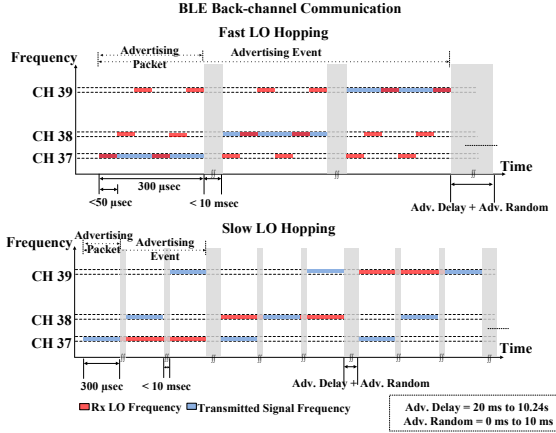


Fig. 7 The concept of back-channel communication in fast and slow modes.

band as it senses the signal without discriminating between sources using different BLE channels.

This section presents two prototypes of BLE back-channel receivers that include channel select filters to improve ACI rejection [5]. Both receivers are BLE compatible and can be used with off the shelf BLE transmitters. The first chip is a 150  $\mu$ W ring oscillator (RO) based receiver with a dual-mixer front-end to save power by using an LO at half the RF frequency. The second chip is a 1.2 mW LC oscillator based receiver with a RF LNA resulting in enhanced frequency stability of the oscillator and improved sensitivity. As a result, the second prototype can support faster frequency hopping. In both designs, channel selectivity is improved by 1) using direct-conversion with narrow baseband filtering (1 MHz) and by 2) defining each BC message based on the presence of packets in three channels instead of only one, which reduces the impact of blockers. Both BC receiver (BC RX) implementations use FSK communication by detecting the hopping sequence on the three BLE advertising channels, which can be specified in any sequence according to the BLE standard. Consequently, these receivers can wake up from a BLE compatible message sent by a mobile device. Depending on the LO frequency hopping speed, the back-channel communication uses either a fast or slow mode as shown in Fig. 7. In the fast mode, and since the receiver is detecting the energy of advertising channels successively, the LO hopping period between all three channels should be less than  $T_{packet}/2$  to ensure capturing each packet's energy for a certain channel. On the other hand, in the slow mode, the hopping period should be at least  $T_{event}/2$  to ensure capturing a complete advertising event comprising transmissions in all three channels. To achieve the fast hopping, and because the receiver has a narrow bandwidth to help its selectivity performance, the LO frequency has to be stable enough to detect the energy in a short time

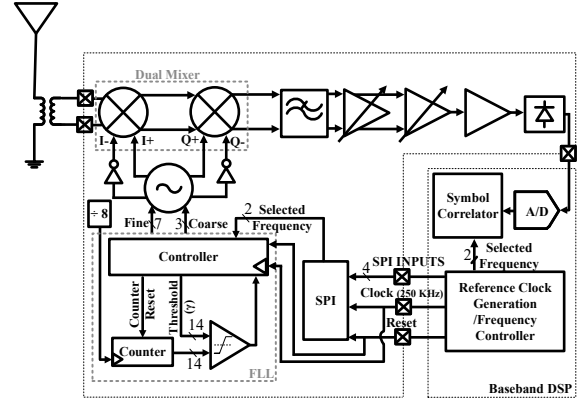


Fig. 8 Block diagram of the RO based BLE back-channel receiver (prototype I).

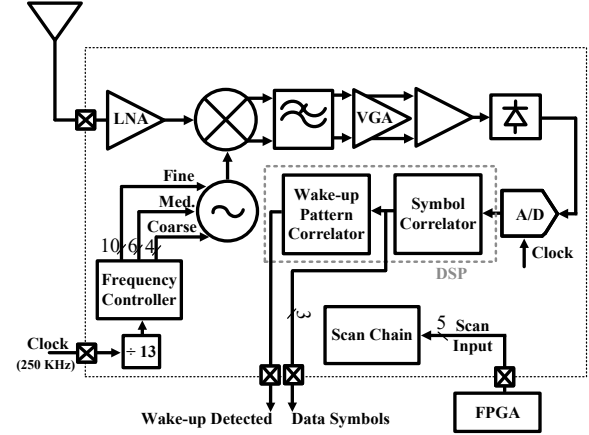


Fig. 9 Block diagram of the LC oscillator based BLE back-channel receiver (prototype II).

window. In our prototypes, an LC oscillator, which has around 20 dB improvement in phase noise at 1 MHz offset compared with the RO, was used to implement the fast hopping exploiting its superior frequency stability even when running open loop.

In this work, we proposed exploiting frequency diversity gain from the multi-channel advertising events discussed in Section II to improve the blocker rejection performance. Assuming fast LO hopping, and when any single advertising channel is jammed by a nearby strong interferer, the transmitted message can be estimated from the remaining two advertising channels. This is done by setting the required threshold for a valid BC message to be two-thirds of the maximum which allows estimating the received BC message from just two out of three channels. The proposed interference rejection solution is possible since the frequency gaps between the three channels are 24 MHz and 54 MHz, which are relatively large compared with the receiver's bandwidth of only 1 MHz. As a typical strong blocker such as Wi-Fi only affects a single advertising channel, BC modulated messages achieve

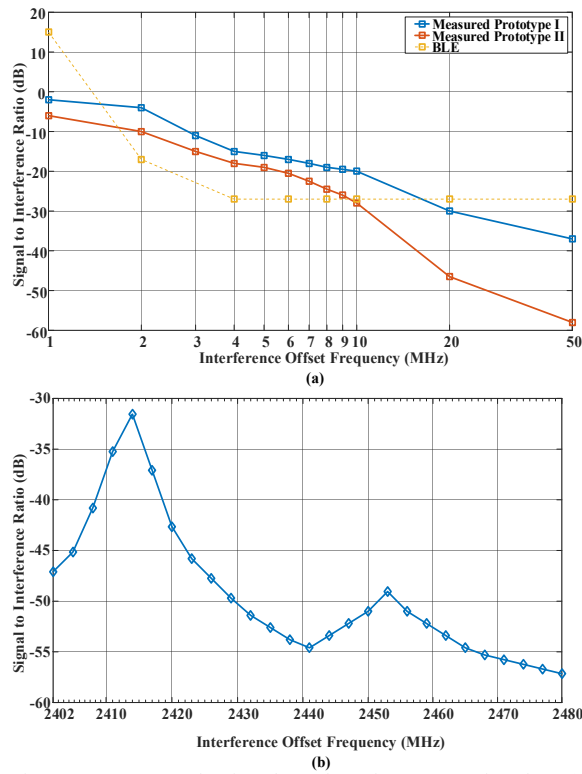


Fig. 10 Measured signal-to interference ratio for (a) prototypes I and II vs. interference offset frequency. (b) prototype II vs. BLE channels assuming BC message communication with frequency hopping.

improved BLE/non-BLE blocker rejection performance using only relaxed low-power baseband filters.

Fig. 8 shows the top level block diagram of the ring based BLE back-channel receiver. A mixer-first architecture is used with a ring oscillator to reduce the total power consumption. A dual mixer is used to set the LO at half of the input RF frequency, leading to significant power savings in the LO and its buffers. The top level block diagram of the LC based BLE back-channel receiver is shown in Fig. 7. This architecture enables the fast frequency hopping by utilizing an RF LNA and an LC oscillator to reduce the noise and improve the frequency stability, respectively. The receiver selectivity is enhanced by limiting the baseband amplifiers bandwidth to 1 MHz.

The RO back-channel receiver was fabricated in a 65 nm LP CMOS process. The receiver has a sensitivity of -57.5 dBm for a BER of  $10^{-3}$ . Fig. 10 (a) demonstrates the signal-to-interference (SIR) performance, which is measured with a wanted signal 3 dB over the sensitivity level and with a GFSK modulated. The interference rejection was measured to be -4, -20, and -30 dB for the 1<sup>st</sup>, 5<sup>th</sup>, and 10<sup>th</sup> BLE adjacent channels, respectively. The total power consumption is 150  $\mu$ W using 0.9 V and 1.1 V supplies for digital and analog blocks, respectively, with 120  $\mu$ W

dissipated by the LO (including its buffers) that runs at 1.2 GHz, the digital FLL, and the LO frequency dividers. The analog baseband consumes the remaining 30  $\mu$ W.

The second prototype, which uses an LC oscillator, was fabricated in a 40nm CMOS process. It achieves a sensitivity of -82.2 dBm for a BER of  $10^{-3}$ . The SIR performance for a single advertisement channel is shown in Fig. 10 (a). The measured rejection ratios are -6, -28, and -46 dB for the 1<sup>st</sup>, 5<sup>th</sup>, and 10<sup>th</sup> BLE adjacent channels, which does not satisfy BLE's single channel block rejection performance (yellow line). On the other hand, Fig. 10 (b) shows the much improved (-32dB or lower) SIR performance when back-channel message level communication is used with the message threshold set at two thirds of its maximum value. This measurement was done by sweeping the interferer frequency across the BLE frequency band while the desired signal is hopping its frequency between the three advertising channels. The worst case rejection ratio is -32 dB at 2414 MHz, which is the middle channel between CH37 and CH38. This result is expected since CH37 and CH38 are closer to each other than CH9. Including the worst case, the rejection ratio at all BLE channels is better than the blocker rejection requirements as set in the BLE specifications. The second prototype consumes 1.2 mW using 0.9 V and 1V supplies for digital and analog blocks, respectively. The dominating blocks are the LC oscillator and the LNA, which dissipate 500  $\mu$ W and 380  $\mu$ W, respectively. The remaining 320  $\mu$ W is consumed by the analog and digital baseband. In both prototypes, the LO generation uses the highest percentage of power.

#### IV. WI-FI WAKE-UP RECEIVER

As mentioned previously, one of the challenges in ULP design is to still be able to communicate through an existing adopted standard, and communication through Wi-Fi can

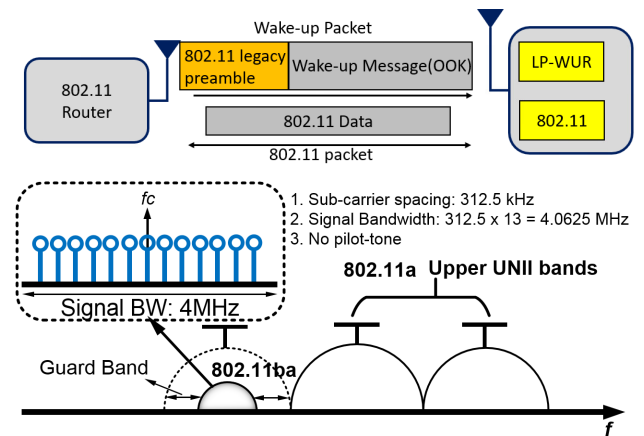


Fig. 11. Conceptual diagram of 802.11ba application (top), and Frequency floor planning of 802.11ba (bottom) [33].



be a good solution. Wi-Fi is one of the most ubiquitous wireless network protocol, however, its direct adoption into ULP IoT nodes is not a good solution due to its excessive active power consumption ( $>100\text{mW}$ ). Even with heavy duty cycling of the 802.11 receiver, the average power is still too high for most ULP IoT applications, and the start-up energy is often too great to make networking and latencies practical at ULP levels.

Recently, the 802.11ba task group established a new standard to reduce the average power of 802.11 receivers by integrating a low-power companion receiver with the main 802.11 receiver, which receives on-off keying (OOK) modulated signals (4 MHz, 13 subcarriers populated a long 20 MHz channel) from an 802.11 transmitter [35]. The power budget of an active Wi-Fi network can be significantly reduced by leveraging a wake-up receiver when the main Wi-Fi receiver remains asleep [35]. The

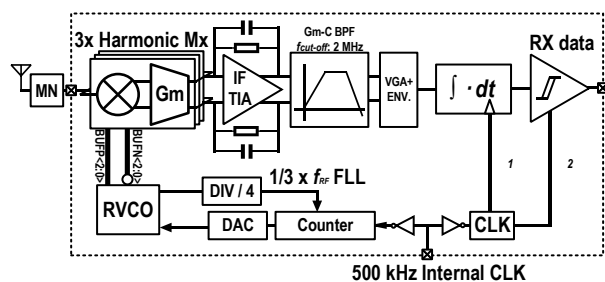


Fig. 12. System block diagram of the RO based 802.11ba low-power wake-up receiver.

frequency planning of the 802.11ba is shown in Fig. 11. Legacy Wi-Fi OFDM signals are generated by modulating sub-carriers in the frequency domain, converting sub-carrier symbols to the time domain, outputting them through a digital-to-analog converter (DAC), and finally up-converting the signal to RF. This OFDM architecture theoretically allows for a wide set of modulations such as OOK or M-ary FSK, although it is not specifically designed for this type of signal generation. By only updating the firmware of an 802.11 OFDM receiver [35], it is possible to map narrowband OOK or FSK symbols onto OFDM subcarriers, and disable the remaining unused sub-carriers.

For active wireless connectivity, the wake-up receiver has to achieve sensitivity of lowest data-rate of 802.11a transmitter, which is  $-82\text{ dBm}$  at data-rate of  $6\text{ Mb/s}$  [12]. the minimum noise figure has been relaxed due to the relaxation of the SNR. This allows us to eliminate the power-hungry active RF gain stage in the wake-up receiver. Two mixer-first low power Wi-Fi wake-up receivers are recently reported that are based on RO [6], and LC oscillator [26].

The RO based Wi-Fi wake-up receiver operates with  $220\mu\text{W}$  while providing sensitivity of  $-83\text{ dBm}$ , and  $-20\text{ dB}$  SIR of 1st adjacent channel. The system block diagram of

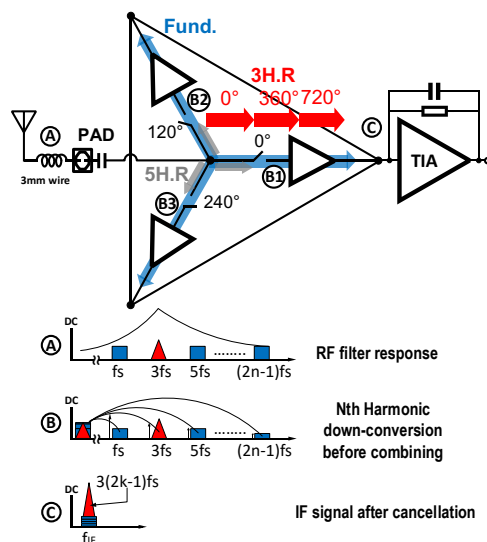


Fig. 13. RF front-end of the receiver using 3<sup>rd</sup>-harmonics down-conversion.

the RO based 802.11ba low-power wake-up receiver is shown in Fig. 12. The receiver is a passive mixer-first architecture with an off-chip matching network. Rather than using an LO-less RF energy detection architecture, which is common among ULP receivers because it results in the lowest active power, this receiver uses a ring-based voltage controlled oscillator (RVCO) to allow channel selection, improve selectivity, and operate at a lower active power than more power hungry LC-VCOs. The receiver receives 4 MHz wide OOK modulated RF signals in the 5.5-5.8 GHz band, compliant with the 802.11ba draft standard. These are down-converted with mixers that operate around  $1/3$  of the RF frequency, thus significantly reducing the active power of the RVCO and buffers. Odd harmonic down-conversion was chosen rather than even harmonic down-conversion because it has a better flicker noise corner vs. power trade-off of the RVCO [36].

To reduce power, no active RF gain stages are used. However, to maintain an adequate sensitivity, step-up transformer based matching network is implemented that provides voltage boost as well. After the three mixer stages, the down-converted IF signals are combined in the current domain before amplification and filtering in TIA. After the TIA, the IF signal is filtered with a  $-40\text{ dB/dec}$  roll off. Finally, the filtered IF signal is rectified, and integrated by baseband circuits, and the RX data is retrieved. The following sub-sections will explain the details of each system block.

The spectrum diagram in Fig. 13 illustrates the behavior of each block that comprise the RF front-end. The RF signal is filtered, and impedance boosted as shown in Fig. 13(a). A commuting passive mixer has a non-linear response, so that at Fig. 13(b), when feeding an LO operating at  $f_{LO}$  to the mixer, it produces harmonic components at  $(2n -$

$1) \times f_{LO}$  ( $n$  is an integer). The actual passive mixer is differential pair that rejects even-order harmonics after down-conversion. Then, in Fig. 13(c), the down-converted signals after each mixer are summed in the current domain using IF low noise amplifiers (IF-LNA) transconductors. The construction and destruction of each harmonic components happen at Fig. 13(c). By combining signals from  $N$ -paths with mixers operating at a  $360^\circ/N$  phase difference each, the  $N$ th harmonic signals at the outputs of the  $N$  mixers will be in-phase at baseband, while the other harmonic components are out-of-phase and cancel.

Simulation results of the power and NF for each harmonic passive mixer down-conversion is shown in Fig. 14. Increasing  $N$  beyond a value of 3 offers diminishing returns in NF vs. active power due to increased insertion loss of harmonic down-conversion gain. Comparing to edge combining duty-cycled frequency multiplication mixer, this save decent amount of power because it uses small number of RF switches, and does not require any high-speed complex logic circuits. Considering noise analysis, and mismatch calibration, this architecture shows an optimal trade-off between performance and power with  $N = 3$ , so that a 3<sup>rd</sup> harmonic 3-path passive mixer is implemented.

Ideally, the front-end can perfectly reject the fundamental RF component while down-converting signals at the 3<sup>rd</sup> harmonic frequency. However, two mismatch factors affect this rejection ratio (3<sup>rd</sup> harmonic / fundamental). Mismatch in the delay cells of the RVCO generate phase mismatch which reduces the rejection ratio as this mismatch increases. However, the dominant factor is gain mismatch in the first inverter-based IF stage, which impacts the rejection ratio due to its common mode offset between IF-LNAs. According to simulation, a phase error less than 5% results in a rejection ratio up to 40 dB. Similar amount of rejection ratio is observed for 5th, and 7th harmonics as well.

To minimize the gain mismatch, self-biased current steering differential IF amplifiers are used with fine resolution gain tuning. Without calibration, there were

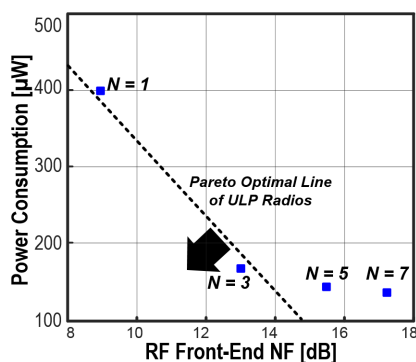


Fig. 14. Simulation results of NF vs. Power trade-off of  $N$ th harmonic Passive mixer RF Front-End. The line represents the Pareto optimal line of state-of-art ULP receivers.

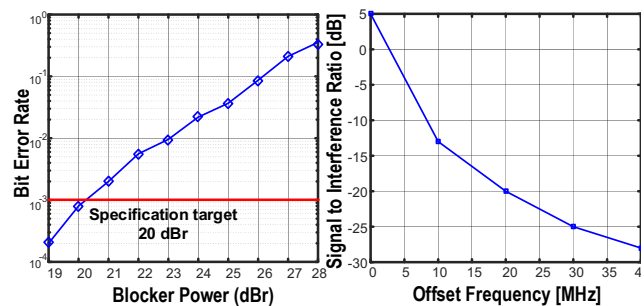


Fig. 15. BER versus blocker power of adjacent channel 1 (left), and signal-to-interference ratio (SIR) versus offset frequency (right).

large variations observed chip to chip, and the worst rejection ratio measured was 25 dB. After calibration, the worst rejection ratio measured was 37 dB, including passive RF matching before the RF front-end.

The receiver was fabricated in a CMOS 40 nm technology with an active area of 0.151 mm<sup>2</sup>. The BER is measured with alternated 802.11ba data. Measured sensitivity of the receiver is -83 dBm at BER of 10<sup>-3</sup>, and data-rate of 62.5 kbps. The sensitivity got 3 dB increment as the data-rate increased twice, which is 125 kbps. Interferer measurements are done with randomized binary data. The SIR of adjacent channel 1, and 2 are -20 dB, and -28 dB, respectively. The interference performance can be limited by the PN of the RVCO, thus, for narrow band receivers, SIR performance is dominated by PN rather than the order of the filter when the order is reasonably high ( $\geq 3$ ).

## V. CONCLUSION

In this paper, a summary of the recent design trends and techniques in low-power receivers design are presented. The power and performance trade-off is discussed and multiple approaches to design receivers that suit the requirements for IoT applications are demonstrated. Two receiver designs, which are compatible with the BLE and Wi-Fi standards, respectively, are presented. These receivers can support a decent communication range while meeting the interference rejection required by the standard with a power consumption in the 100 of  $\mu$ W range.

## ACKNOWLEDGMENT

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