27.1 A 65nm Energy-Harvesting ULP SoC with 256kB Cortex-M0 Enabling an 89.1μW Continuous Machine Health Monitoring Wireless Self-Powered System

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This paper presents a system-on-chip (SoC) that enables commercial self-powered systems (SPSs) by flexibly managing application needs, harvesting energy from multiple modalities, coordinating low-latency/high-density network communication, and optimizing power across the system. To scale to a trillion IoT nodes, devices must untether from batteries by achieving energy autonomy. A SPS must balance harvested power (P_H) with load power (P_L) to enable continuous operation, which becomes challenging in real-world harvesting conditions for applications with stringent functional needs. While this SoC can support many IoT applications, we demonstrate the SoC in a machine health monitoring (MHM) product that uses multi-modal sensors to forecast motor failure to minimize downtime.

Figure 27.1.1 shows a system block diagram for the SoC in the MHM product, which has a 49×48×81mm^3 enclosure including the antenna, and enables continuous sensing even in poor harvesting environments. Multiple mechanical interfaces enable flexible attachment of the node onto a motor. The SoC has an ARM Cortex-M0 microcontroller (MCU) to execute application code, clocked by a crystal oscillator (XO) at 32.768kHz for low power. An integrated PLL scales the clock for higher speed computation and for streaming sensor data by a direct memory access (DMA) block. A 7.3728MHz XO provides for a turbo mode when harvesting allows. An FFT accelerator and 256kB of sub-threshold (sub-V_T) memory provide power-efficient computation at the edge, which is critical to the MHM application. A wakeup receiver (WRX) with full wakeup protocol gives interference robustness and security for dense networks in industrial environments. The SoC includes SPI, I2C, and UART to interface with external parts. Extensive power and clock gating throughout the SoC minimize P_L. A true random number generator (TRNG) and 128b AES encryption enable secure 802.15.4g wireless communication by an off-chip transceiver (TRX) at 915MHz. An RF switch connects the WRX and TRX to one antenna for improved system integration. A boot manager handles sub-V_T clocking and memory access while booting from internal OTP memory, external NVM, or reprogramming with over-the-air updates. A multi-modal energy-harvesting power management unit (EH-PMU) with supercapacitor management enables reliable batteryless operation from an electromagnetic (EM) coil, photovoltaic (PV) cell, thermoelectric generator (TEG), vibration, or RF energy harvesting.

The MHM product requires near-continuous assessment of the state of a rotating machine to observe potential problems in its operation or environment, but voluminous data, high transmit power, and relatively low harvestable power preclude streaming raw data as a generic solution. To support the MHM product requirements, the SoC combines multi-modal sensor data (accelerometer, magnetometer, temperature/relative humidity (T/RH)), supports sub-V_T edge processing, and enables flexible power-aware control over node response. When P_H is high, the node can stream raw data, but usually edge processing must extract key information from the sensor data so the node can report machine state accurately with less TX power. Fig. 27.1.2 shows the state flow for one example operating mode of the MHM product, in which a synchronizing wakeup event from the network triggers the addressed set of nodes. After wakeup, the system optionally flashes an LED for human-visible feedback, measures T/RH to track environmental conditions, and measures magnetic field strength and vibration to capture motor health. The SoC then leverages the MCU and accelerators to extract a low frequency FFT and compute key health indicators on the node, optimizing for low P_L to sustain the power balance of the SPS. Finally, the node transmits key metrics to the cloud, and the system returns to sleep. The SoC enables flexible control over data, computation, and communication based on available node energy.

The EH-PMU (Fig. 27.1.3) supports SPS operation in real-world conditions for numerous applications. A boost circuit with programmable, multi-mode maximum power-point tracking (MPPT) and cold start can harvest from EM, PV, TEG, or vibration modalities and store the energy on VCAP, with integrated supercapacitor management. Different asset settings give different optimal harvesting modalities, so the MHM product uses a separate module to house the harvesting transducer for in-field reconfigurability. A single-inductor multiple-output (SIMO) regulator transfers energy from VCAP to three V_{DD}s, including an adjustable rail (VDDADJ) for dynamic voltage and frequency scaling (DVFS) across different process, temperature, and operating modes. Fig. 27.1.3 shows example startup waveforms from TEG and PV for VIN through VCAP to VDDADJ. The PMU LDO provides an internal V_{DD} for auxiliary circuits, and a sub-V_T LDO provides a clean low V_{DD} for sensitive analog and clocking circuitry. The energy harvesting (EH) condition monitor provides state-of-charge information to the SoC for system-level decision-making, which is critical to leveraging the SoC's low-power hooks for reliable self-powered operation.

The SoC supports a wireless network protocol that can synchronize a dense network of 1000 sense nodes in real-world environments within range of one gateway (Fig. 27.1.4). The physical layer uses on-off keyed WRX beacons for network synchronization and a programmable number of time slots of 802.15.4g frequency-shift keyed data packets for uplink to the cloud, which the SoC secures using AES. Compared with duty-cycled high-power TRXs with clock drift, an always-on WRX provides lower power time synchronization for dense low-latency networks, especially with shorter intervals between WRX beacons. However, a correspondingly higher uplink packet rate increases the uplink collision rate, requiring retransmission and raising average power in the sense node. A wideband WRX beacon also provides initial frequency synchronization between gateway and sense nodes, allowing the gateway to frequency hop.

The WRX (Fig. 27.1.4) comprises an off-chip matching network to provide passive gain into a rectifier-first analog front-end with baseband gain before conversion by a differential, 10b SAR ADC. The protocol supports both fast wakeups with shorter time-on-air and secure wakeups with in-band burst and continuous wave interference robustness, data payload, and protection against energy or replay attacks. If the digital baseband correlates the received sync word above a threshold, it issues a fast wakeup to the MCU. For secure wakeups, the baseband demodulates a header in the physical layer and passes the secure payload through a cryptographic checksum before issuing a wakeup. The WRX also provides clear-channel assessment (CCA) and RSSI for network link quality tracking.

To enable flexible control of the node's P_L, the SoC supports DVFS into sub-V_T, wide range clock control, extensive clock/power gating, accelerators for edge compute, and low voltage I/Os. The power balance in an SPS makes power optimization often more important than minimum energy, emphasizing slow low-voltage operation. The SoC includes an ADC and SRAM (Fig. 27.1.5) that operate robustly and at low power across the DVFS range. Fig. 27.1.5 shows how the SRAM combines product features like BIST and redundancy with circuit/architecture techniques (e.g. 8T cell, decoupled R/W, peripheral assist features) to enable reliable operation down to sub-V_T.

The SoC is fabricated in 65nm CMOS (Fig. 27.1.7) and provides a comprehensive solution for networked self-powered nodes. Fig. 27.1.6 compares the SoC to other ultra-low power (ULP) and self-powered SoCs. While some SoCs are integrated into systems, the proposed SoC enables continuously active batteryless self-powered products. For an MHM product, the SoC enables 89.1μW average system power (from VCAP) for continuous asset monitoring in an industrially hardened, securely networked batteryless node.

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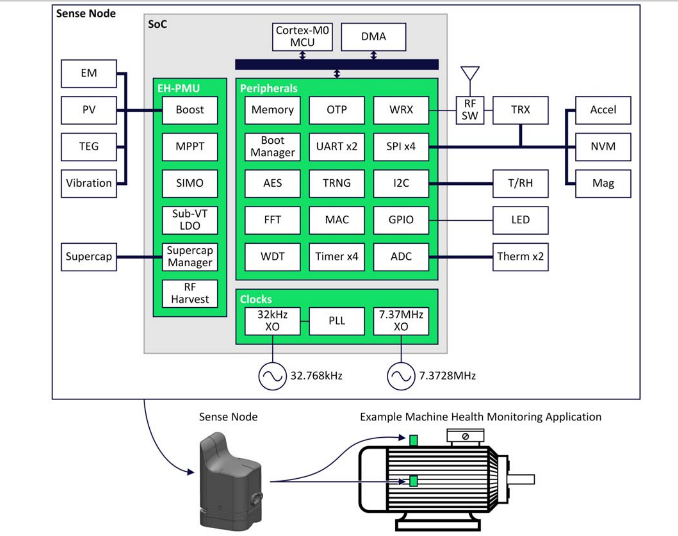


Figure 27.1.1: System block diagram showing the SoC in a commercial self-powered sense node for continuous machine health monitoring (MHM).

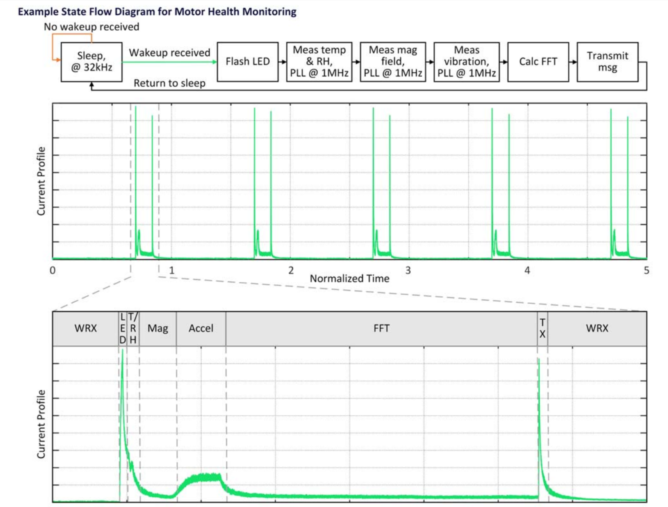


Figure 27.1.2: State flow diagram and measured self-powered system current profile for an application example of machine health monitoring, which uses multiple sensors to detect, analyze, and report machine status.

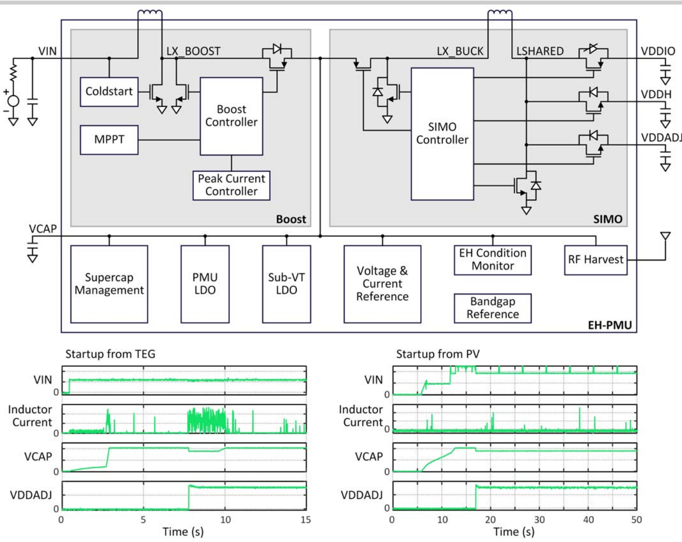


Figure 27.1.3: Energy-harvesting power management unit (EH-PMU) with measured cold-start waveforms from TEG and PV harvesting modalities.

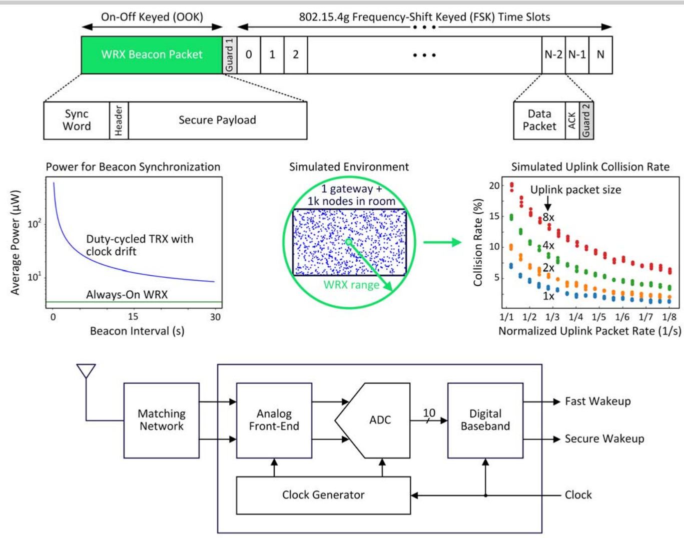
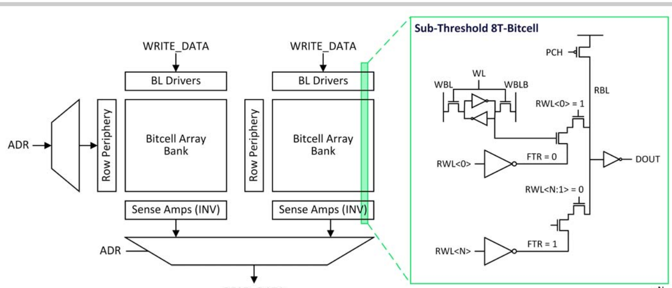


Figure 27.1.4: Simulated performance of the network protocol with the proposed physical layer and supporting WRX architecture.



SRAM Feature	Enabling Design
Fast characterization	Memory BIST testing from banks simultaneously
High yield	Redundancy and remapping
Low voltage operation	Decoupled read/write with write assist

SoC Power Saving Feature	Enabling Design
Performance across PVT	Sub-VT circuits and DVFS
Low idle power	Low frequency clock and extensive clock gating
Low power operation	Power gating of unused clocks and peripherals
Low power vibration measurement	Reducing load on MCU with direct memory access
Low power FFT calculation	FFT accelerator
Low power wireless network synchronization	Always-on wakeup receiver

Figure 27.1.5: SRAM banks and 8T bitcell for DVFS into sub-V_T with tables enumerating SRAM and SoC power saving features.

		This work	[1] ISSCC '18	[2] VLSI '17	[3] ISSCC '19	[4] JSSC '19	[5] TMTT '16
Sense Node	Average Power	89.1µW* full MHM system	200µW* idle, 25000µW* peak	507nW+	144µW+	82.9µW+	1.8mW+
	Networked Operation	Y	Y	N	N	N	N
	Sensing Modalities	Acceleration, T/RH, Mag Field	Image	ECG	-	EEG	Localization
SoC	Technology	65nm CMOS	14nm Tri-Gate CMOS	130nm CMOS	28nm FDSOI	65nm CMOS	65nm CMOS
	Industry/Academia	Industry	Industry	Academia	Academia	Academia	Academia
Digital	MCU	Cortex-M0	x86	Custom	Cortex-M0 DS	No MCU	No MCU
	Operating Frequency	32kHz-7MHz	200kHz-950MHz	32kHz	40-80MHz	20MHz	100-400MHz
	DVFS Implementation	Y	Y	N	N	N	N
	Sub-VT Memories	Y	N	Y	Y	N	N
	Accelerators	FFT, MAC, AES, TRNG	Neural Network, Crypto Engine	2xDSP ,RR-AFIB, Compression	FFT	-	-
	Interfaces	ADC, GPIO, I2C, SPI, UART	AFE, GPIO, I2C, SPI, UART	ADC, GPIO, SPI, JTAG	GPIO, SPI, JTAG	AFE	Serial
EH-PMU	Energy Harvesting Modalities	EM, RF, PV, TEG, Vibration	PV	PV, TEG	-	-	-
	Regulator Efficiency	83%	-	71.1%	-	-	-
	Batteryless	Y	N	Y	N	-	Y
	Coldstart & MPPT	Y	N	Y	N	-	N
	Supercap Support	Y	N	N	N	-	N
Radio	Sensitivity (dBm)	-54	-72	No RF	No RF	No RF	-30.7
	FEC	Y	N	-	-	-	N
	Payload	Y	N	-	-	-	N
	Crypto Checksum	Y	N	-	-	-	N

* Full system power. Measured from VCAP/VBAT

\+ Component power. Measured from supply rail

Figure 27.1.6: Performance and comparison table with other ULP and SPSs.

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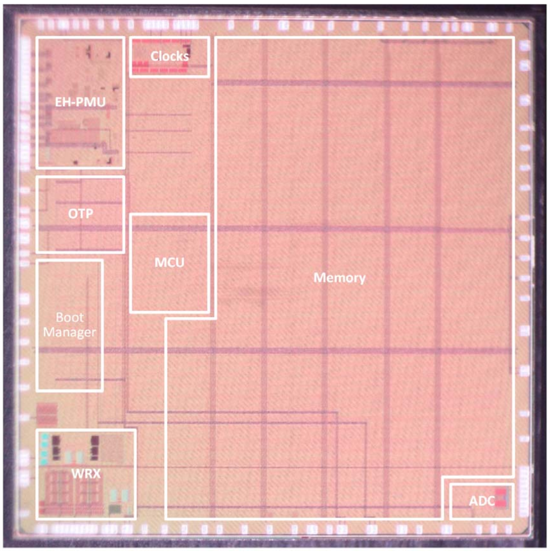

Figure 27.1.7: Die photo of the 65nm self-powered SoC.

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