Analysis and Design of an Ultra-Low-Power Bluetooth Low-Energy Transmitter With Ring Oscillator-Based ADPLL and 4× Frequency Edge Combiner

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***Abstract*— In this paper, we present an all-digital ring oscillator (RO)-based Bluetooth low-energy (BLE) transmitter (TX) for ultra-low-power radios in short range Internet-of-Things (IoT) applications. The power consumption of state-of-the-art BLE TXs has been limited by the relatively power-hungry local oscillator (LO) due to the use of LC oscillators for superior phase noise (PN) performance. This paper addresses this issue by analyzing the PN limit of a BLE TX and proposes an RO-based solution for power and cost savings. The proposed transmitter features: 1) a wideband all-digital phase-locked loop (ADPLL) featuring an $f_{RF}/4$ RO, with an embedded 5-bit TDC; 2) a 4× frequency edge combiner to generate the 2.4-GHz signal; and 3) a switch-capacitor digital PA optimized for high efficiency at low transmit power levels. These not only help reduce the power consumption and improve PN performance but also enhance the TX efficiency for short range applications. The TX is prototyped in 40-nm CMOS, occupies an active area of 0.0166 mm^2, and consumes 486 μW in its low-power mode, while configured as a non-connectable advertiser. The TX has been validated by wirelessly communicating beacon messages to a mobile phone.**

***Index Terms*— All-digital phase-locked loop (ADPLL) Bluetooth low-energy (BLE), Internet of Things (IoT), phase noise (PN), ring oscillator (RO), switch-capacitor digital power amplifier (SCDPA), transmitter, ultra-low-power (ULP).**

I. Introduction

BECAUSE of its versatility and practicality, Bluetooth low energy (BLE) is becoming more popular as the wireless communication protocol for Internet-of-Things (IoT) applications [1]–11]. The recently finalized Bluetooth 5.0 standard enables a faster data rate, more versatile advertising channel interactions, and an extended communication range [12], which makes BLE radios more adaptive in IoT designs. However, state-of-the-art BLE designs still consume an average of 4–5 mW active power [1]–[6], while commercial BLE SoCs consume more than 10 mW, limiting battery life and placing a ceiling on their adoption into IoT devices. In applications that require extended battery life or self-powered operation via energy harvesting such as wireless body sensor networks (WBSNs), implantable medical devices, and disposable consumer electronics, BLE radios consume too much power to be adopted at a large scale. In such systems, ultra-low-power (ULP) radios with proprietary asymmetric communication protocols are used [13]–[17] to save power in the edge nodes while pushing all the computation and power into the base station. But these designs either suffer from a significantly lower data rate, more severe interference and multiple access issues, or an extra bulky aggregator. Thus, it is very beneficial to explore a way to further reduce the BLE radio's power consumption, especially the BLE transmitter (TX), and enable a standard compatible asymmetrical communication with a sub-milliwave BLE TX in the edge nodes and fully compliant BLE transceivers in a cellphone or tablet as the base station. It will not only save a significant amount of power and extend the lifetime of IoT SoCs but could also help resolve the interference and base station issues in ULP wireless systems.

The bottleneck of further power reduction in BLE TX design mainly results from two building blocks: the local oscillator (LO) and the power amplifier (PA), which typically take more than 80% of the TX power consumption combined. Significant effort has been spent on the phase-locked loop (PLL) design for BLE [18]–[21]. Some state-of-the-art all-digital phase-locked loop (ADPLL) designs have successfully broke through the 1-mW barrier [19], [20]. But due to the use of *LC* voltage-controlled oscillators (LCVCO) which are implemented with on chip inductor whose quality factors are <20, power cannot be reduced further, no matter the performance, because oscillation cannot be sustained. A recent trend shows that more and more BLE designs prefer to use open-loop LCVCO designs with direct modulation [4], [10], since its phase noise (PN) performance is more than enough for BLE. In normal cases, the LO PN requirement

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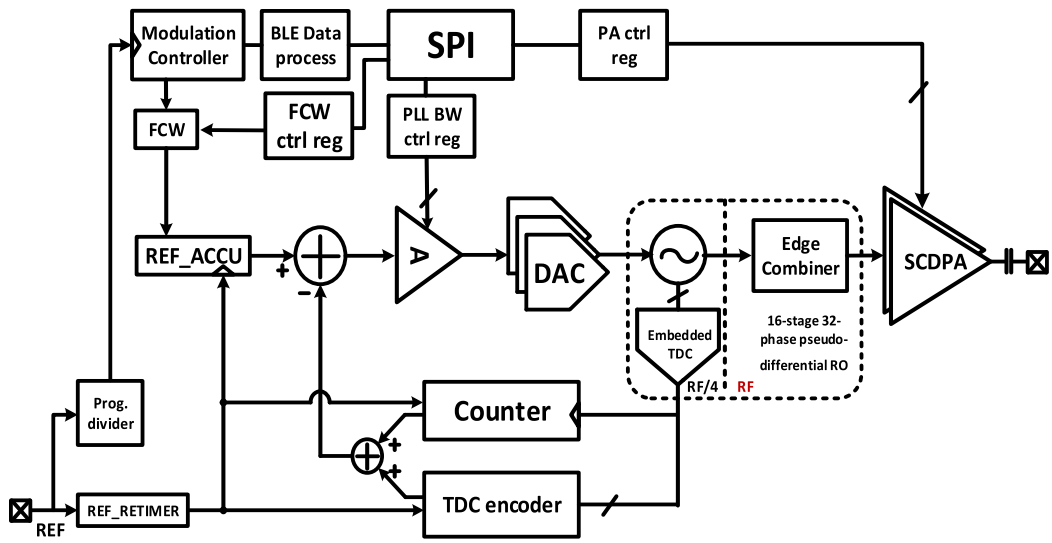


Fig. 1. Block diagram of the proposed RO-based all-digital BLE transmitter.

for a BLE TRX is determined by the receiver (RX) side due to the requirements in RX sensitivity, blockers, and reciprocal mixing, and it is always better to have a better PN. But for a BLE TX-only prioritized design, the PN limit for the LO has not been studied. This is especially true if this TX is in an asymmetric network where the RX LO in the "base station" is often overprovisioned with high PN tolerance.

This paper will address this issue by giving a detailed analysis between PN and system level specifications for a transmitter, using a similar method as in [22] and [23]. The relaxed PN limit for BLE TX will not only help bring down the TX power consumption to its physical limit but also increases flexibility in BLE circuit design based on the application emphasis. Based on the analysis, we propose the first-ever reported ring oscillator (RO)-based BLE TX [24], as shown in Fig. 1, with an ULP wideband type I ADPLL using a 32-phase $f_{\mathrm{RF}}/4$ RO, which not only forms a 5-bit embedded TDC but also serves as a 4× frequency edge combiner. It reduces the PLL power and improves its PN at the same time. To further reduce PA power consumption, we utilize a switch-capacitor digital PA (SCDPA) [31] with a matching network optimized for low-power operation achieving a high efficiency. The BLE TX consumes 486 μW, while configured as a non-connectable advertiser, which is desirable for short-range TX-only beacon devices in an asymmetric BLE network. Its functionality has been validated by wirelessly communicating beacon messages to a mobile phone.

This paper is an extension of [24], and is organized as follows. Section II introduces the analysis and derivation of the PN limit for BLE TXs. Section III discusses the system level design considerations. Section IV talks about detailed circuit design and tradeoffs to achieve low power and the required noise performance. Section V discusses the measurement results and the comparison to the state of the art. Finally, Section VI draws the conclusion.

II. Phase Noise Analysis For BLE TX

The relationship among PN, period jitter, and instantaneous frequency variation has been well analyzed in [22] and [23]. Frequency error of an LO can be roughly calculated based on the integrated PN [25]. Since BLE is frequency modulated, it is beneficial to derive an intuitive relationship to link circuit level specs such as PN, and system level specs such as frequency deviation, and modulation index. Reference [22] analyzed it for FSK radios based on bit error rate (BER), but in BLE designs, the PN requirement needs to be more specific.

In a high SNR regime where the target communication range is within 1–2 m, PN is the dominant noise source. Flicker noise will contribute more in the slow-frequency drift, so its effect in random jitter and instantaneous frequency variation (IFV) is negligible in this analysis. The mean-squared value of period jitter and IFV is given by

$$\sigma_f^2 = f_0^4 \sigma_\tau^2 \tag{1}$$

where σ_f and σ_τ represent the standard deviation of IFV and jitter and f_0 is the center frequency. Using the Wiener–Khinchine theorem [32], we can calculate the mean-squared jitter from the spectral density

$$\sigma_\tau^2 = \int_0^\infty S_\tau(f)df = \frac{1}{f_0^4}\int_0^\infty S_\phi(f) f^2 \mathrm{sinc}^2\left(\frac{\pi f}{f_0}\right) df \tag{2}$$

where $S_\tau(f)$ and $S_\phi(f)$ are the power spectral densities (PSDs) of jitter and random phase, respectively. It can be further simplified as

$$\sigma_\tau^2 = \frac{2}{\pi f_0^3}\int_0^\infty \mathcal{L}(f) f^2 df \int_0^\infty \mathrm{sinc}^2(x)dx \tag{3}$$

where $\mathcal{L}(f)$ is the PN PSD. With only white noise taken into consideration, $\mathcal{L}(f)f^2$ is a constant. Thus, across the whole single-side band (SSB), the relation among period jitter, IFV,

and PN can be simplified as

$$\sigma_\tau^2 = \frac{1}{f_0^3}\mathcal{L}(f)f^2 \tag{4}$$

$$\sigma_f^2 = f_0\mathcal{L}(f)f^2. \tag{5}$$

This is the classical link between jitter and PN, with a relation to IFV when noise in the whole SSB is considered. However, when it comes to the PN impact in radio circuit designs, we need to consider the noise filtering effect in the receiver. Assuming a brick wall filter in the RX with a bandwidth $\mathrm{BW_{rx}}$

$$\sigma_\tau^2 = \frac{2}{\pi f_0^3}\mathcal{L}(f)f^2\int_0^{\frac{\mathrm{BW}_{rx}\pi}{f_0}} \mathrm{sinc}^2(x)dx. \tag{6}$$

Since the RX bandwidth is much smaller than the carrier frequency, the integral of the squared sinc function can be approximated as

$$\int_0^{\frac{\mathrm{BW}_{rx}\pi}{f_0}} \mathrm{sinc}^2(x)dx \approx \mathrm{Si}\left(\frac{2\mathrm{BW}_{rx}\pi}{f_0}\right) \approx \frac{2\mathrm{BW}_{rx}\pi}{f_0}. \tag{7}$$

Thus, with the RX filter, the relation among jitter, PN, and IFV can be modified as

$$\sigma_\tau^2 = \frac{4\mathrm{BW}_{rx}}{f_0^4}\mathcal{L}(f)f^2 \tag{8}$$

$$\sigma_f^2 = 4\mathrm{BW}_{rx}\mathcal{L}(f)f^2. \tag{9}$$

This offers a simple intuition for circuit designers that once the RX filter BW is known, the PN spec at certain offset, say 1 MHz, can be calculated directly from the system level requirements for the frequency modulated signal.

Next, we consider the case where a PLL affects the PN noise shaping. When the PLL has a bandwidth $\mathrm{BW_{pll}}$, and with all the PLL noise sources taken into account, the in-band PN can be approximated as a constant L_{in}. So (2) becomes

$$\sigma_\tau^2 = \frac{2\mathcal{L}_{\mathrm{in}}}{f_0^4}\int_0^{\mathrm{BW_{pll}}} \frac{f_0^2}{\pi^2}\sin^2\left(\frac{\pi f}{f_0}\right)df + \frac{2\mathcal{L}_{\mathrm{in}}f_{\mathrm{BW_{pll}}}^2}{f_0^4}\int_{\mathrm{BW_{pll}}}^{\mathrm{BW}_{rx}} \mathrm{sinc}^2\left(\frac{\pi f}{f_0}\right)df. \tag{10}$$

Simplified as

$$\sigma_\tau^2 = \left\{\begin{array}{l} \frac{1}{2\pi^3 f_0}\left(\frac{2\pi\mathrm{BW_{pll}}}{f_0} - \sin\left(\frac{2\pi\mathrm{BW_{pll}}}{f_0}\right)\right) \\ +\frac{4}{f_0^4}\left(\mathrm{BW}_{rx} - \mathrm{BW_{pll}}\right)\mathrm{BW_{pll}^2} \end{array}\right\} L_{\mathrm{in}} \tag{11}$$

$$\sigma_f^2 = \left\{\begin{array}{l} \frac{f_0^3}{2\pi^3}\left(\frac{2\pi\mathrm{BW_{pll}}}{f_0} - \sin\left(\frac{2\pi\mathrm{BW_{pll}}}{f_0}\right)\right) \\ +4\left(\mathrm{BW}_{rx} - \mathrm{BW_{pll}}\right)\mathrm{BW_{pll}^2} \end{array}\right\} L_{\mathrm{in}}. \tag{12}$$

Note that (11) and (12) show that the larger the PLL bandwidth, the larger the jitter and IFV. That is because in these equations, the in-band PN is set as a constant, and larger BW means a higher oscillator PN. On the other hand, larger BW means lower L_{in} if the oscillator PN is preset. In PLL designs, the in-band PN is a more valuable spec than the oscillator spot PN at certain offset, since it also defines specs for other circuit blocks, which are also major PLL noise sources such as the reference, divider, TDC, and DAC. For the $\mathrm{BW}_{rx} < \mathrm{BW_{pll}}$ case, the PN, jitter and IFV relations are shown as follows:

$$\sigma_\tau^2 = \frac{1}{2\pi^3 f_0}\left(\frac{2\pi\mathrm{BW_{rx}}}{f_0} - \sin\left(\frac{2\pi\mathrm{BW}_{rx}}{f_0}\right)\right)L_{\mathrm{in}} \tag{13}$$

$$\sigma_f^2 = \frac{f_0^3}{2\pi^3}\left(\frac{2\pi\mathrm{BW}_{rx}}{f_0} - \sin\left(\frac{2\pi\mathrm{BW}_{rx}}{f_0}\right)\right)L_{\mathrm{in}}. \tag{14}$$

This case is very useful for RO-based designs where RO PN is the dominant noise source for PLL design and it needs to be regulated with a wide PLL bandwidth.

The above derivations show the relationship among PN, jitter, and IFV with only white noise taken into consideration. Introducing a flicker noise corner in the model will make the theoretical approximation much more complicated with very limited model accuracy improvement. As in PLL regulated cases, the in-band PN floor is contributed by different noise sources such as the TDC, DAC, and reference, thus, a flat noise floor is a straightforward and quite accurate representation. In practical open loop *LC* oscillator-based designs, the slow-frequency drift due to flicker noise (<10 kHz within 1 ms) will be recalibrated before each data packet.

Comparing this to the simple integral format, even though seemingly more complicated, it offers a more intuitive link between spot/in-band PN to a system level spec in frequency modulated radios. This is because the $6\sigma_f$ of the

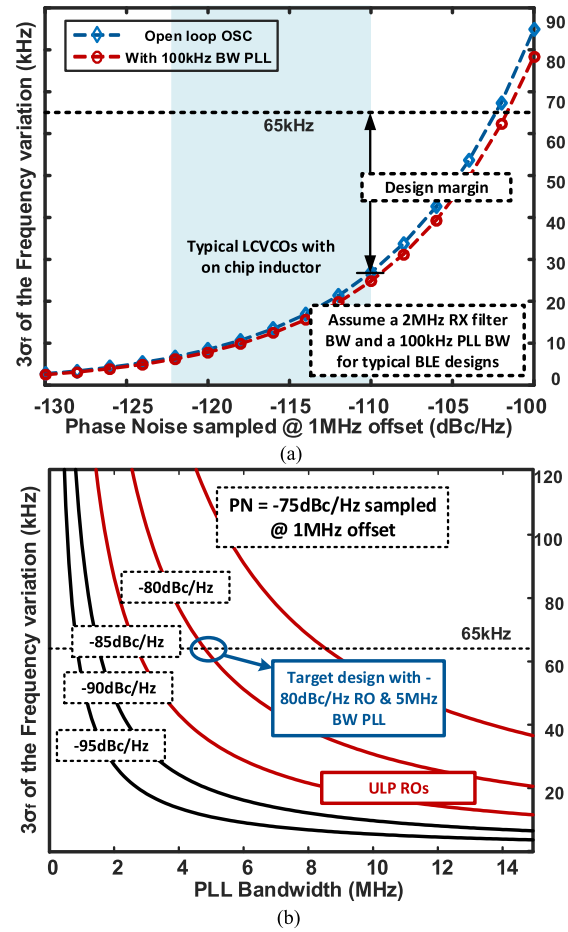


Fig. 2. (a) Simulated IFV versus LO PN between open loop oscillator and oscillator with100-kHz BW PLL. (b) Simulated IFV versus PLL bandwidth for RO designs with varying PN.

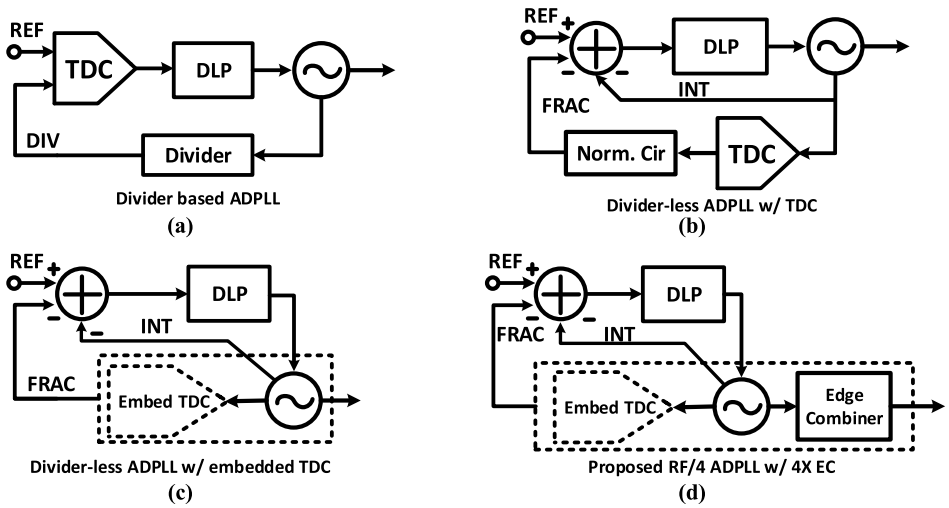


Fig. 3. Simplified block diagram of different ADPLL architectures. (a) Divider-based ADPLL with TDC as the PD. (b) Divider-less ADPLL with TDC. (c) Divider-less ADPLL with embedded TDC. (d) Proposed ADPLL with quarter-frequency OSC and 4× edge combiner.

IFV is approximately the peak-to-peak frequency error, and spot/in-band PN is a direct indicator of oscillator/PLL design. For example, as shown in Fig. 2(a), BLE requires a >370 kHz minimum frequency difference for a ±250 k frequency deviation. Therefore, a $3\sigma_f < 65$ kHz can be used to define the PN spec (40 kHz for GFSK but in the noise limited region, Gaussian shaping would not effectively improve the spectrum efficiency). Comparing the open loop oscillator and PLL regulated case of (9) and (11) when the PLL BW and RX BW are set to 100 kHz and 2 MHz, Fig. 2(a) shows that the resulting IFV is comparable and leaves a big margin to the 65-kHz BLE requirement using LCVCO, which indicates an over-design in the LO noise-power penalty. Fig. 2(b) further shows that with a wide band PLL to suppress the in-band PN, an ULP RO could also achieve the target. So in order to achieve the targeted LO performance, while balancing the power consumption between the oscillator and the PLL controller, and achieving the lowest overall power consumption of the LO, we propose to utilize a −80 dBc/Hz RO at 1 MHz offset with a 5 MHz bandwidth PLL to verify the above analysis. The overall LO power is below 400 μW, while the RO itself is kept below 100 μW.

III. System Level Analysis for the Proposed RO-Based BLE Transmitter

A. Proposed ADPLL Architecture

In order to achieve the target PN using a noisy RO rather than the generally used LCVCO, the PLL design for the BLE transmitter is critical. Even though the major noise source is the VCO PN, other building blocks also need to be carefully dealt with, especially for low-power designs. Fig. 3 shows four different architectures of the TDC-based ADPLLs. The divider-based ADPLL [26] shown in Fig. 3(a) needs a relatively high-power divider and suffers from divider noise folding as well as reference noise upconversion. For fractional operation, an extra delta–sigma modulator (DSM) is needed for the divider. Thus, this is a relatively a power hungry choice. The divider-less ADPLL [27] shown in Fig. 3(b) directly uses a TDC to generate the fractional error. This architecture effectively removes the noise contributed from the divider and the DSM but a TDC running at RF frequency consumes a significant amount of power as well, let alone an extra normalization circuit. Advanced designs [18], [19] in this architecture effectively reduce the TDC power consumption while maintain an excellent noise performance by introducing a DTC and snapshot circuit, but the timing misalignment and non-linearity of the DTC and TDC will introduce spurs. The pre-calibration circuit will result in extra power consumption, thus, making it hard for further power reduction. As for the architecture shown in Fig. 3(c) with an embedded TDC [28], the power is saved by removing the explicit TDC and the normalization circuit. However, the TDC resolution is limited by the number of RO stages at high frequency, which will result in a relatively high in-band PN for high-frequency applications.

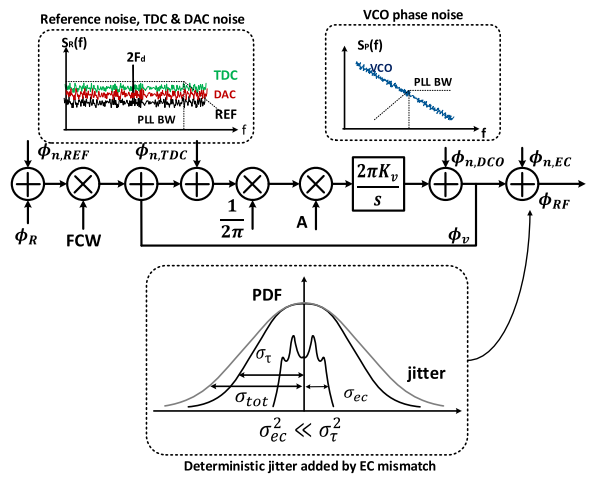


Fig. 4. System level noise analysis with different noise sources including reference noise, TDC noise, DAC noise, VCO noise, and EC noise.

Fig. 3(d) shows the simplified block diagram of the proposed ADPLL to address the above issues. The detailed block diagram is already shown in Fig. 1. To achieve the targeted frequency variation error with the RO, a 5-MHz bandwidth ADPLL for aggressive in-band PN suppression is implemented. It features a fast settling time and direct reference

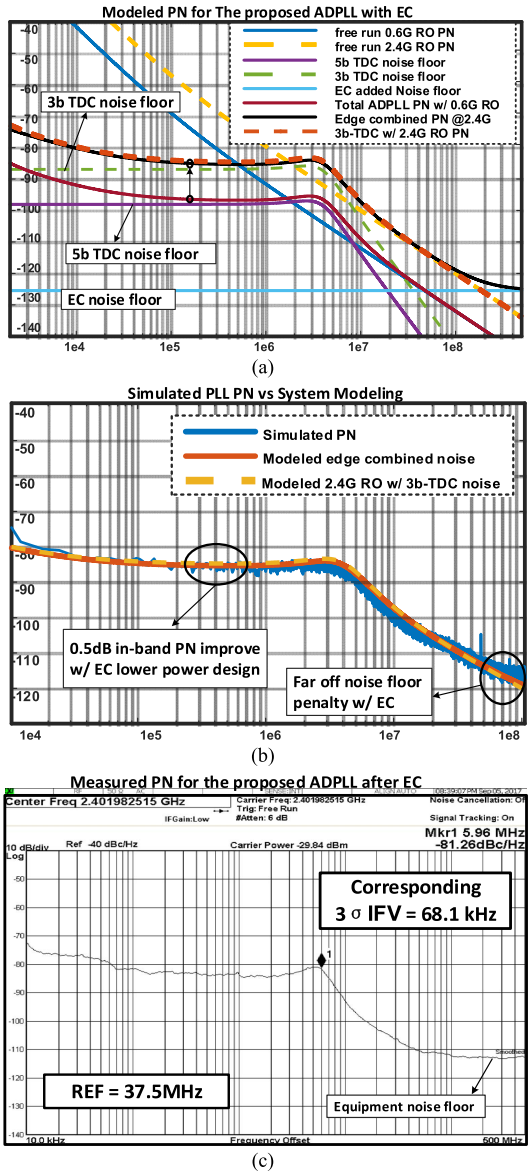


Fig. 5. Noise performance of the proposed ADPLL. (a) Modeled different PN sources. (b) Simulated versus modeled total PN. (c) Measured PN with corresponding IFV.

phase modulation at the frequency control word (FCW) since the PLL BW is much larger than the modulation BW. The BW is programmable by changing the loop filter gain through a SPI interface, as shown in Fig. 1. Several techniques are used to save the PLL power and enhance its in-band PN at the same time. The RO is designed at a frequency of $f_{\mathrm{RF}}/4$ and implemented with a 16-stage pseudo-differential architecture with 32 phases directly used as an embedded TDC. Its phases are also used in a windowed edge combiner (EC) for 4× frequency multiplication to produce the 2.4-GHz RF frequency. The lower frequency RO further saves the power of the counter in the PLL as it not only reduces the operating frequency but also the number of counter stages. It prevents the noise folding effect from happening in the divider-based PLL, thus improving in-band PN performance. At the same time, the high-power explicit TDC and its delay normalization circuits are also saved, and the TDC performance

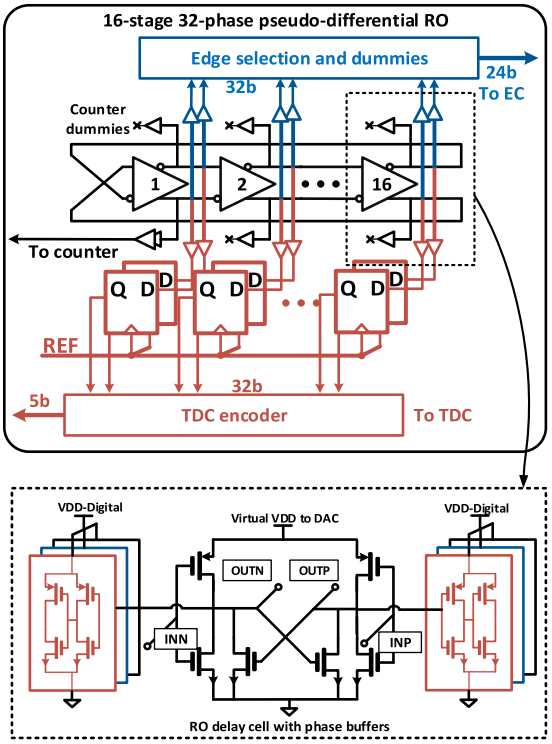


Fig. 6. Proposed 16-stage pseudo-differential RO block and the RO delay cell with buffers.

can be relaxed by dealing with the same amount of jitter at a lower frequency while maintaining the same resolution. The low-frequency embedded TDC with extra edge combiner design consumes around 60 μW less power in total compared to the normal frequency PLL design from simulation, and it can maintain the low flicker noise corner from the low-frequency RO, which will again, enhance the in-band PN [29]. However, extra deterministic jitter will be introduced because of the mismatches in the different paths of the EC, as modeled in Fig. 4. Due to periodical phase shifts, the EC will also introduce spurs at $\pm f_{\mathrm{RF}}/4$ off the center frequency. Its negative effect will be analyzed in more detail in B.

B. Noise Analysis With the Edge Combiner

Major noise sources are modeled for the PLL, as shown in Fig. 4, including reference noise, TDC noise, DAC noise, and RO PN. The PLL is designed to achieve a 5-MHz BW with a −85 dBc/Hz in-band PN after edge combining. In this design, the in-band PN is dominated by both the RO and TDC. The TDC noise floor is around −100 dBc/Hz with the 5-bit resolution at quarter RF frequency, which is comparable to the in-band PN of the quarter frequency RO, as shown in Fig. 5(a). Ideally, the relative noise floor difference between RO and TDC are the same with or without the quadruple effect. However, since the absolute delay offset due to layout mismatch, loading variation and RO jitter are the same, the actual TDC noise floor is slightly enhanced in the quarter frequency RO architecture due to the larger VCO period

$$L_{\mathrm{TDC}} = \frac{(2\pi)^2}{T_v^2}\left(\frac{t_{\mathrm{res}}^2}{12} + \frac{\Delta_M^2}{3} + \frac{2}{\pi}\sigma_\tau^2\right)\frac{1}{f_{\mathrm{REF}}} \tag{15}$$

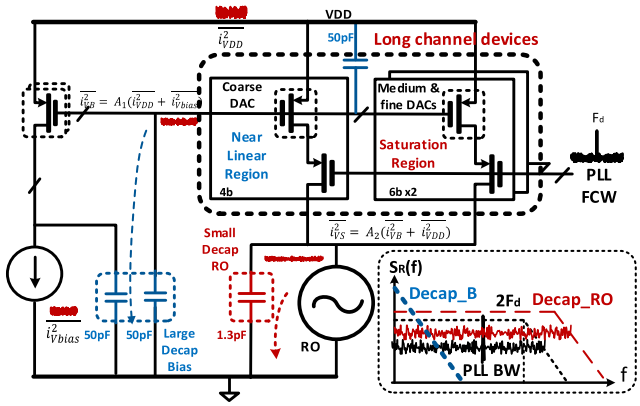


Fig. 7. Current steering DAC for RO tuning and its major noise contributions.

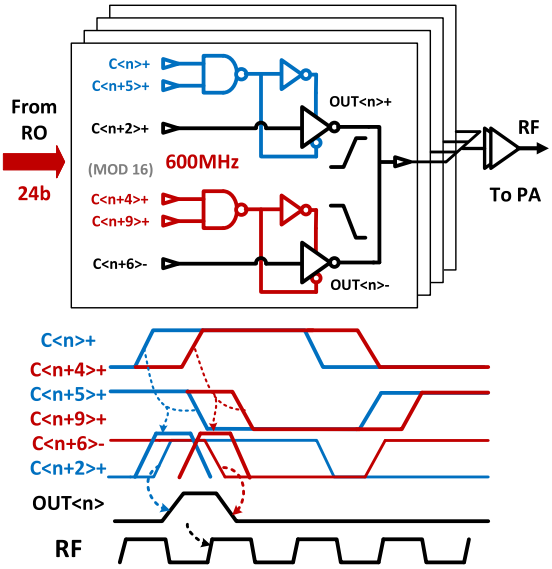


Fig. 8. Schematic of the edge combiner block and its working principle.

where t_{res} and T_v is the TDC delay and the VCO period, and Δ_M correspond to the average mismatch. Here, the mismatch is assumed as uniformly distributed, and for the embedded TDC, the jitter on the TDC edges follows the Gaussian distribution of the RO output. Since the delay, jitter, and average mismatch are not correlated, the actual TDC noise floor with and without quarter frequency multiplication are shown in Fig. 5(a), assuming a 10-ps rms jitter for the RO at 2.4 GHz. After frequency multiplication, the in-band PN at 2.4-GHz output is slightly improved compared to a normal frequency embedded TDC as a reference (edge combined PN versus 2.4G RO w/3b-TDC PN). The DAC resolution is restricted by the modulation, thus, the DAC noise floor is pretty low. Because of the divider-less nature of this design, its noise would not be upconverted as a problem.

The edge combiner, due to loading mismatch, will add a certain delay "D" for each path. Thus, the variance of the timing uncertainty from one path is

$$\sigma_{\tau_{\text{EC}}} = \frac{(D)^2}{12}. \tag{16}$$

In the worst case, there will be three phases with positive delay and one phase with negative delay, or vice versa. Thus,

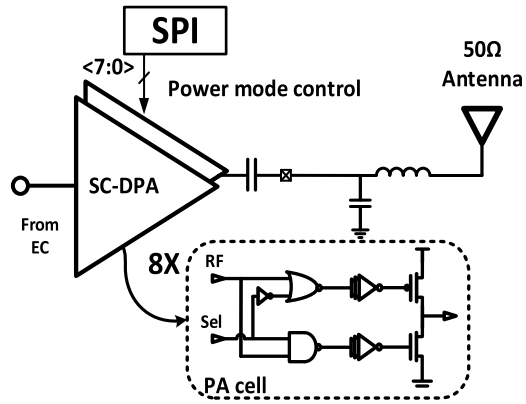


Fig. 9. Programmable SCDPA and schematic of the PA unit cell.

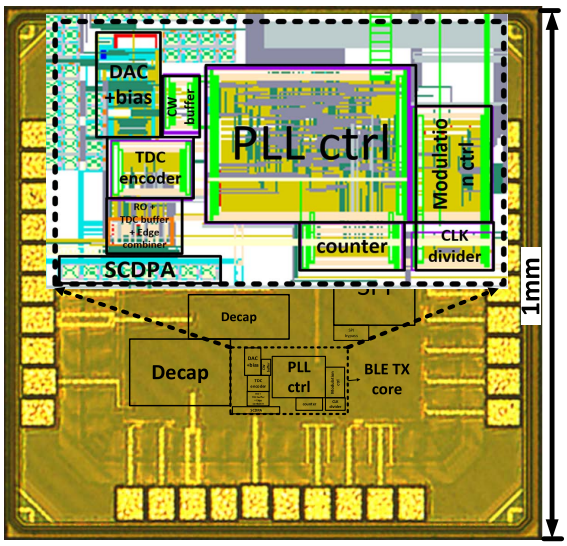


Fig. 10. Die photograph of the proposed BLE transmitter.

the worst case delay is 3-D in (16). The phase uncertainty is

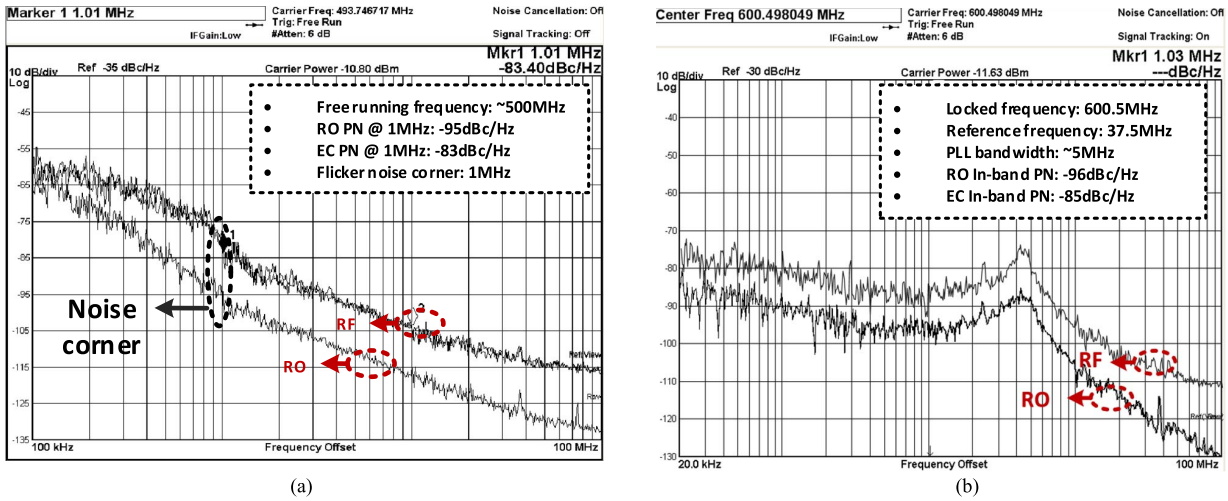
$$\sigma_{\phi_{\text{EC}}} = \frac{2\pi\,\sigma_{\tau_{\text{EC}}}}{T_v}. \tag{17}$$

So the worst case PN introduced by the EC is

$$\mathcal{L}_{\text{EC}} = \frac{(2\pi)^2}{12}\frac{(3-\text{D})^2}{T_v^2}\frac{1}{f_V}. \tag{18}$$

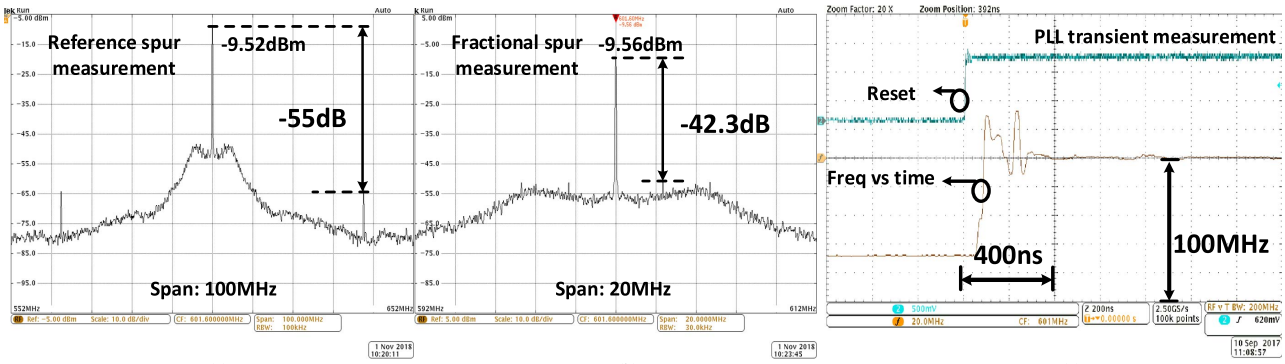
It shows that the EC will add an extra non-filtered noise floor in the overall PN output due to the path delay from layout mismatch. But in practice its level is relatively low compared to other noise sources unless the farout PN is of concern. Monte Carlo simulations for the EC show that the average delay offset is around 1.5 ps, and 1.7 ps calculated from indirect open loop PN measurement, which translates into an EC added noise floor of around −125 dBc/Hz. Thus, the EC noise basically does not contribute to the in-band PN. The far out PN floor discrepencies between simulation and measurement results shown in Fig. 5(b) and (c) are mainly due to the instrumental noise.

From a time-domain perspective, the EC-introduced jitter is much smaller than, and not correlated with, the random jitter from the high-PN RO. The windowed EC would not affect the overall RF performance in the random noise region. In this



(a) (b)

Fig. 11. Measured PN comparison. (a) Free running RO compared to the RF output. (b) Closed-loop RO compared to the RF output.



(a) (b) (c)

Fig. 12. Measured PLL spurious performance and locking transient performance. (a) Reference spur measurement. (b) Fractional spur measurement. (c) PLL locking time measurement.

design, in order to balance the phases offset and improve the EC spur performance, dummies are added to each RO phase output and the layout of the RO has been carefully designed with symmetry. Furthermore, extra loadings were added to each phase output after PEX extraction. Fig. 5(b) shows the simulated PLL noise performance versus the model from the above analysis, and Fig. 5(c) shows the measured PN of the proposed ADPLL. The PN performance corresponds to a 68.1 kHz $3\sigma_f$ IFV, which is close to the target design. The spur level is equal to $20\log(\Delta t/T_v)$ according to [30] and [33], where Δt is the average delay mismatch associated with each combined output phase. The average phase delay offset improves from 2.95 to 1.5 ps in simulation due to the loading calibration in the layout, improving the spur from -43 to -49dBc. With this $f_{\mathrm{RF}}/4$ RO and edge combiner architecture as well as the 5b embedded TDC, the PLL controller's power consumption is 253 μW in a 40 nm technology.

IV. Circuit Implementation

A. Ring Oscillator

The detailed circuit design of the 16-stage pseudo-differential RO is shown in Fig. 6. All the 32 phases are buffered out and directly sampled by 32 D flip-flops at the reference clock as an embedded TDC [28] without extra delay lines. Then the 32b outputs are encoded to form a 5b binary output as a fractional phase error sampler. One phase output is sent to the counter for integer phase error calculation, while the rest phases are connected to dummies for a balanced output to minimize the TDC DNL. On the other hand, all phases are also buffered out to an edge selection circuit, where 24 of them are arranged and fed to the edge combiner while the other eight phases are connected to dummies too. The RO cell is implemented with two inverter stages for each cell and NMOS-only cross couple pairs rather than cross coupled inverters for minimized loading. Each cell has six buffered outputs for TDC, EC, and counter (or dummies). This helps achieve the best balance among speed, PN, and power efficiency for the RO.

B. Current Steering DAC

The current steering DAC for digital RO tuning is shown in Fig. 7. The DAC is one of the most important circuit blocks for the PLL noise performance since supply and bias noise are critical to RO-based designs. Since the PLL BW is very large for in-band PN suppression and direct reference phase modulation, the decap on the virtual VDD of the RO has to be fairly small to keep the PLL loop stable, thus plenty of noise from the supply and the bias network will pass through.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work		JSSC15[1]	ISSCC15[2]	ISSCC15[3]	JSSC16[4]		ISSCC18[10]
Technology (nm)	40		55	40	40	28		28
LO Architecture	RO + ADPLL		LC + analog PLL	LC + ADPLL	LC + analog PLL	LC + ADPLL		LC + analog PLL
Supply voltage (v)	0.6-0.9		0.9-3.3	1	1.1	0.5/1		0.2
PLL REF frequency (MHz)	37.5		16	32	32	5/40		1
PLL settling time (μs)	0.4		15	15	N/A	14		N/A
PLL In-band PN (dBc/Hz)	-85		N/A	-90	N/A	-92/-101		-80
PLL FoM	-208.5		N/A	-220.9	N/A	-231.6		-227.2
Max output power (dBm)	@0.6V	@0.9V	0	-2/1	0	3		0
	-9.4	-3.3						
Max PA efficiency	41%*		30%	25%	<30%	41%		32%
TX Power consumption	0.49mW	1.55mW	10.1mW	4.2mW	7.7mW	4.4mW	3.8mW**	4mW
	@-19dBm	@-3dBm	@0dBm	@-2dBm	@0dBm	@0dBm	@-3dBm	@0dBm
TX max efficiency	32% @-3dBm		15%	10%	13%	36%		25%
Core Area (mm^2)	0.0166		0.6***	0.6***	0.6***	0.65		0.53
FSK error	9.1%		N/A	4.8%	N/A	2.7%		2.2%
HD2 @ 0dBm	-42.5****		-49	-49	-52	-50		-49.6
# of ext. components	2		0	N/A	0	0		0

*With 0.7V PA power supply **Estimated from PA efficiency
***Estimated from die photo for only TX ****Measured with off chip matching network

To deal with this, the coarse DAC bank is designed at the edge of the triode region to minimize the noise gain while the medium and fine DAC banks are designed in the saturation region to keep the required tuning linearity while the PLL is locked. Additional large decaps are added to the gate of the DAC cells to filter the accumulated supply and bias noise. The medium and fine current steering DACs are 6b each that covers 70 MHz range with approximately 20-kHz LSB tuning step for the RO and the coarse DAC is 4b and can cover up to 300 MHz.

C. Edge Combiner

Fig. 8 shows the windowed edge combiner. In the 24 phases of the RO input, six phases are used for each rising and falling edge to be combined, in which the two windows are spaced by four RO delays and the window width is five delays to ensure all selected phases pass through in different PVT corners. Tristate gates are used to pass the selected phase and buffer the interference from other phases. The timing diagram for edge combining is shown in Fig. 8. In this design, the EC consumes just 20 μW from simulation and its added jitter is much smaller than the RO jitter itself, keeping the RF output in the random noise region. In applications where the EC jitter is comparable to the oscillator jitter, then it cannot be treated as working in the random noise region for frequency multiplication. Power has to be traded off for mismatch in the EC circuit design according to system requirement.

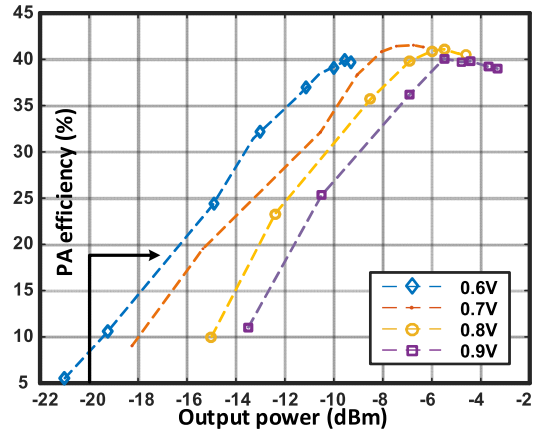
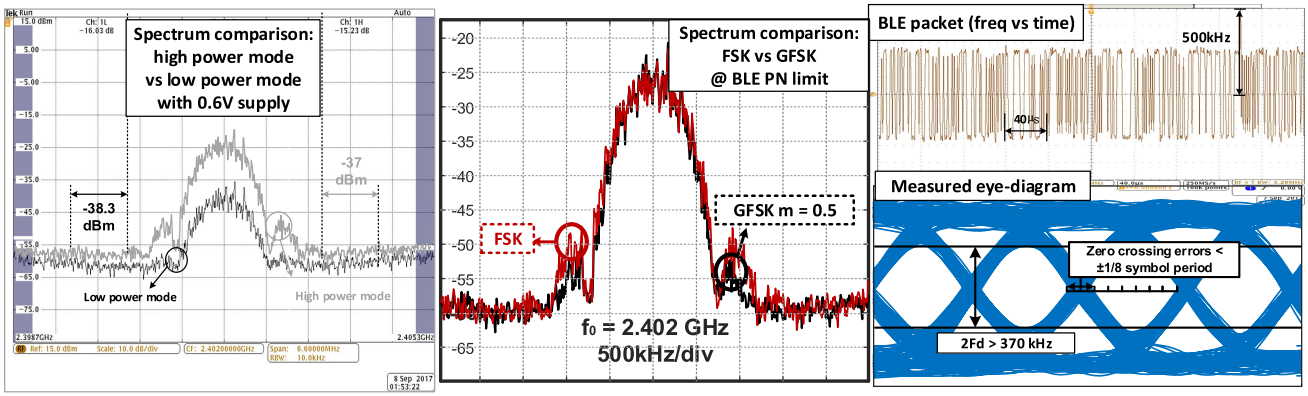


Fig. 13. PA efficiency versus output power with different power supplies.

D. Switched-Capacitor Digital PA

A class-D SCDPA [31] is utilized in this design due to its robustness, low cost and great performance in efficiency. Compared to other switching PAs, even though the class-D does not possess the highest efficiency, it is more robust and less susceptible to driving transistor parasitics, PVT variations and matching, and with the supply sensitive RO implementation in the LO, class D is more reliable due to its relatively low output swing. As there is no on-chip resonant component, it is more suitable for low cost fully integrated solutions and



(a) (b) (c)

Fig. 14. TX performance measurement. (a) Output spectrum in low-power and high-power mode. (b) Spectrum comparison of FSK and GFSK in the PN limit region. (c) Captured BLE packets and eye diagram.

can benefit from advances in technology scaling with better switches. The efficiency of this kind of PA is related to the ratio of the loading impedance and on-resistance of the driving transistor minus the power of the harmonics, thus, it is more versatile in matching schemes to achieve the highest efficiency at a targeted output power based on application emphasis. For example, higher loading impedance results in a low maximum output power but helps with efficiency in low output power levels. Different from the typical SCDPA design [31], where series capacitors are within each PA cell, this design utilizes a shared capacitor bank to prevent extra output power loss due to the grounded capacitors in the off PA cells. As shown in Fig. 9, the SCDPA is thermometer coded with 8-bit cells and is matched and optimized for the highest efficiency for −10 dBm operation, which is sufficient for 2–3 m short range communication.

V. Measurement Result and Analysis

The proposed BLE transmitter is fabricated in 40-nm CMOS and the die photograph of the prototype chip is shown in Fig. 10. The core area of the TX is 0.0166 mm^2. The measurement results are shown as follows. Fig. 11 shows the measurement of the open loop (a) and closed loop (b) PN performance of the proposed ADPLL. When the RO is free running at 494 MHz, the PN at 1 MHz offset is −95 dBc/Hz and the EC output at around 2 GHz is −83 dBc/Hz, with the noise corner both at around 1 MHz. The PN of the ADPLL is shown in (b). It is locked at 600.5 MHz with a 37.5 MHz reference. The PLL bandwidth is around 5 MHz and the measured in-band PN of the oscillator and the EC output at 2.402 GHz are −96 and −85dBc/Hz, respectively.

The PLL outputs are directly measured at 600MHz shown in Fig. 12. The reference spur is −55 dBc and the fractional spur is −42.3 dBc, as shown in Fig. 12(a) and (b), respectively. As can be seen from the frequency vs time diagram in Fig. 12(c), due to the large bandwidth, the PLL locks within 400 ns after reset from a 70 MHz initial frequency offset.

Fig. 13 shows the SCDPA measurement showing the PA efficiency versus output power at different supply voltages. Using a 0.6-V power supply, the PA consumes 107 μW with a −19.2 dBm output power, yielding a 10.8% PA efficiency

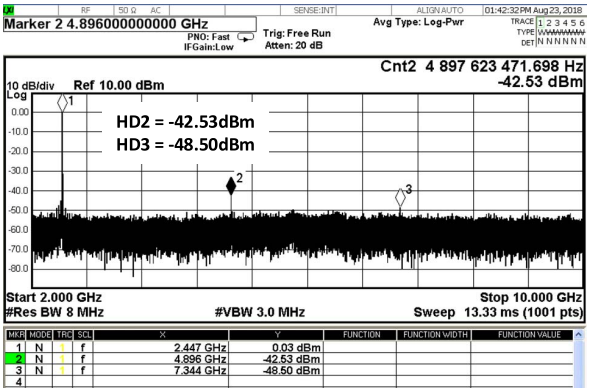


Fig. 15. TX-harmonic measurement with external matching network.

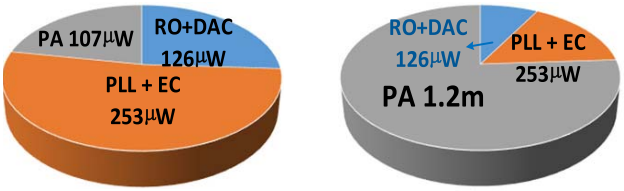


Fig. 16. TX power breakdown in low-power and high-power mode.

at the lower boundary of the BLE output power requirement. In its high-power mode with a 0.9-V supply, it can deliver −3.3 dBm, while consuming 1.2 mW with a 39% efficiency. The maximum efficiency of 41% is achieved at around −7.1 dBm (at 0.7 V) output power with a 476-μW PA power consumption. Due to the non-linear nature of the SCDPA, an external matching network is used to suppress TX harmonic emissions.

The TX spectrum is measured, while transmitting a repeated BLE packet. The spectrum output is compared using a 0.6-V supply between high-power mode with all 8 PA cells are turned on and low-power mode with only 1 PA cell is enabled. It can be seen in Fig. 14(a) that both cases meet the BLE spectrum mask. A comparison of FSK and GFSK at the PN limit region is shown in Fig. 14(b), showing that when operating at the PN limit region, FSK and GFSK basically have the same spectrum efficiency. This simplification in modulation could potentially help reduce the power consumption even

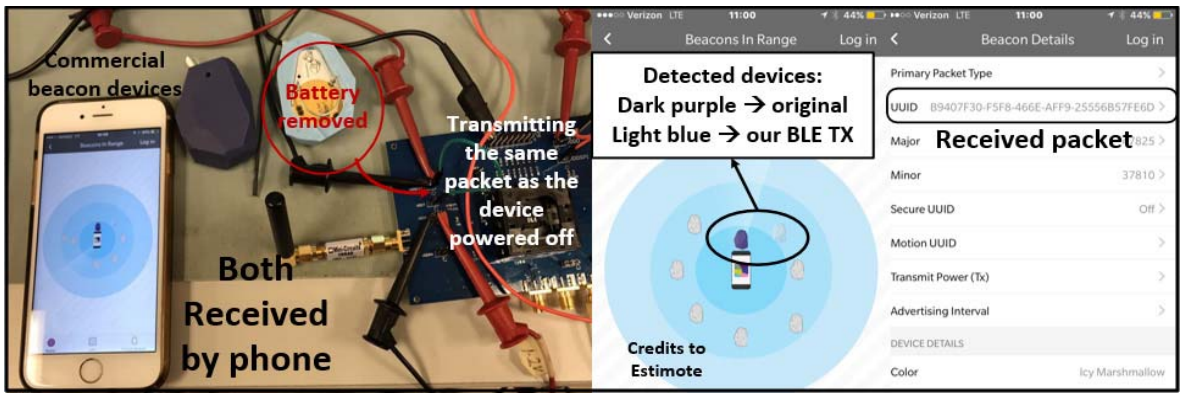


Fig. 17. Phone connectivity measurement setup for the proposed BLE TX.

more for low-power applications such as self-powered sensors with power consumption as the primary concern and the targeted communication range is within 2–3 m. The measured frequency versus time for part of the BLE packets is also shown in Fig. 14(c). The eye diagram is plotted from the captured frequency domain signal. The PN from the RO-based design does degrade the eye performance, but as designed, both the symbol timing and 3σ IFV barely meet the BLE communication limit. The FSK error is 9.1% for this design, which can be expected from the 68-kHz frequency variation. The measured harmonic performance is shown in Fig. 15. With the off chip matching network, both HD2 and HD3 are smaller than -42 dBm with a 1.2-V PA power supply, which complies with BLE requirements.

The power breakdown is shown in Fig. 16. While working at the low-power mode with a 37.5 MHz off chip reference, the RO with the DAC bias network consumes 126 μW, the PA consumes 107 μW and the PLL blocks with the edge combiner consumes 253 μW. In the highest power mode with 0.9-V supply, the PA consumes 1.2 mW. The all-digital RO-based BLE TX consumes a total 486 μW and 1.6 mW in low-power and high-power mode. The comparison to the state of the art is shown in Table I. As the first reported RO-based BLE TX design, it cherishes certain benefits compared to the LCVCO-based designs. With the RO, the TX is able to work at the BLE PN limit without extra power-noise penalty. The LO block is able to achieve a power consumption of less than 400 μW combined. This helps to enhance the TX efficiency regardless of the PA design. The core area is also considerably small with the RO implementation and can benefit even more with technology scaling, reducing the cost for massive IoT production. Yet for practicality, it is still better to leave some extra margin for the RO design according to the theory analysis in session II, since from the PLL measurement result, it can be seen that the PLL is at the edge of being unstable and the IFV is also a bit higher than the 65 kHz target.

Fig. 17 shows the wireless test setup. Here, the BLE TX is configured to transmit an iBeacon message, which is picked up by the iBeacon app, and shows the correct packet information.

VI. Conclusion

In this paper, a theory analysis for BLE PN requirement has been studied. Instantaneous frequency variation of the local oscillator due to PN under different circumstances is used as the link between system level specifications in BLE transmitter to circuit level design choices for the LO. A PN limit is derived as the design baseline too. To verify the analysis, an all-digital RO-based BLE TX is designed and measured. The key techniques to reduce the power consumption while maintaining the performance are: 1) a wideband ADPLL featuring an quarter RF frequency RO, with an embedded 5-bit TDC; 2) a 4X frequency edge combiner to generate the 2.4 GHz signal; and 3) an SCDPA optimized for high efficiency at low transmit power levels. The measurement results show excellent agreement between theory analysis and circuit design, and proving RO is feasible for BLE TX design with low power.

The transmitter consumes 486 μW in low-power mode, while talking to a phone and is extremely low cost due to the implementation with RO. Moreover, because of the all-digital nature of this design, it can further benefit from technology scaling.

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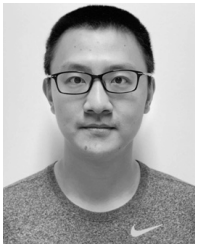

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