A 220-μW −83-dBm 5.8-GHz Third-Harmonic Passive Mixer-First LP-WUR for IEEE 802.11ba

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***Abstract*— A 40-nm CMOS IEEE 802.11ba low-power wake-up receiver (LP-WUR) is presented. It receives 802.11ba messages generated by an 802.11 orthogonal frequency-division multiplexing (OFDM) transmitter operating at 5.8 GHz. The power consumption of the RF front-end is minimized by removing active RF gain stages and using a third harmonic passive mixer with a ring-based local oscillator (LO) operating at one-third of the RF frequency. The noise figure is 14 dB, taking advantage of a 1:3 transformer that provides passive voltage gain in front of the high switch loss mixer-first RF front-end, and matching across 5.5–5.8 GHz with < −12 dB S_{11}. The receiver achieves a sensitivity of −83-dBm and −20-dB adjacent channel signal-to-interference ratio (SIR) while consuming 220 μW at a bit error rate (BER) of 10^{-3} and data rate of 62.5 kb/s, which shows the best sensitivity-power tradeoff among >3-GHz receivers.**

***Index Terms*— 802.11ba low-power wake-up receiver (LP-WUR), step-up transformer, third harmonic three-path passive mixer.**

I. Introduction

Wi-Fi is the most ubiquitous wireless network protocol, however, its adoption into ultralow power (ULP) Internet of Things (IoT) devices has been limited because of the high active power consumption (>100 mW) of Wi-Fi radios. Even with heavy duty cycling of the 802.11 radio, the average power is still too high for most ULP IoT applications, and the startup energy is often too great to make networking and latencies practical at ULP levels.

As shown in Fig. 1, many custom ULP wake-up receivers (WURs) which operate well below 1 mW have been proposed. In particular, ULP receivers that operate <100 μW, with sensitivities better than −80 dBm have been demonstrated [1]–[3]. Moreover, several local oscillator (LO)-less, submicrowatt, < −60 dBm ULP receivers have been reported [4], [5]. While this last category of ULP receivers offers the best sensitivity-power tradeoff, one drawback of these LO-less receivers is they tend to suffer from poor channel selectivity, [1], [4], [5]. The common disadvantage shared by all of these ULP receivers is they are not compliant with any Wi-Fi standard, and therefore cannot take advantage of the ubiquity of Wi-Fi networks.

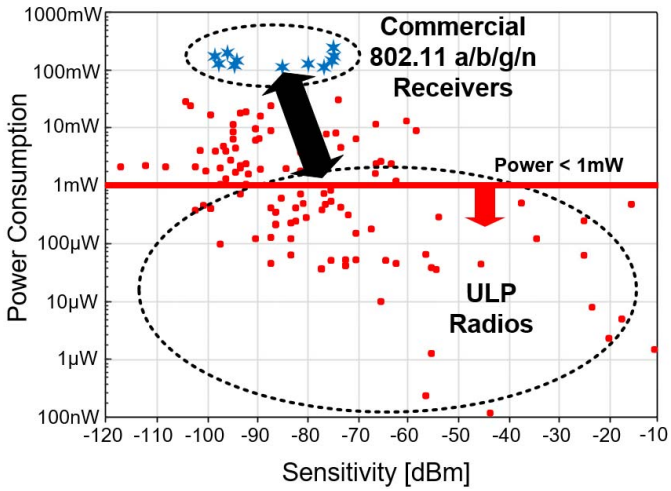

Fig. 1. ULP radio survey from 2005 to present. Red data points of the radio survey are from top conferences (ISSCC, VLSI, RFIC, and CICC) and commercial TRx chips. The blue stars are reported performance of commercial 802.11 a/b/g/n radios.

More recently, work has focused on bridging the gap between commercial 802.11 receivers and ULP radios, such as the 802.11ba task group for future deployments, and back-channel communication for backward compatibility [6], [7].

The 802.11ba task group established a new standard to reduce the average power of 802.11 radios by integrating a low-power companion radio with the main 802.11 radio, which receives ON-OFF keying (OOK) modulated signals (4 MHz, 13 subcarriers populated a long 20-MHz channel) from an 802.11 transmitter. The power budget of an active Wi-Fi network can be significantly reduced by leveraging a wake-up radio when the main Wi-Fi radio remains asleep [8]. Wi-Fi back-channel communication is also presented [9], which generates a wideband, simple modulation scheme such as frequency shift keying (FSK), OOK, and pulsed phase shift keying (PPSK) by streaming a crafted bit sequence to the 802.11 data path. Receivers were presented which support these Wi-Fi wake-up modes, however, the sensitivity of −72 dBm [6], [7] is somewhat limiting compared to Wi-Fi radios at < −80 dBm.

This paper is the extended version of [10]. In this paper, an ULP 802.11ba WUP is presented with a sensitivity of −83 dBm while consuming 220 μW with a one-fourth of the coding rate. The receiver minimizes power by using passive mixer-first architecture. Furthermore, the third har-

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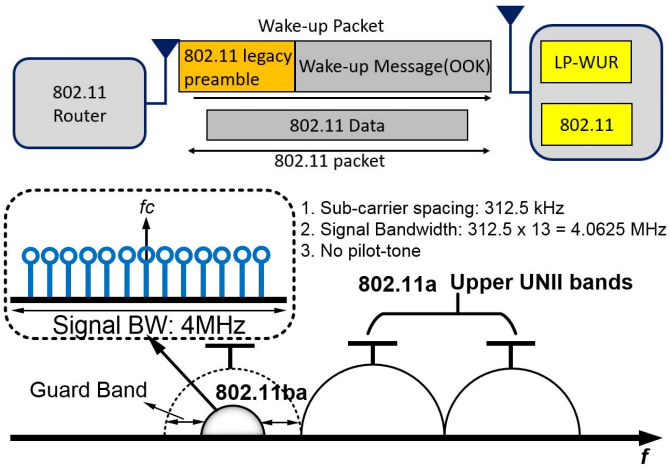


Fig. 2. Conceptual diagram of the 802.11 LP-WUR application (top) and frequency floor planning of 802.11ba (bottom) [8].

monic down-conversion is used which requires a ring-based LO operating at one-third of the RF frequency—reducing power in the LO and LO drivers. The receiver uses a three-path third harmonic mixer that enhances the third harmonic component while rejecting the fundamental component through the mixer. In addition, a 1:3 transform is used for passive voltage gain before the passive mixer to achieve an overall NF of 14 dB, resulting in the best sensitivity-power tradeoff among >3-GHz ULP receivers, and Wi-Fi wake-up radios.

This paper is organized as follows. The 802.11 low-power WUR (LP-WUR) OOK frequency planning and its (de)modulation is covered in Section II. Detailed circuit architectures and analysis of the third harmonic down-conversion and its matching network, and other circuit blocks in Section III. Measured results of the receiver and comparison with past ULP down-conversion receivers are discussed in Section IV. Finally, Section V concludes this paper.

II. Frequency Plan and System Architecture

The frequency planning of the 802.11 LP-WUR is shown in Fig. 2. Legacy Wi-Fi orthogonal frequency-division multiplexing (OFDM) signals are generated by modulating subcarriers in the frequency domain, converting subcarrier symbols to the time domain, outputting them through a digital-to-analog converter (DAC), and finally up-converting the signal to RF. This OFDM architecture theoretically allows for a wide set of modulations such as OOK or M-ary FSK, although it is not specifically designed for this type of signal generation. By only updating the firmware of an 802.11 OFDM radio [7], [8], it is possible to map narrowband OOK or FSK symbols onto OFDM subcarriers and disable the remaining unused subcarriers.

As shown in Fig. 2, the 802.11 LP-WUR signal can be generated by selectively allocating power to a subset of subcarriers, which are OOK modulated. The maximum symbol rate of the Wi-Fi wake-up data is 250 kS/s, the same as the OFDM symbol rate. As subcarriers are 312.5 kHz apart, the resulting 13 subcarriers OOK WUR signal has a bandwidth of 4 MHz, which is wider than conventional ULP transceivers [7], [8]. The proposed frequency plan has a symmetric power allocation on double-sided bands (DSB). According to studies that have been done in [7] and [8], DSB symmetric power allocation with a single noisy LO with an extremely small loop bandwidth FLL (<10 kHz) does not introduce significant effect on the sensitivity compared to single sideband (SSB) asymmetric power allocation without the image on the other side of the carrier. This removes the requirement for quadrature mixing at the receiver, and the multicarriers are shifted slightly above the center frequency to avoid flicker noise floor when demodulating the wake-up signal.

As shown in Fig. 2, 802.11ba is utilizing the existing 802.11a upper UNII bands so that it has a 4-MHz signal BW, with 8-MHz guard bands on each side, which relaxes the phase noise (PN) and filtering requirements of the receiver design. Compared to full band 802.11a that utilizes 52 subcarriers, this saves four times the signal bandwidth and relaxes the required signal-to-noise ratio (SNR) of the receiver by 6 dB, while providing more margins on interferer rejection as well due to larger guard space between channels.

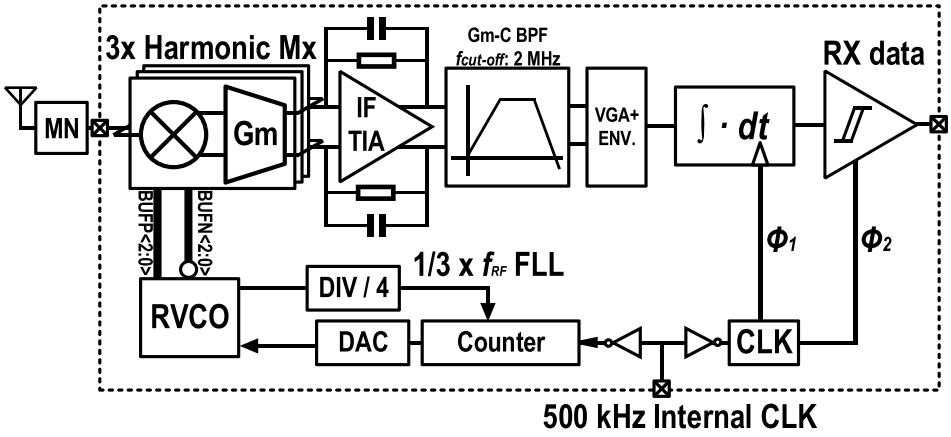
The system architecture is shown in Fig. 3, which performs direct down-conversion. Although the WUR signal is generated from an 802.11 OFDM transmitter, the receiver does not require a highly linear RF front-end, high-resolution analog-to-digital converter, or significant digital baseband processing due to its relatively simple wideband (de)modulation scheme.

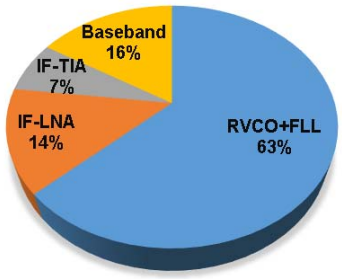
III. Circuit Implementation

For active wireless connectivity, the WUR has to achieve a sensitivity of the lowest data rate of 802.11a transmitter, which is −82 dBm at a data rate of 6 Mb/s [7]. Thanks to the modulation explained in Section II, the minimum noise figure has been relaxed due to the relaxation of the SNR. This allows us to eliminate the power-hungry active RF gain stage in the WUR.

The system block diagram of the 802.11 LP-WUR is shown in Fig. 3. The receiver is passive mixer-first architecture with an off-chip matching network. Rather than using an LO-less RF energy detection architecture, which is common among ULP receivers because it results in the lowest active power, this receiver uses a ring-based voltage controlled oscillator (RVCO) to allow channel selection, improve selectivity, and operate at a lower active power than more power hungry *LC*-voltage-controlled oscillator (VCOs). The receiver receives 4-MHz-wide OOK modulated RF signals in the 5.5–5.8-GHz band, compliant with the 802.11ba draft standard. These are down-converted with mixers that operate around one-third of the RF frequency.

To reduce power, no active RF gain stages are used. However, to maintain adequate sensitivity, a passive voltage gain is implemented in the matching network. After the three mixer stages, the down-converted IF signals are combined in the current domain before amplification and filtering in TIA. After the TIA, the IF signal is filtered with a −40 dB/dec roll-off. Finally, the filtered IF signal is rectified, and integrated by baseband circuits, and the RX data is retrieved. The following sections will explain the details of each system block.





	RVCO+FLL	IF-LNA	TIA	Gm-C Filter	Env.	Int.	Bias Circ.	Ext. Clock
Power [μW]	137	30	15	15	5	5	10	3

Fig. 3. System block diagram of the receiver (left) and its power portion for each block.

A. Third Harmonic Mixer-First RF Front-End

As shown in Fig. 4, the ULP 802.11ba WUR uses a passive mixer-first RF front-end which down converts the 5.8-GHz 802.11 RF signal with the third harmonic generated from the RVCO. This saves power because neither the oscillator nor the LO buffer, which are the most power-hungry blocks as shown in the pie chart in Fig. 3, is required to operate at 5.8 GHz. Subharmonic down-conversion architectures have been proposed in [2], [9] for low-power receivers that perform frequency multiplication from a low-frequency oscillator by using either logic or injection locking of high-frequency reference clocks. The drawback to this approach is they still require significant power in the LO buffers and fast logic circuits. In contrast, the highest frequency that is generated and/or used in this receiver is $f_{\mathrm{RF}}/3$, or 1.933 GHz, thus significantly reducing the active power of the RVCO and buffers. Odd harmonic down-conversion was chosen rather than even harmonic down-conversion because it has a better flicker noise corner versus power tradeoff of the RVCO, which will be covered in Section III-C.

The spectrum diagram in Fig. 4 illustrates the behavior of each block that comprises the RF front-end. The RF signal is filtered and impedance boosted as shown in Fig. 4(a). A commutating passive mixer has a nonlinear response, so that at Fig. 4(b), when feeding an LO operating at f_{LO} to the mixer, it produces harmonic components at $(2n-1)\times f_{\mathrm{LO}}$ (n is an integer). The actual passive mixer is a differential pair that rejects even-order harmonics after down-conversion. The down-converted signals after each mixers are summed in the current domain using IF low-noise amplifier (IF-LNA). Then, in Fig. 4(c), the summed signal is filtered, and amplified by TIA. Fig. 5 shows the schematics of the IF-LNA and TIA. The IF-LNAs are self-biased by connecting each differential IF-LNA output to the mixer input with a triode resistor that provides large resistance, thus only regulating the dc common-mode voltage. The construction and destruction of each harmonic components happen at Fig. 4(c). By combining signals from N-paths with mixers operating at a 360°/N phase difference each, the Nth harmonic signals at the outputs of the N mixers will be in-phase at baseband, while the other harmonic components are out-of-phase and cancel.

The behavior of the Nth harmonic down conversion can be expressed with an equivalent mathematical expression. The RF signal at the input of the passive mixer can be expressed as $V_{rf}(t)$, and the RF switch based mixer can be expressed as the Tayler series of a square wave. As shown in (1), after voltage–current conversion from the IF-LNA input (Gm), the down-converted RF signal before the TIA can be expressed as

$$G_m V_{rf}(t)\left[\sum_{k=1}^{N}\sum_{n=1}\frac{A_0}{2n-1}\cos\left((2n-1)\left(\omega_{\mathrm{LO}}t+\frac{2\pi}{N}k\right)\right)\right] = G_m V_{rf}(t)\sum_{l=1}\frac{NA_0}{N(2l-1)}\cos(N(2l-1)\omega_{\mathrm{LO}}t). \quad (1)$$

The noise figure of the third harmonic passive mixer front-end can be determined by the insertion loss of the passive mixer and noise folding from the higher/lower harmonics. As the number of paths, N, increases, the insertion loss increases, along with the number of higher/lower harmonics up to the frequency of interest. The switch noise is suppressed with current summation after the IF-LNA because the correlated down-converted RF signal adds constructively in current, while the uncorrelated switch noise only adds in power. Simulation results of the power and NF for each harmonic passive mixer down-conversion is shown in Fig. 6. Increasing N beyond a value of 3 offers diminishing returns in NF versus active power. Comparing to edge combining duty-cycled frequency multiplication mixer, this saves a decent amount of power because it uses a small number of RF switches and does not require any high-speed complex logic circuits. Considering noise analysis, and mismatch calibration, this architecture shows an optimal tradeoff between performance and power with $N = 3$ so that a third harmonic three-path passive mixer is implemented.

Including differential RF signaling, the third harmonic passive mixer architecture requires $2N = 6$ mixers operating at f_{RF}/N. The number of LO buffers and RF switches used

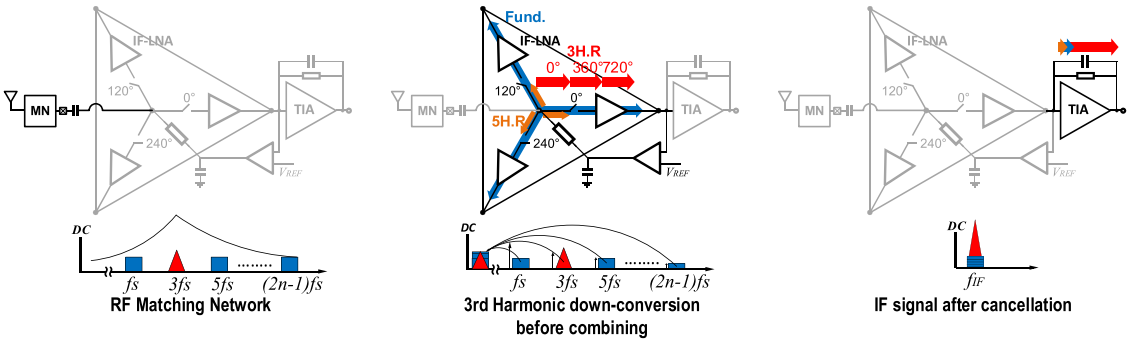


Fig. 4. RF front-end of the receiver using the third harmonics down-conversion in single mode (actual RF front-end uses a differential passive mixer). (a) RF matching and filtering at the RF input node. (b) Third harmonic down-conversion. The IF-LNA after the passive mixer induces current from down-converted voltage for current combination. (c) Induced currents are combined, improving third harmonics while rejecting other harmonic components.

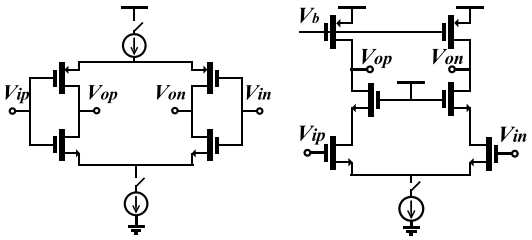


Fig. 5. IF circuits. Single cell of the IF-LNA (left) and the TIA (right).

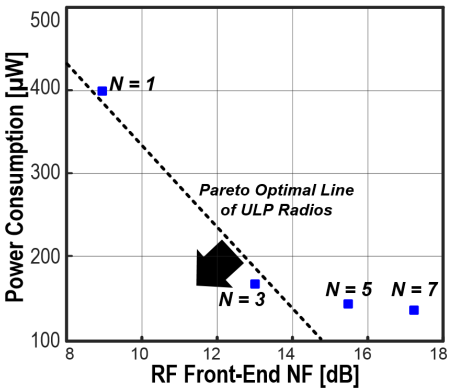


Fig. 6. Simulation results of NF versus power tradeoff of Nth harmonic passive mixer RF front-end. Line: Pareto optimal line of state-of-the-art ULP receivers.

for the RF front-end is two times fewer than in [2], a harmonic mixing architecture using injection locking. These buffers wind up being the dominant factor of the overall ULP receiver power consumption. Furthermore, this architecture does not inevitably require a high-Q RF filtering stage in front of the mixing stage due to undesired harmonic spurs generated from the subsampling mixer down-converting unwanted signals to the IF band, as in [11]. Instead, these unwanted signals cancel in the current-domain at baseband after the mixers because they arrive out of phase. As shown in Fig. 4, the subharmonic passive mixer only requires N narrowband IF-LNAs, which is a good tradeoff for ULP radio designs because these operate at significantly lower power than RF stages.

B. Matching Network and NF Optimization of RF Front-End

Many mixer studies have been published on methods to improve the linearity of receivers [12], [13].These references

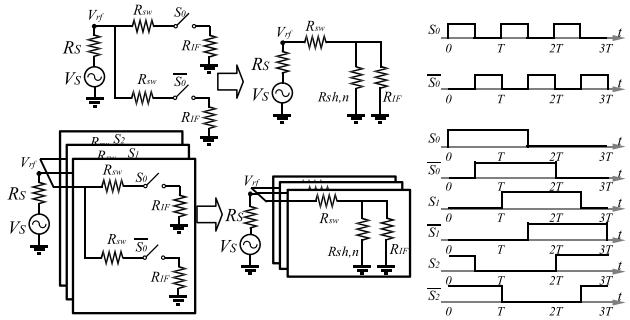


Fig. 7. Two-path passive mixer linear time-invariant equivalent model (top) [3], [13], and the third harmonic linear time-invariant equivalent model (bottom).

go through a noise analysis assuming sufficient wideband matching to a 50-Ω terminal, assuming a low switch resistance (usually $< 50\ \Omega$). Low switch resistance is achieved by wide FETs, driving up the LO buffering requirements and thus the power. This mixer-first architecture has much higher high switch resistance from the mixer switches because it has a low VDD and narrow FETs to reduce the power from the LO buffers. In this paper, an FET of 3 μm/60 nm is chosen which has a switch resistance of more than 300 Ω at 5.8 GHz. Therefore, the input impedance at the RF node is large, which would usually require a high-quality factor off-chip matching network to provide sufficient matching.

The third harmonic passive mixer can be easily matched with a 50-Ω interface with high resistive switch resistance. According to the equation from [3], [13], $R_{sh,n}$ in Fig. 7 is expressed as

$$R_{sh,n} = \frac{2\gamma\,(R_S + R_{\rm sw})R_{\rm IF}}{2(R_S + R_{\rm sw})(n^2 - \gamma) + R_{\rm IF}(n^2 - 2\gamma)}, \quad n = 1, 3, 5, \ldots. \tag{2}$$

The input impedance of the two-path passive mixer can be derived based on the linear time-invariant equivalent model as

$$Z_{\rm in}\,(n\omega_{\rm LO} + \omega_{\rm IF}) = \left[R_{sw} + \left(R_{sh,n} \| R_{\rm IF}\right) \| \left(\frac{1}{jn\omega_{\rm IF}C_{\rm IF}}\right)\right], \quad n = 1, 3, 5, \ldots. \tag{3}$$

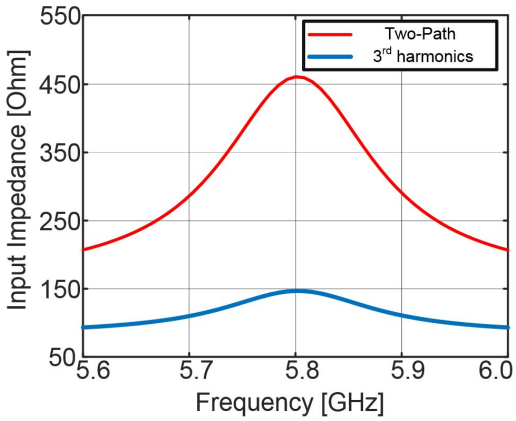


Fig. 8. Input impedance of the two-path fundamental mixer and the third harmonic mixer.

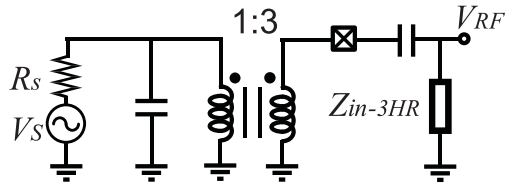


Fig. 9. RF matching network of the third harmonic passive mixer.

The input impedance of the third harmonic passive mixer in Fig. 7 can be expressed as

$$Z_{in-3HR} = \frac{Z_{in}\,(3\omega_{\mathrm{LO}})}{3} = \frac{R_{sw} + \left(R_{sh,3} \| R_{\mathrm{IF}}\right)}{3}. \quad (4)$$

Assuming that $R_{\mathrm{IF}} = \infty$, setting $R_{\mathrm{sw}} \cong 2.82R_S$ will match the third harmonic passive mixer input impedance Z_{in-3HR} to R_S. For example, if matching to a 50-Ω terminal, the switch resistance has to be roughly 141 Ω for a third harmonic passive mixer. Fig. 8 shows the input impedance of a two-path and third harmonic passive mixer over frequency.

For acceptable noise figure, with good matching, the low-power mixer first architecture requires a step-up transformer [12]. The effective input impedance seen from the RF node is around one-third of a single balanced passive mixer. As can be seen in Fig. 9, the RF node is interfaced with 1:3 RF transformer to provide matching and passive voltage gain. This approach helps to achieve the required sensitivity with an NF <16 dB (calculated from an −82-dBm sensitivity requirement).

Ideally, the front-end can perfectly reject the fundamental RF component while down-converting signals at the third harmonic frequency. However, two mismatch factors affect this rejection ratio (third harmonic/fundamental). Mismatch in the delay cells of the RVCO generates phase mismatch which reduces the rejection ratio as this mismatch increases. However, the dominant factor is a gain mismatch in the first inverter-based IF stage, which impacts the rejection ratio due to its common mode offset between IF-LNAs. According to simulation, a phase error of less than 5% results in a rejection ratio up to 40 dB.

To minimize the gain mismatch, self-biased current steering differential IF amplifiers are used with fine resolution gain tuning. Without calibration, there were large variations observed chip to chip, and the worst rejection ratio measured was 25 dB. After calibration, the worst rejection ratio measured was 37 dB, including passive RF matching before the RF front-end.

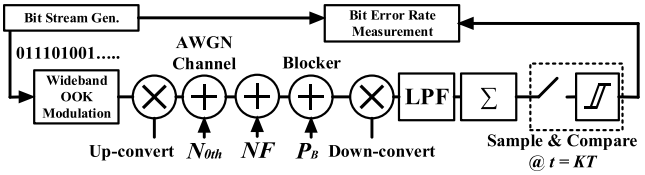


Fig. 10. Equivalent model of the WUR for PN and blocker analysis.

C. LO Analysis and Generation

For low power design, an RVCO is used for the RF oscillator; however, this can result in degradation of the sensitivity due to tone spreading from the high PN of the RVCO. High PN also limits the blocker tolerance [14] of the receiver. This section explains how PN of the RVCO was chosen, and the impact on system performance.

Fig. 10 shows the equivalent model of the 802.11 WUR that was implemented to define the PN profile that achieves a sensitivity of −82 dBm, considering a target NF, while rejecting interferers of >20 dB. The following describes the design and simulation procedure. First, the number of samples was chosen which can easily show the bit-error-rate (BER) performance, then, the bit sequence for each sample was randomized. Based on the current bit, a 13 subcarrier, 4-MHz-wide OOK modulated baseband signal was generated. The baseband signal was up-converted with an input power of the target WUR sensitivity level. Then, thermal noise with the WUR's noise figure and blocker power were added to the RF signal, which was then direct down-converted. After the second-order low pass filtering and integration, the signal was sampled and compared every 4 μs. The retrieved bit sequence was compared with the input randomized bit sequence and BER was measured.

First of all, we focused on the PN at a frequency offset of <2 MHz because it directly relates to the in-band power loss due to the tone-spreading. This approach has been done to achieve the optimal point of the LO design that minimizes the tone spread along with the 4-MHz signal bandwidth while also minimizing the active power consumption of the RF oscillator. Fig. 11 shows the BER results as a function of PN of the RVCO for the desired channel and the adjacent channel. According to the simulation, the in-band PN of −75 dBc/Hz at an offset frequency of 1 MHz is been chosen which achieves the BER of 10^{-3} within signal level of −82 dBm. Then, blocker RF power at the adjacent channel (20-MHz offset frequency) was inserted along the AWGN channel to specify the PN at a high frequency offset over 10 MHz. Theoretically, PN profile for out-of-band blocker rejection can be chosen by the following equation. Assuming noise from the blocker's tone spread due to the PN dominates the total noise floor ($N_{\mathrm{Blocker}} \gg N_{\mathrm{thermal}}$), the SNR of the receiver when the blocker is present can be expressed as:

$$\mathrm{SNR}_{\mathrm{blocker}}\,[\mathrm{dB}] = (P_C - P_B)\,[\mathrm{dBm}] - \mathcal{L}_{\mathrm{LO}}\,(\Delta f)\,[\mathrm{dBc/Hz}] - 10\log BW\,[\mathrm{dBHz}] \quad (5)$$

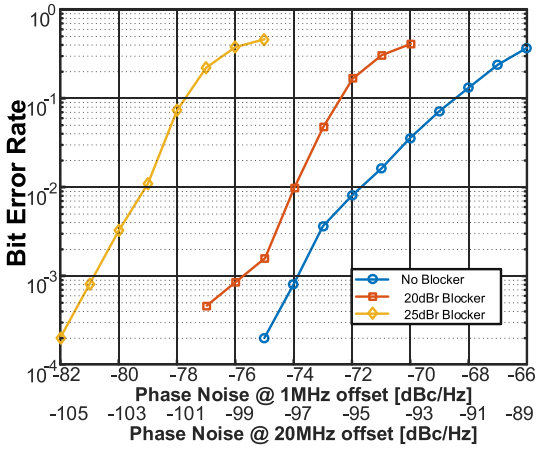


Fig. 11. BER versus PN analysis with a different blocker power. NF and target sensitivity were considered in this plot.

where P_C is the carrier power on the desired channel and P_B is the blocker power [14]. In order to achieve adjacent channel blocker rejection of >20 dB with the minimum required SNR of 12 dB [8]

$$\mathcal{L}_{LO}(\Delta f = 20\ \text{MHz}) \leq -20\,[\text{dB}] - 10\log(4\ \text{MHz})\,[\text{dBHz}] - \text{SNR}_{\text{blocker,min}}\,[\text{dB}] = -98\,[\text{dBc/Hz}]. \quad (6)$$

With practical understanding, the low active power RVCO's noise corner of $1/f^3$ easily exceeds 1 MHz, and we applied a PN slope of < -20 dBc/Hz^2 above a 1-MHz frequency offset.

To achieve this PN specification with minimum active power, time-interleaved RVCOs (TI-RVCOs) from [15] are used for the LO design that can achieve better PN specification at a certain offset frequency for a narrowband application that can provide better power efficiency when compared to conventional RVCOs. Using a harmonic component from a lower operating frequency, TI-RVCO results in a lower $1/f^3$ frequency corner at the target RF frequency when compared to an RVCO that operates directly at the target RF frequency. This results in better PN versus power efficiency for harmonic TI-RVCOs. Furthermore, the power dissipated from the divider in a TI-RVCO based FLL operates at a lower frequency, further reducing power. In [15], logic cells are used to multiply the frequency of a TI-RVCO. However, in this design, the low-frequency LO signals are directly applied to the mixer which performs harmonic mixing, saving power from high-speed logic.

To aggregate three phase offsets from the RVCO that runs at $f_{RF}/3$, a 9-stage differential RVCO was chosen. As shown in Fig. 12, the LO is comprised of a 9-stage differential TI-RVCO and counter-based programmable FLL with a low frequency reference for frequency calibration. The DAC counter decides to increase/decrease the RVCO current based on a duty-cycled counter value. The counter counts frequency pulses from the divider for several reference cycles to improve the center frequency resolution. When the counted value exceeds the target reference value, the IDAC current is reduced, and vice versa when the value is lower than the reference value. For fine settling, the FLL updates its code

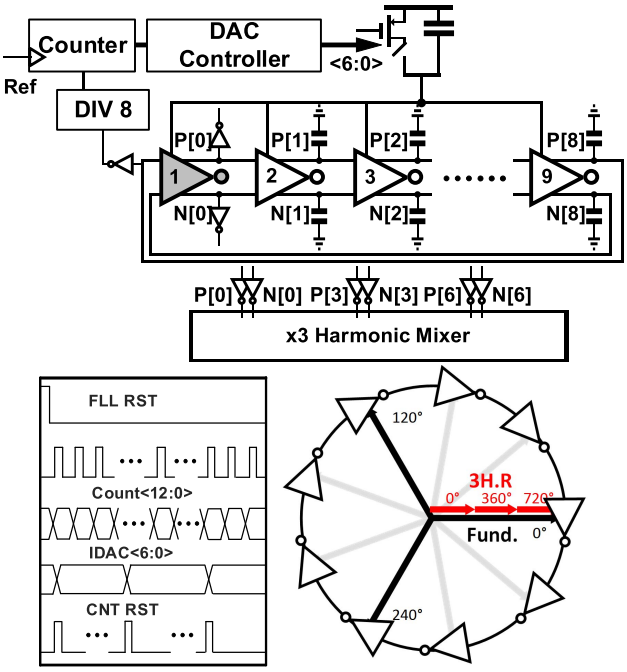


Fig. 12. Frequency-locked loop of the receiver (top), timing diagram of the FLL (bottom left), and conceptual diagram of phase aggregation for the third harmonic improvement (bottom right).

word for every 16 reference cycles, which is 32 μs. For coarse settling, the IDAC changes with larger steps with two reference cycles when the absolute value difference between the counter and reference is over a programmable threshold.

D. Intermediate Frequency and Baseband Circuits

After the third harmonic down-conversion, the OOK data are retrieved after IF gain stages and energy collection stages. As shown in Fig. 4, the IF signal is low pass filtered with an IF center frequency below 2 MHz. The second-order Gm-C filters with gyrators were used for each filter design that can mitigate the distortion that comes from the down conversion of out-of-band blockers [12]. To achieve an adjacent channel signal-to-interference ratio (SIR) better than -20, -40 dB/dec roll-off is required with the given RVCO PN profile. The baseband filter has a high pass corner frequency of 20 kHz, which is close to one-third of the WRX data rate. Utilizing a scrambler in the 802.11 data path, we avoid a bit stream of more than four consecutive equal bits, which is sufficient to stay above the high-pass corner. The filtered signals are envelop-detected and then integrated, then finally compared with an on-chip voltage reference with a 1-bit comparator. The integrator is oversampled by an external clock to determine the symbol boundaries. The measured gain provided by the baseband is 23 dB.

IV. Measured Results and Comparisons

The 802.11 WUR was fabricated in a 40-nm CMOS technology with an active area of 0.151 mm^2, as shown in Fig. 13. The receiver is operating at 5.5–5.8 GHz with a signal bandwidth of 4 MHz, which utilizes only part of the 802.11a upper UNII band. The 802.11 WUR uses a 500-kHz external clock and

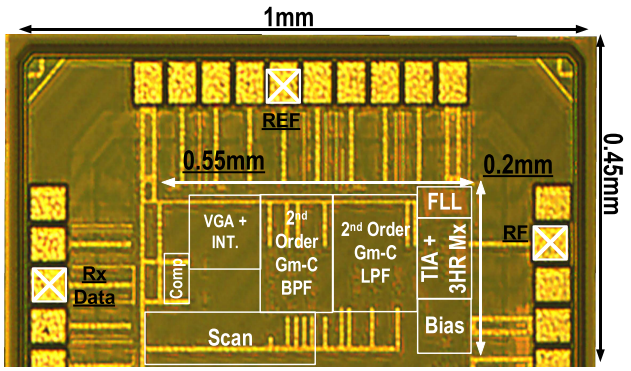


Fig. 13. CMOS 40-nm chip photograph.

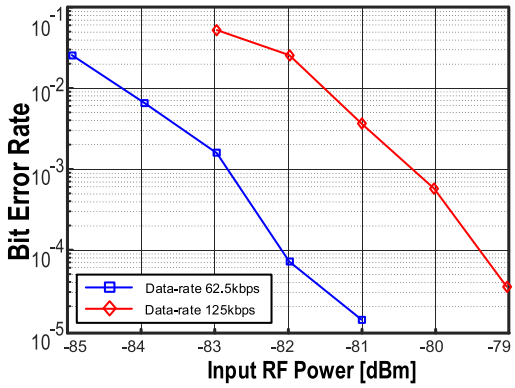


Fig. 14. BER waterfall curve at different data rates.

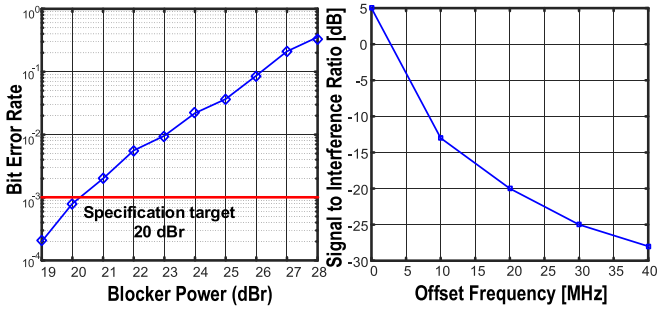


Fig. 15. BER versus blocker power of the adjacent channel 1 (left) and SIR versus offset frequency (right).

transformer as off-chip components. Fig. 14 shows a measured BER waterfall curve. The BER is measured with alternated 802.11ba data. The sensitivity of the 802.11 WUR is −83 dBm at the BER of 10^{-3} and data rate of 62.5 kb/s. The sensitivity got 3-dB increment as the data rate increased twice, which is 125 kb/s. The tone-spread of down-converted RF signal due to PN degraded power is captured in 4-MHz bandwidth by 1 dB.

Interferer measurements are done with randomized binary data. Fig. 15 shows blocker performance of the 802.11 WUR. The left figure in Fig. 15 shows BER performance in different blocker power at adjacent channel 1, which has 20-MHz offset from the desired center frequency. The SIR of adjacent channels 1 and 2 are −20 and −28 dB, respectively. The interference performance can be limited by the PN of the RVCO, thus, for narrowband receivers, SIR performance is

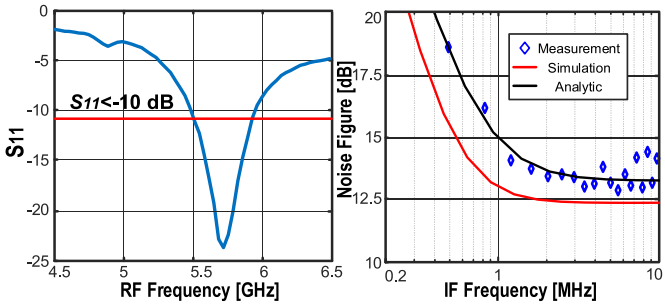


Fig. 16. S_{11} and noise figure of the receiver.

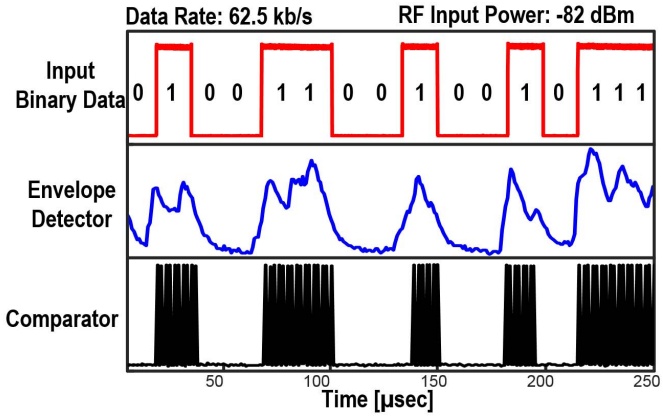


Fig. 17. Receiver outputs from final bit decision inter stages. The 802.11ba data are randomized with ¼ coding rate.

dominated by PN rather than the order of the filter when the order is reasonably high ($\geq$3).

The measured noise figure and S_{11} are shown in Fig. 16. The noise figure of the system is 14 dB across the signal bandwidth, which matches simulations very well. However, the measured flicker noise corner had a slight deviation between the simulation result, which was within the range of PVT variation. By boosting the input impedance, the receiver was able to achieve $S_{11} < -10$ dB across the desired band of 5.5–5.8 GHz.

Fig. 17 is showing demodulated randomized RF data. The down-converted signal is integrated and oversampled by the comparator by eight times to find the symbol boundary. The input RF power was −82 dBm.

The measured LO leakage power at the RF input was −92 dBm at 5.8 GHz. The active power of the 802.11 WUR is 220 μW and its detail power break-down and pie chart are depicted in Fig. 3. As shown in the pie chart, two-third of the power is consumed by the RF blocks. The 500-kHz reference clock generation which can be realized with a 3-μW crystal oscillator is included. Table I summarizes the performance of the receiver with state of the art Wi-Fi wake-up radio and high operating frequency ULP receivers which have the best performance in sensitivity-power tradeoff. According to the ULP survey shown in Fig. 18(a), the receiver advances the Pareto optimal line of >3-GHz receivers in sensitivity-power tradeoff. Based on the data rate of the receiver, Fig. 18(b) shows the ULP receiver survey with normalized sensitivity

TABLE I
COMPARISON WITH STATE-OF-THE-ART ULP RADIOS

	[16]	[3]	[7]	[6]	This Work
CMOS Tech. [nm]	90	65	14 FinFET	65	40
Active Area [mm^2]	0.9	0.058	0.19	0.228	0.151
External Component	1 MHz External Clock	High-Q inductors	32 kHz RTC	250 kHz External Clock Off-chip RF Filter	500 kHz External Clock Off-chip Transformer
Carrier Frequency [GHz]	3-5	2.4	2.4	5.8	5.5-5.8
Voltage [V]	1	0.5	0.95	1	0.95/0.55**
Modulation	FM-UWB	OOK	OOK	FSK	OOK
Sensitivity [dBm] @ 10^{-3}	-80.5	-97/-92	-72	-72	-83
Active Power [µW]	580	99	95	335	220
Noise Figure [dB]	6.6	20***	23.5***	25***	14
Data Rate [kb/s]	200	10/50	62.5	31.25	62.5
LO Generation	No LO, RF Env.	Unlocked LC-VCO	Ring with FLL	Ring with FLL	TI-RVCO with FLL
SIR*[dB]	-28	-25/-22	-20****	-13	-20
WiFi WUR	N	N	Y	Y	Y

* Adjacent Channel **0.5V for VCO, 0.95V for Analog Blocks
*** *Back calculated from Sensitivity* [dB] = -174 + *signal BW.* + *NF* + *SNRout.* **** ACI rejection measurement

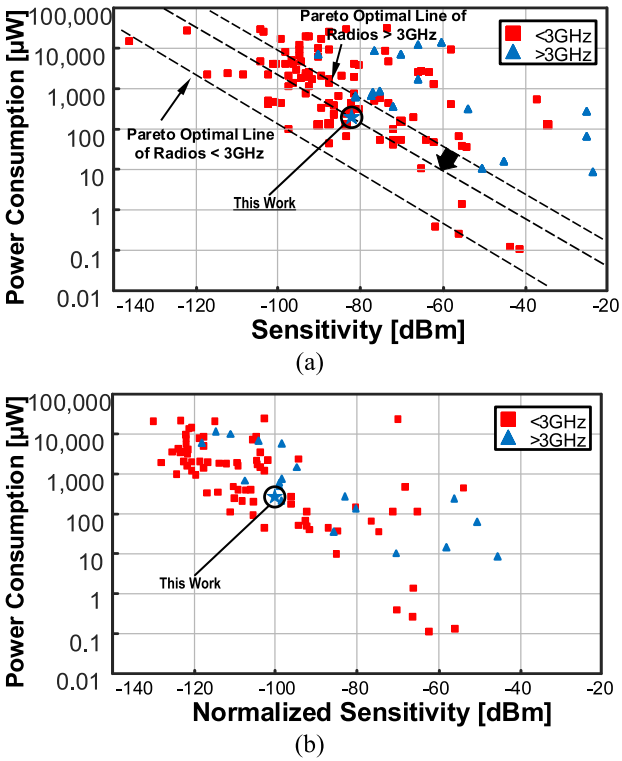


Fig. 18. ULP radio survey from 2005 to present [17]. The data of the radio survey are from top conferences (ISSCC, VLSI, RFIC, and CICC) and commercial TRx chips. (a) Sensitivity versus power consumption. (b) Normalized sensitivity versus power consumption that is weighed to the data rate in kb/s.

that is expressed as

$$P_{\text{Sense,Norm}} = P_{\text{Sense}} - 10\log_{10}\left(\frac{\text{Datarate}}{1\ \text{kb/s}}\right). \quad (7)$$

The sensitivity is normalized to the data rate in unit of kb/s.

V. CONCLUSION

An IEEE 802.11ba LP-WUR receiver is presented. The receiver demodulates OOK modulated messages generated by an 802.11 OFDM Wi-Fi transmitter operating at 5.8 GHz. The third harmonic down-conversion receiver reduces active power consumption while rejecting unwanted harmonic components. Sufficient noise figure was achieved by using a 1:3 transformer that provides gain to a high switch-loss mixer-first RF front-end with good matching across 5.5–5.8 GHz. The receiver achieves a sensitivity of −83 dBm while consuming 220 μW at a BER of 10^{-3} and data rate of 62.5 kb/s, which shows the best sensitivity-power tradeoff among >3-GHz operation frequency receivers.

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