A Receiver/Antenna Co-Design for a 1.5mJ per Fix Fully-Integrated 10x10x6mm^3 GPS Logger

Hyeongseok Kim[1], Nikolaos Chiotellis[1], Elnaz Ansari[1], Muhammad Faisal[2], Taekwang Jang[1], Anthony Grbic[1], Hun-Seok Kim[1], David Blaauw[1], David Wentzloff[1]
[1]University of Michigan, Ann Arbor, MI; [2]Movellus, Ann Arbor, MI
E-mail: hskims@umich.edu

***Abstract*— This paper presents an ultra-low-power (ULP) GPS logger system that features a custom miniaturized antenna co-designed with a GPS analog front-end (AFE) optimized for heavy duty-cycling and a 10x10x6mm^3 form-factor. The complete system includes a GPS AFE, processor, two custom 8Mb flash memory chips, custom antenna, and a 12mAh polymer Li-ion battery. An electrically small differential loop antenna (*ka* value of 0.24) is designed and all components are integrated on the top and bottom of the antenna in close proximity without degrading the antenna efficiency. In the sleep mode, the processor and the timer consume 50nW and in active mode it draws 12.5mW from a 1.2V supply. The AFE achieves a maximum conversion gain of 72dB, a noise figure of 2.2dB, and P1dB of -46dB. The blocker level that desensitizes the gain by 1dB is -6.1dBm at 1710MHz, one of the closest blockers near the GPS bands. The GPS logger achieves a 10dB SNR after correlation at an input power level of -125dBm. The logger is capable of storing data for 37 position fixes by streaming 10ms of received signal per fix to dual flash memories for later egress and post-processing.**

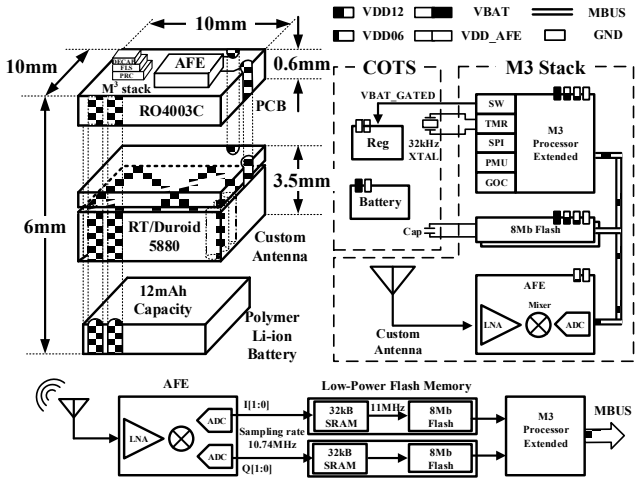

Fig. 1. Conceptual diagram and overall system block diagram of the proposed GPS logger for 10x10x6mm^3

I. Introduction

There is a growing demand for low-power, millimeter-scale GPS tracking systems. Interest in these systems is driven by the desire for small form factor and long lifetime for applications such as wearable devices, asset trackers, and drones. One of the main challenges when miniaturizing GPS tracking systems is power consumption. Millimeter-scale batteries have limited capacity and low peak current levels, both of which present challenges for powering a GPS AFE for acquiring signals and flash memory for storing sampled data. A second challenge is the antenna design. At millimeter-scale, a GPS-band antenna is electrically small, and as a result efficiency can suffer. Finally, there is the challenge of integrating the entire system together, in particular for the RF performance, because all components, including the battery and ICs, need to be placed in close proximity of the antenna. This paper presents a complete GPS logger system that features a custom antenna co-designed with a GPS AFE optimized for heavy duty-cycling and a 10x10x6mm^3 form-factor. The complete stack is modeled and incorporating into a differential loop antenna design, which allows integration of components on the top and bottom of the antenna without impacting of antenna efficiency. Furthermore, the antenna and AFE are co-designed to maximize sensitivity. The GPS logger is capable of storing data for 37 position fixes by streaming 10ms of received signal per fix to dual flash memories for later egress and post-processing.

The proposed system is specifically designed for an ULP, fully integrated, and miniaturized GPS logger. As shown in Fig. 1, this GPS logger includes a GPS AFE, ARM Cortrx-M0 processor, two custom 8Mb flash memory chips, custom antenna, and a 12mAh polymer Li-ion battery with a total system volume of 10x10x6mm^3. The AFE turns on for 10ms intervals, sufficient to capture one GPS fix. The AFE boots up and shuts down in 20us, minimizing the energy overhead from startup. Since highly accurate time is kept, the AFE can also turn on precisely when new satellite ephemerides are broadcast and sleep during the rest of the transmission. When the AFE is operating, the quantized 2 bits I/Q signals at the ADC are captured for 10ms at a 10.74MHz sampling rate. The off-line correlation is performed with the expected PN sequence of the GPS satellite signal. An electrically small GPS antenna has an overall size of $0.05\lambda_0$ x $0.05\lambda_0$ x $0.018\lambda_0$. For easier integration, the inter-connection between the AFE and antenna is through castellated holes in the PCB.

II. Overall GPS Analog Front-end (AFE) Receiver

The overall block diagram of the GPS AFE is shown in Fig. 2(a). It includes a low noise amplifier (LNA), an active double

978-1-5386-2483-8/18/$31.00 ©2018 IEEE

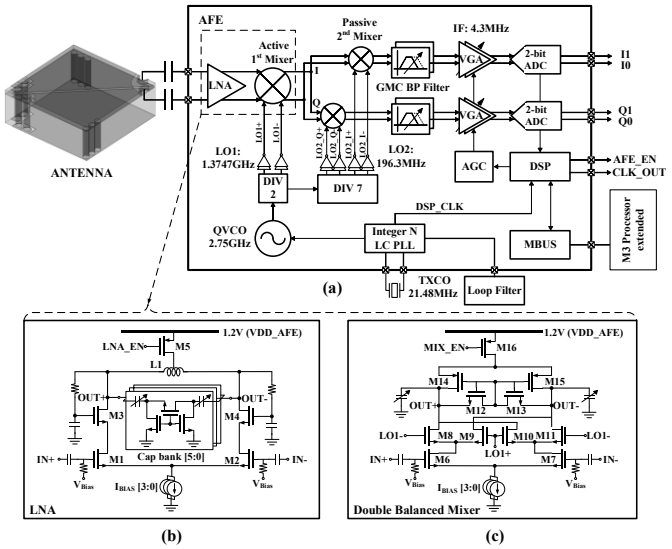

Fig. 2. (a) Overall block diagram of AFE, (b) simplified schematics of the LNA, and (c) simplified schematics of the active mixer

balanced mixer, passive mixers, IF filter, a VGA, a 2 bits ADC, digital baseband with an automatic gain control (AGC) loop, frequency synthesizer, DSP and MBus interface connecting the chip with the system processor. When the AFE is powered, the MBus interface and DSP blocks are always-on, while the rest of blocks are in stand-by mode until receiving an enable signal from the processor.

The entire receiver employs fully differential quadrature signals. The signal path includes an internal LNA, a Gilbert type double balanced mixer for a 1st down-conversion stage, and an IQ passive mixer for a 2nd down-conversion. Fig. 2(b) depicts the schematic of the differential cascode CS LNA with a tunable LC load. The LC load is reconfigurable to account for PVT variation and filter out out-of-band interferers. The 6-bit cap bank at the LC load also supports covering a range from 1.1GHz to 1.6GHz. The input impedance of the LNA is co-designed with a custom antenna to conjugate match its impedance. The output of the LNA is AC-coupled to a Gilbert type double-balanced quadrature mixer which realizes 1st down-conversion to IF1 (200.7MHz) in Fig. 2(c). A tunable RC bank filters out the interferers after the 1st down-conversion. An I/Q passive mixer, driven by a differential quadrature LO, performs the 2nd down-conversion to IF2 (4.3MHz). The voltage-driven passive mixer is implemented to save the power of the transimpedance amplifier (TIA). The low-IF path is comprised of an IF filter and VGA with an AGC loop. The AGC loop controls the amplification of VGA based on the histogram of the ADC codes to maintain the desired signal level at the ADC input. The ADC quantizes in 2 bit outputs at a sampling rate of 10.74MHz.

An integrated Integer-N PLL is used to provide differential and quadrature signals. The differential LC VCO oscillates at 2.749GHz while LO1 and LO2 are at 1374.7MHz and 196.3MHz, respectively. The LO signal is divided further to provide the sampling clock for the ADC and DSP. It has an external loop filter with a 100kHz bandwidth and a reference clock of 21.48MHz, all integrated within the system depicted in Fig. 2(a).

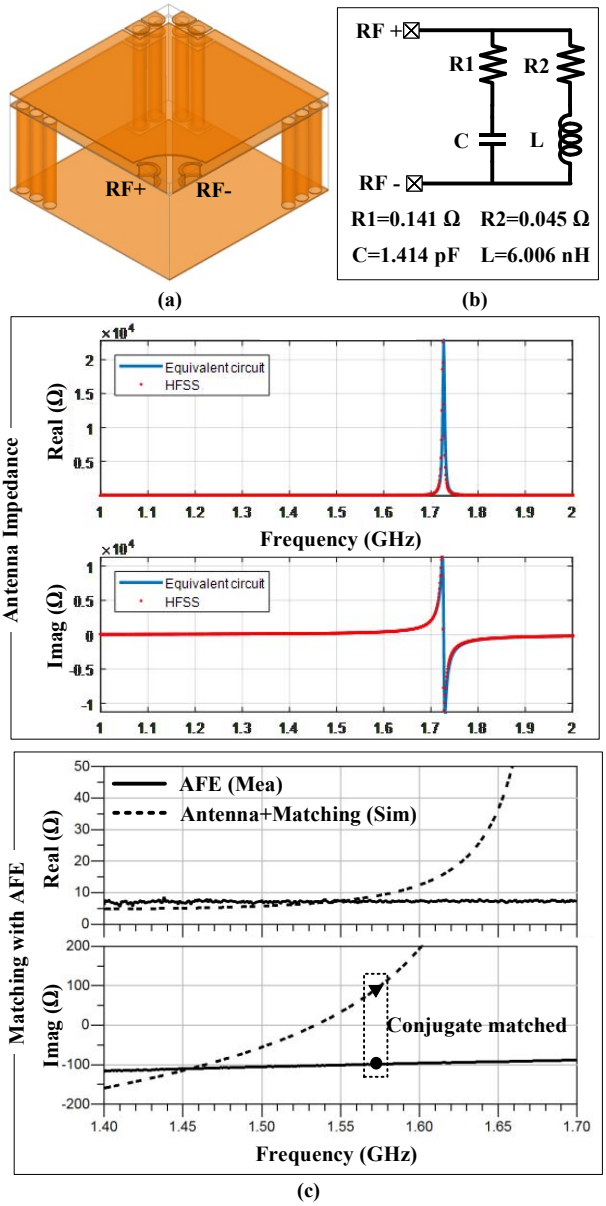

Fig. 3. (a) Miniaturized GPS antenna (b) equivalent circuit (c) input impedance and impedance matching with AFE

III. Custom Designed GPS Antenna

A custom antenna has been developed for the GPS logger presented here. The GPS AFE utilizes a linearly polarized, differentially-fed single-turn loop antenna. It consists of two Rogers RT/duroid® 5880 PCBs with dimensions 10x10x3.175mm^3 and 10x10x0.381mm^3. The thicker board is responsible for reception, while the thinner one shields the antenna from the AFE and provides the necessary routing. As a result, the antenna occupies a 10x10x3.556mm^3 volume and exhibits a *ka* value of 0.24, where k is the wavenumber at the frequency of operation (1.575GHz) and α is the radius of the smallest sphere that encircles the antenna. A *ka* value of less than 1 indicates an electrically small antenna [1].

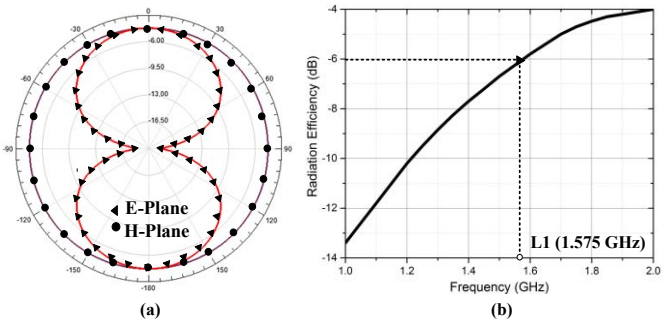

Fig. 4. (a) Radiation pattern (b) radiation efficiency

The antenna, shown in Fig. 3(a), sits under the PCB that contains the AFE and is connected to it through two castellated holes, to which the differential signal (RF+ and RF-) is applied. The four holes on the opposite side provide conducting paths in case another PCB or system (e.g. a PV cell) is attached on the bottom side of the antenna. The RF current travels through the holes to the right, traverses the bottom metal plane, and returns through the holes on the left, forming a loop. Alternatively, the current can jump over the thin gap. Hence, as shown in Fig 3(b), the antenna's equivalent circuit comprises an inductor and a capacitor in parallel. The inductance can be tuned by adjusting the right and left holes' number and radius, and the capacitance by adjusting the gap. The antenna's self-resonant frequency can thus be easily tuned. The design is simulated and optimized in ANSYS Electronics Desktop (formerly HFSS). The antenna operates below resonance at the GPS frequency. This allows it to be subsequently conjugately matched to the AFE using only lumped capacitors in order to maximize the sensitivity of the system (Fig. 3(c)). As expected, its radiation pattern corresponds to that of an electrically small loop (Fig. 4(a)). The input impedance of the antenna prior to matching is presented in Fig. 3(c) and its radiation efficiency (-6dB at 1.575GHz) as a function of frequency are shown in Fig. 4(b).

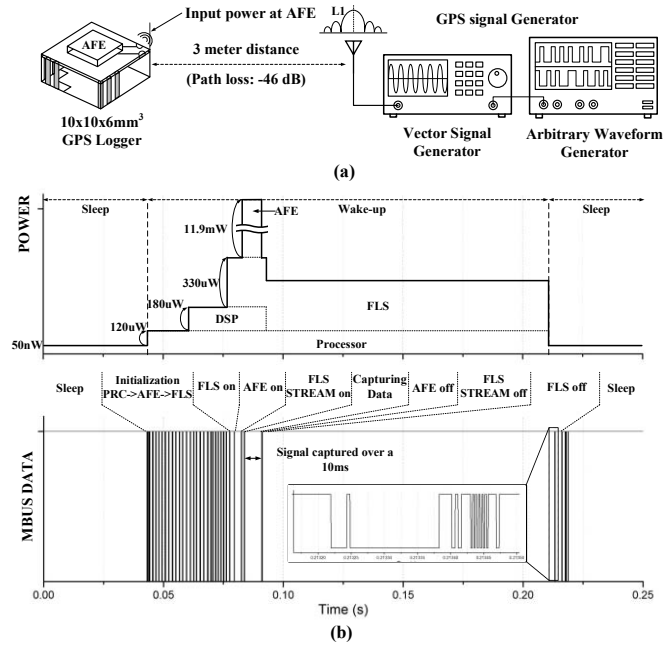

Fig. 5. (a) Measurement setup (b) timing diagram of MBUS data and power consumption for a fix

IV. Measurement Setup and Results

Fig. 5(a) shows a test setup between the GPS logger and the GPS signal generator. The signal generator transmits the L1 C/A-coded GPS signal with PN sequence of any 32 satellite IDs. The antenna, PCBs, and AFE were assembled at mm-scale (Fig. 1) and verified stand-alone, and receiver performance is reported from these stacks. Control signals to the M3 stack and flash connected to a separate PCB, verifying full functionality of the GPS logger recording fixes. Various GPS signal power levels were tested by adjusting EIRP of the transmitter at a distance of 3 meters (-46dB path loss) where ensured radiating at the far field distance in a wireless setup. The AFE and other layers are controlled via MBus, a fully digital energy efficient interconnect bus scheme.

The timing diagram of initial control waveform of MBus and power consumption are presented in Fig.5(b). For initialization, with a wake-up signal, the processor, AFE, and flash are initialized in sequence and then flash start erase operation. This step happens one-time at the initialization. The AFE turn on and off for 10ms and the captured data store in SRAM and transfer to flash memory. The GPS logger get back to the sleep mode when the storing data into the flash is completed. In the sleep mode, the processor and the timer only consume 50nW and in the active mode the total power jumps up to 12.5mW which is dominated by the power consumption from the AFE. From the 12mAh Li-ion battery, the GPS logger can sample 115K fixes and the flash is sufficient to hold ADC samples for 37 fixes before retrieval.

The AFE achieves a maximum conversion gain of 72dB, a noise figure of 2.2dB, and P1dB of -46dB. The measured phase noise of the VCO is -115.6dBc/Hz at 1MHz offset frequency from the LO1 at 1374.7MHz (Fig.6). The blocker level that desensitizes the gain by 1dB is -6.1dBm at 1710MHz, one of the closest blockers near the GPS bands. The measured 3dB CNR degradation level with the CW out-of-band blockers is shown in Fig. 7. The AGC loop is implemented in the controller and regulates the 5-bits VGA control code varying the gain from -13 to 22dB (Fig.8(a)). The ADC outputs are captured over a 10ms and off-line correlation is performed where the captured ADC sample sequence retrieved from flash

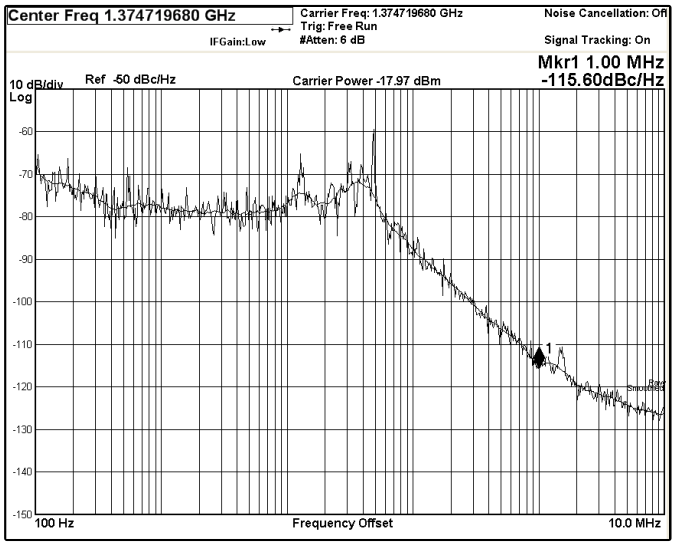

Fig. 6. Measured PLL phase noise at L01 (1374.7MHz)

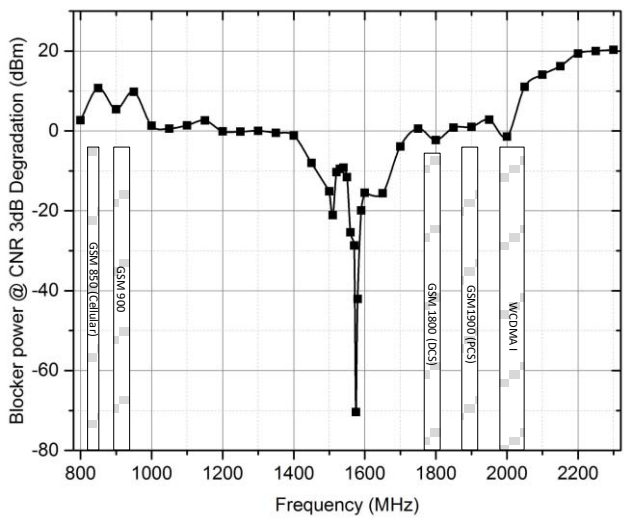

Fig. 7. Measured out-of-band blocking performance

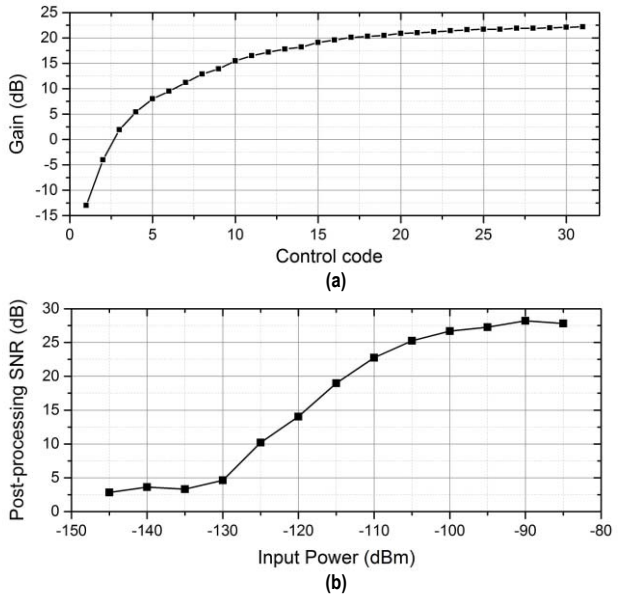

Fig. 8. (a) Measured VGA gain tuning range (b) post-processing SNR in L1

is correlated with the expected PN sequence of the GPS satellite signal. The GPS logger achieves a 10dB SNR after correlation at an input power level of -125dBm with capturing over a 10ms. The results of the post-processing SNR depending on the input power is shown in Fig. 8(b).

V. Conclusion

The fully integrated GPS logger co-designed receiver and antenna is presented. The proposed GPS logger has total volume of 10x10x6mm^3 while achieving 1.5mJ energy per fix. The GPS logger can sample 115K fixes from the 12mAh Li-ion battery before recharging. The flash is sufficient to hold ADC samples for 37 fixes before retrieval. After post-processing by streaming over 10ms, the 10dB SNR required for the GPS logger is -125dBm. In the sleep mode, the processor and the timer only consume 50nW and in the active mode the total power jumps up to 12.5mW. Table I summarizes the measured performance of the GPS receiver with comparison to the state-of-the-art. The AFE is fabricated in a 65nm CMOS process and occupies 2.35x1.5mm^2. The die micrographs of the system are shown in Fig. 9.

References

[1] J. S. McLean., "A Re-Examination of the Fundamental Limits on the Radiation Q of Electrically Small Antennas," IEEE Trans. Antennas Propagat, pp. 672-676, 1996.

[2] N. Qi et al., "A dual-channel GPS/Compass/Galileo/GLONASS reconfigurable GNSS receiver in 65nm CMOS," IEEE CICC, pp. 1-4, 2013

[3] P.Yu, et al., "A 1.2 mm^2 Fully Integrated GPS Radio with Cellular/WiFi Co-existence," IEEE CICC, pp. 919-927, 2010.

[4] C. G. Tan et al., "A universal GNSS (GPS/Galileo/Glonass/Beidou) SoC with a 0.25mm2 radio in 40nm CMOS," ISSCC Dig. Tech. Papers, pp. 334-335, 2013.

[5] C. H. Wu et al., "A GPS/Galileo SoC with adaptive in-band blocker cancellation in 65nm CMOS," ISSCC Dig. Tech. Papers, pp. 462-464, 2013.

[6] H. Moon et al., "A 23mW fully integrated GPS receiver with robust interferer rejection in 65nm CMOS," ISSCC Dig. Tech. Papers, pp. 68-69, 2010.

[7] K. Cheng et al, "A 7.2mW quadrature GPS receiver in 0.13µm CMOS," ISSCC Dig. Tech. Papers, pp. 422-423, 2009

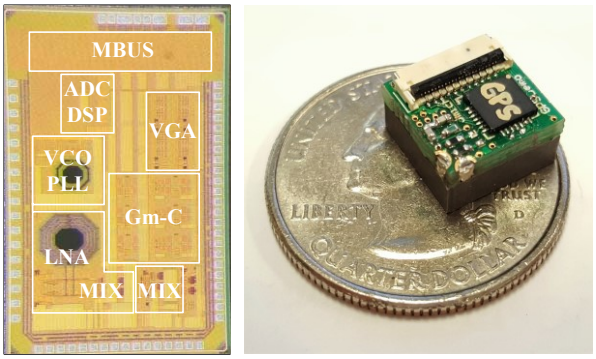

Fig. 9. (a) Chip micrography (b) the proposed GPS logger

TABLE I. Measurement Summary and Performance Comparison

	This work	CICC 13 [2]	CICC 13 [3]	ISSCC 13 [4]	ISSCC 11 [5]	ISSCC 10 [6]	ISSCC 09 [7]
Application	GPS Logger	GPS receiver	GPS receiver	GPS receiver	GPS receiver	GPS receiver	GPS receiver
Captured time	10ms	Contiguous	Contiguous	Contiguous	Contiguous	Contiguous	Contiguous
System	GPS L1	L1/Compass /Galileo/ GLONASS	GPS L1	GNSS	L1/Galileo	GPS L1	GPS L1
RX NF (dB)	2.2	2.2	2.4	2.1	2.0	2.3	6.5
RF-IF Gain (dB)	72	64	>100	-	-	42	42.5
LO Phase noise @ 1MHz offset (dBc/Hz)	-115.6	-118	-115.8	-94	-118	-114	-110
1dB Gain de-sense @1710MHz blocker (dBm)	-6.1	-	-	-18	-	-15	-
System Integration	Complete GPS w/ Antenna	GPS AFE	GPS AFE	GPS AFE	GPS AFE	GPS AFE	GPS AFE
Power (mW)	12.5 (System)	31	41.4	20	18	23	7.2
AFE Area (mm^2)	3.52	10.5	1.2	0.25	1.4	2.5	3.05
Technology	65nm CMOS	65nm CMOS	55nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	130nm CMOS