A 152μW -99dBm BPSK/16-QAM OFDM Receiver for LPWAN Applications

Avish Kosari, Milad Moosavifar, David D. Wentzloff
University of Michigan, Ann Arbor, USA

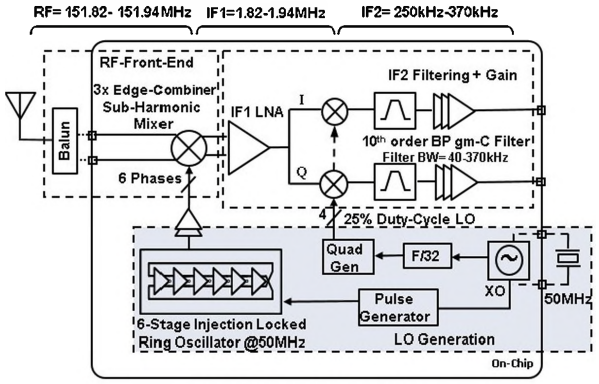
***Abstract*—This paper presents a 152μW BPSK/16-QAM OFDM receiver operating in the 151MHz Multi-Use Radio Service (MURS) frequency band for low power and long-range IoT applications. Sub-harmonic passive mixers and an injection locked ring oscillator are used, together with a dual-IF architecture for power efficiency and blocker rejection. As a solution for LPWAN applications, the receiver is designed to operate in two modes of single-carrier and multi-carrier transmission schemes, and is implemented in a 40nm CMOS process consuming 152μW of power while achieving a sensitivity of -99dBm for BPSK modulation at 5kb/s and -77dBm for 16-QAM OFDM modulation at 384kb/s. Under only 0.9V of supply, it achieves a phase noise of -128dBc/Hz at 1MHz offset, a blocker rejection of 63dB, and is fully integrated except for the reference crystal and the balun.**

***Index Terms*— Injection locking, IoT, long-range, low power radios, LPWAN, MURS band, sub-harmonic mixing.**

I. Introduction

The rapid growth of Internet of Things (IoT) applications requiring long-range data transmission is leading to the prosperous development in long distance wireless communication systems. Recently, different standards are being proposed in sub-GHz bands which target narrowband, low data-rates, and long-range connectivity for low-power IoT applications [1].

The FCC compliant Multi-Use Radio Service (MURS) band at 151-154MHz, exhibits lower path-loss and building penetration loss compared to other higher frequency bands used for low-power wide area network (LPWAN) applications. To this end, recently a low-power MURS band transmitter was developed addressing the long-range transmission requirements of LPWAN [2]. In this work, we present a 152μW MURS band receiver addressing the low active power, high sensitivity, and interference rejection challenges and requirements of LPWAN radios. The BPSK/16QAM OFDM receiver (RX) is data rate agile and suitable for remote IoT connectivity in multipath rich environments. The RX achieves a sensitivity of -99dBm at 5kb/s, capable of 50km line-of-sight communication. This is enabled by a power efficient RX architecture (Fig. 1) and several low-power design techniques, including a dual intermediate frequency (IF) RX architecture using passive multipliers, an edge combiner sub-harmonic mixer first architecture which enables the operation of the frequency synthesizer at a much lower frequency, injection locked



MURS Long-range Transmission

Freq.	Licensed	Modulation	Data rate	Range	Sensitivity
151 MHz	NO	16QAM OFDM/ BPSK	5-384 kb/s	LOS: 50 km	-77/ -99dBm

Fig. 1. Block Diagram of the Receiver.

local oscillators (LOs) which enable more energy efficient frequency generation compared to PLLs, and efficiently distributing the gain and noise performance requirements in the RF and IF blocks. The RX achieves a -128dBc/Hz phase noise (PN) at 1MHz offset for the LO and realizes a blocking rejection of 48dB and 63dB at 2MHz and 10MHz offsets, respectively.

II. System Architecture

The RX operates in two modes of single-carrier and multi-carrier transmission and is designed with the goal of achieving a similar coverage range to LPWAN technologies at a much lower power consumption. The MURS band single-carrier transmission scheme is based on 5kb/s BPSK modulation with 10kHz channel bandwidth (BW), and 60kHz channel spacing. Based on our link budget analysis, for the RX sensitivity of -99dBm and an uplink power of 10dBm, we can achieve a communication range of 50km with a path loss exponent of 2. For higher data-rate applications in denser environments, an OFDM modulated multi-carrier transmission scheme is utilized, which uses 16-QAM on 16 subcarriers with 10kHz subcarrier spacing. The multicarrier modulation symbols have a symbol duration of 125μs with a data rate of 384kb/s.

To achieve the low power consumption requirements of IoT transceivers along with the specifications for the proposed transmission scheme, a mixer-first injection locked dual IF RX architecture is employed, as shown in Fig. 1. Achieving maximum sensitivity at low current levels is a major challenge. This is enabled by two major

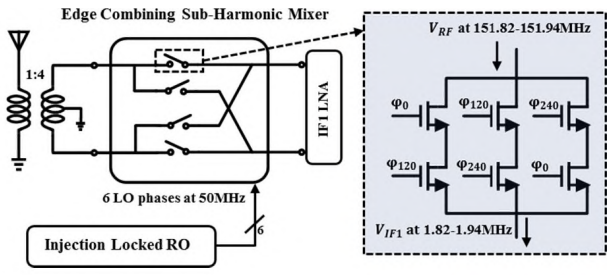


Fig. 2. RX RF front-end.

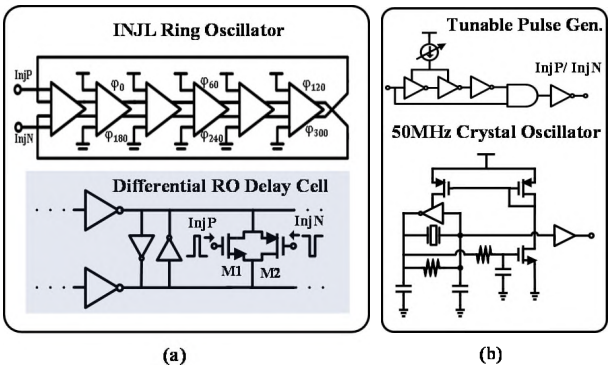


Fig. 3. Injection locked LO generation blocks (a) 6-stage RO and RO delay cell, (b) Pulse generator and 50 MHz XO.

considerations in the system-level design of the RX architecture. 1) The dual IF, sub-harmonic mixer-first architecture is chosen in order to transfer the high dynamic range and hence gain requirements of the RX to the baseband blocks as well as shifting the dual I/Q paths to the lower IF frequency where the power consumption is minimized. In addition, due to the very low IF in the second IF stage (250–370 kHz), the dynamic range and complexity of the required analog to digital converter (ADC) is highly relaxed. 2) The LO frequency generation, which is often the most power hungry block in a RX, is implemented by an injection locked frequency synthesizer at 50MHz, and therefore down-conversion is performed by a 3x sub-harmonic edge-combiner passive mixer. This also enables us to achieve the required PN at a much reduced power.

As shown in Fig. 1, the edge combiner at the input of the receiver is driven by three-phase differential LOs from the injection-locked ring oscillator (ILRO) and is followed by a low-noise amplifier (LNA) at the first IF frequency (IF1), 1.82–1.94MHz, providing 25dB of gain in the first down-conversion step. This is loaded by a quadrature passive mixer driven by 25% duty cycled LOs that are directly driven from the divide-by-32 divider from the on-chip crystal oscillator operating at 50MHz. The second mixers are then followed by very low IF (IF2) 10th order bandpass filters providing 20–54 dB of gain and a tunable bandwidth (BW) of 40–370 kHz. All the blocks are AC coupled to reject DC off-sets.

III. Design Implementation

A. RF Front-End

Fig. 2 represents the RF front-end of the receiver. We have used an on-chip differential double balanced edge-combining sub-harmonic mixer at the input of the RX to save power and reject LO feedthrough due to the presence of random mismatches in the LO phases in the IF signal. An off-chip balun is used for impedance matching to the 50Ω source and single to differential conversion. The six differential three-phase LO signals driving the edge-combiner are fed by the ILRO operating at 50MHz and are phase shifted by 120°. As shown in Fig. 2, the voltage mode edge-combiner is realized by NMOS transistor switches to perform an AND operation on the LO waveforms in each branch and an OR operation to select one of the non-overlapping down-converted signals in each of the three main branches. Overall, the network of 24 NMOS switches, resembles a passive double balanced mixer comprising 4 combined switches operating at 3xLO frequency or 150MHz. The effect of the systematic phase error of injection locking on the output of the sub-harmonic mixer is carefully simulated and discussed in the next section.

B. Injection-Locked Frequency Synthesizer

As shown in Fig. 3, the ILRO at 50MHz is implemented by a six stage differential ring oscillator directly locked to an on-chip reference crystal oscillator [Fig. 3(a)], providing the six output phases from three differential outputs. The schematic of the crystal oscillator (XO) is shown in Fig. 3(b), where a feedback path is used to starve the primary amplifier used with the off-chip crystal, and has a measured power consumption of 29μW. The tunable pulse generator shown in Fig. 3(b) is implemented by an AND operation on the reference signal and tunable delayed versions of the reference. It outputs programmable pulse width signals, Inj_P and Inj_N, to tune the locking range and ensure that the pulse width of the injected signals is smaller than half of the crystal oscillator period. The injection differential pulses drive M_1 and M_2 transistors and short the differential output of the RO [Fig. 3(a)]. Even though the reference pulse is only injected in the first stage of the RO, all the stages are identical to increase matching. Since the injection often only happens in the first stage of the RO, ILRO systems have a systematic phase mismatch between the stages which leads to spurs occurring at LO frequency in the frequency multiplied signals in the IF stage of the receiver. The phase error between the adjacent stages in the ILRO is proportional to the frequency difference between the free running RO (f_{RO}) and the injected signal (f_{inj}) and can be written as: $\theta_{error} = \frac{\pi}{3}(f_{RO} - f_{inj})/f_{RO}$. This systematic phase error was simulated with the edge combiner mixer to ensure the LO feedthrough is small enough and can be filtered by the baseband filters. This eliminates the use of multiphase injection locking techniques and therefore,

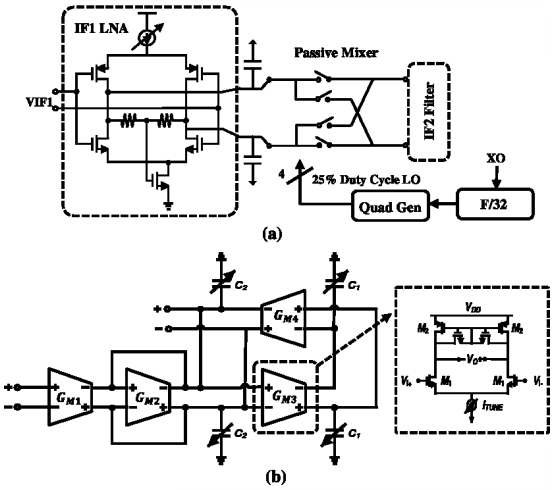


Fig 4. (a) IF1 stage and schematic of IF1 LNA, (b) Block diagram of a single stage of IF2 10th order filter.

saves power. An 8 bit current DAC is used to tune the RO frequency and minimize the effect of the phase mismatches on the receiver performance.

C. *First Intermediate frequency (IF1) stage*

As shown in Fig. 4(a), an inverter based topology is used for the IF1 LNA for gain and noise efficiency. Common mode feedback is provided by both the pseudo resistors and the bottom NMOS transistor, guaranteeing the output common mode stay at half V_{DD}. Since the input impedance of the LNA directly affects the receiver's input impedance and therefore noise performance through the passive mixers, the LNA's input devices as well as the tail currents are adjusted to match the desired noise level. The outputs of the LNA are directly loaded by a quadrature passive mixer driven by 25% duty cycled LO signals. The LO signals, are generated by a divide-by-32 divider driven by the XO. This further down-converts the signal for an optimum power consumption as well as a good blocker rejection performance.

D. *Second Intermediate frequency (IF2) Stage*

In order to enable the targeted specifications for MURS communication, a 10th-Order Chebyshev-I bandpass g_m-C filter is designed. The filter is implemented using five cascaded biquad stages. Each of the biquad stages provide a 1st-order high-pass and low-pass response with programmable pole frequency, quality factor, and gain, as shown in Fig. 4(b). In order to achieve a broad tuning range, both g_m and capacitors of each stage are designed to be tunable. The g_m variation of the G_m-cells, often causes a significant change in DC operating points. Therefore, in order to prevent DC operating point variations, and maximize the tuning range simultaneously, self-biased differential G_m-cells are used in the biquad stages. The programmability feature enables the filter to create a Chebyshev response or Bessel with different band widths,

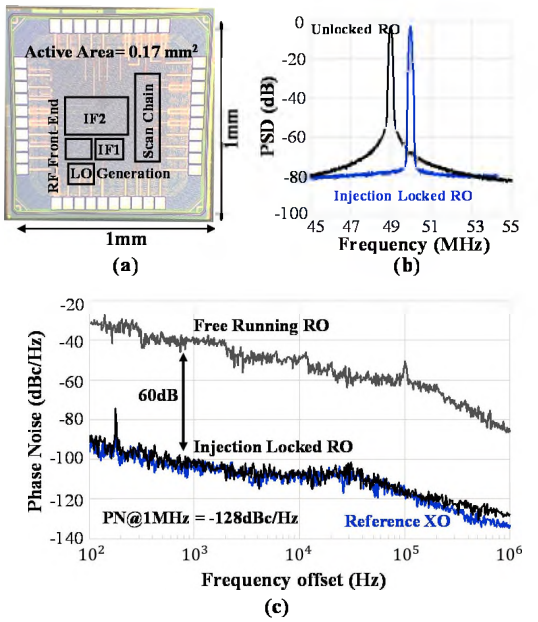


Fig 5. (a) Die micrograph of the RX, (b) Unlocked and locked RO PSD, (c) ILRO, XO and unlocked RO PN.

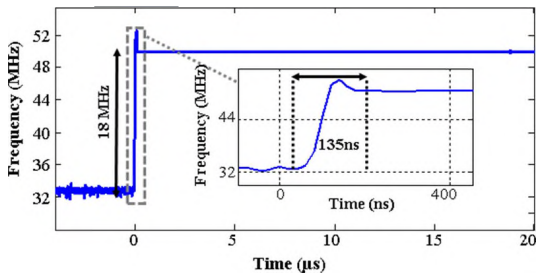


Fig 6. Frequency transient showing the settling time for ILRO.

making the receiver reconfigurable for different modes of operation. The filter has two modes of operation, one providing higher measured gain of 20–54dB and a BW of 40kHz for BPSK operation mode. The other mode provides a lower gain of 20–32 dB, but higher BW from 170–370 kHz for OFDM mode of operation with higher data rates. The devices in the IF2 stages are optimally dimensioned to reduce the flicker noise. The differential filtered IF2 signals are fed to an off-chip 5MS/s ADC for digitization and baseband processing.

IV. Measurements

The RX was fabricated in a 40nm CMOS process and packaged in a 6×6mm QFN40 package. The RX core blocks, not including the I/O pads, occupy an area of 0.17mm^2. Fig. 5(a) shows the die photo of the receiver. The power spectral density of the locked and unlocked RO and the phase noise of the free-running RO, XO and ILRO are shown in Fig. 5(b) and 5(c), respectively. The measured PN at 1MHz offset is -128dBc/Hz that minimizes reciprocal mixing of LO PN. An off-chip SMD crystal (AMB8) is used with the on-chip XO. The power dissipation of the XO

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART NARROWBAND RECEIVERS

Reference	This Work		[3] ISSCC17	[4] RFIC15	[5] ISSCC16
Technology (nm)	40		65	130	180
Architecture	Dual-IF w/ Sub-Harmonic Mixer and ILRO		Low-IF	Low-IF	Low-IF
Carrier Freq. (MHz)	151.82-151.94		850-920	433	160/960
Supply Voltage (V)	0.9		3.3	1.2/0.5	2.2/3.6
Modulation	BPSK	16QAM OFDM	UNB DBPSK	2-FSK	2-GFSK
Data-rate (kb/s)	5	384	0.100	1	2.4/37.5
Active Power (μW)	152		14500	378	57000
Sensitivity (dBm)	-99*	-77*	-136	-102.5	-122
Blocking, 3dBsens.loss (dB)	48 @2MHz/ 63 @10MHz		90 @10MHz	14 @ 0.2MHz	93 @ 2MHz
Oscillator PN (dBc/Hz)	-128 @ 1MHz		-106 @ 1MHz	N/A	-138 @ 2MHz

* Sensitivity is reported at BER of 10^{-3}

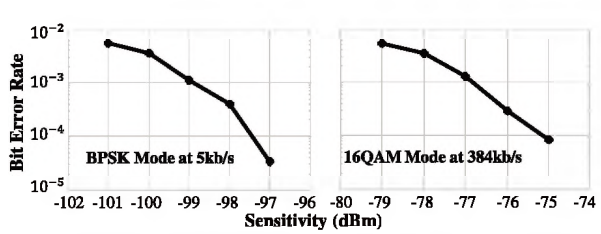


Fig. 7. BER vs. sensitivity for BPSK and 16QAM OFDM modes

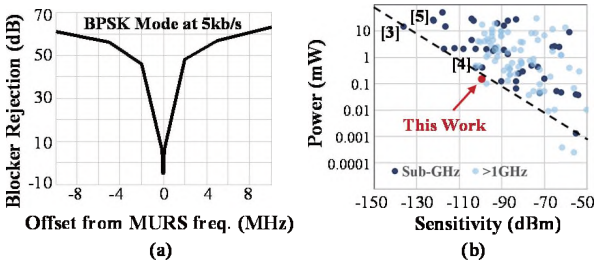


Fig. 8. (a) Blocker rejection for the BPSK mode. (b) Low-power radio survey from 2005 to present. The data of the radio survey is from top conferences and commercial RX chips [6].

and RO (and RO buffers) is 29μW and 21μW, respectively, and the pulse generator and LO dividers consume 17μW total. The maximum locking range for the ILRO is 18MHz and Fig. 6 shows the ILRO lock time of shorter than 135ns, which is measured by enabling the injection signal when the free running RO is operating at 17.6MHz offset from f_{inj}.

The measured sensitivity at BER of 10^{-3} is -99dBm for the BPSK mode at 5kb/s and is -77dBm for the 16-QAM OFDM mode at 384kb/s. Fig. 7 presents the BER performance vs. the input RF power for the two modes of operation. The blocker rejection ratio for out of band blockers is shown in Fig. 8(a). The blocker rejection ratio for 2MHz and 10MHz offsets are 48dB and 63dB, respectively, for 3dB sensitivity loss. The receiver consumes 152μW from a 0.9V power supply, and the IF1 LNA and IF2 filters consume 59μW and 26μW, respectively. The overall gain of the receiver is 79dB at the maximum gain mode, with 25dB in the RF front-end and IF1 stages and 54dB in the IF2 stage. Table I summarizes the measured performance of the receiver and presents a comparison between this work and other state-of-the-art narrow-band receivers. According to the low power radio survey shown in Fig. 8(b) [6], this receiver sits below the power vs. sensitivity trend-line, demonstrating the best reported power amongst sub-GHz receivers with sensitivity values below -90dBm.

V. CONCLUSION

A low power MURS band receiver with an efficient system-level design and several low power design techniques is proposed for LPWAN applications. The receiver utilizes an edge-combiner mixer first with two step down-conversion architecture, and uses an injection locked ring oscillator for LO. It achieves -99dBm sensitivity with 152μW of power at 5kb/s and a 63dB blocker rejection at 10MHz offset. The ILRO, which is locked to a stable 50MHz crystal reference, achieves a PN of -128dBc/Hz at 1MHz offset. In terms of sensitivity versus power consumption tradeoff, this radio shows the lowest power consumption compared to the state-of-the-art receivers with better than -90dBm sensitivity values.

ACKNOWLEDGMENT

This work is supported by NSF under award number CNS 1422175.

REFERENCES

[1] M. Centenaro *et al.*, "Long-range communications in unlicensed bands: the rising stars in the IoT and smart city scenarios," in *IEEE Wireless Commun.*, vol. 23, no. 5, pp. 60-67, October 2016.

[2] A. Kosari *et al.*, "A MURS Band Digital Quadrature Transmitter with Class-B I/Q Cell Sharing for Long Range IoT Applications," in *IEEE Trans. on Circuits and Systems II:Express Briefs*, Jan. 2018.

[3] D. Lachartre *et al.*, "A TCXO-less 100Hz-minimum-bandwidth transceiver for ultra-narrow-band sub-GHz IoT cellular networks," *IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, 2017.

[4] N. E. Roberts *et al.*, "A 380μW Rx, 2.6mW Tx 433MHz FSK transceiver with a 102dB link budget and bit-level duty cycling," *IEEE Radio Frequency Integrated Circuits Symposium*, 2015.

[5] N. Kearney *et al.*, "26.4 A 160-to-960MHz ETSI class-1-compliant IoE transceiver with 100dB blocker rejection, 70dB ACR and 800pA standby current," *IEEE Int. Solid-State Circuits Conf.*, 2016.

[6] David D. Wentzloff, "Low Power Radio Survey," [Online]. www.eecs.umich.edu/wics/low_power_radio_survey.html