A 60-GHz Integrated Slot Loop Antenna in 0.13-µm BiCMOS Technology

Hyeongseok Kim and David D. Wentzloff
Department of Electrical Engineering
University of Michigan
Ann Arbor, MI, USA
hskims@umich.edu

***Abstract*—This paper presents a rectangular slot loop antenna integrated in a standard 0.13-µm BiCMOS technology. By using the slot loop antenna, it can easily satisfy the metal density rules without dummy metal fill and can be integrated with other circuitry. The total area of the antenna including the ground plane is 0.883 mm^2 and the loop antenna only occupies 0.24 mm^2. The antenna resonates at 59.93 GHz and the bandwidth is 5.44 GHz from 57.82 GHz to 63.26 GHz. The simulated total gain is 2.69 dBi while the efficiency at 60GHz is 86%. The radiation efficiency is better than 74% over the band.**

I. Introduction

There is increasing interest in integrated antennas using the unlicensed 60-GHz band for wireless personal area networks (WPANs) thanks to its wide bandwidth, high capacity, and interference resistance. The mm-wave bands are particularly beneficial for mm-scale wireless sensors used in short-range IoT applications. These devices integrate all components of a sensor node into a cubic-mm volume, including the antenna. Antennas designed for the more typical <10GHz ISM bands at mm-scale often result in <1% radiation efficiency. Therefore, the 60GHz band tends to be a better match for the size of these devices.

For mm-scale wireless sensor nodes, having the antenna integrated in a CMOS process along with the RF circuits enables compact, low-cost, and short-range wireless communication. However, an on-chip antenna co-designed with the circuitry must conform to the CMOS design rules, in particular meeting metal density rules. This can be problematic for many antenna designs that use large blocks of metal, such as a patch, or large open areas without metal, such as a loop. For example, if the antenna is designed either under or over density, dummy metal fill or metal slots must be added in and around the antenna, which inevitably degrades antenna performance. This work presents a slot loop antenna which can easily satisfy the density rules without requiring dummy metal fill, which can also be integrated with other active circuits underneath the antenna.

II. Ractangular Slot Loop Antnenna Design

Fig. 1(a) shows the geometry of a slot loop antenna using the layer profile of 0.13-µm BiCMOS technology. The loop antenna is designed on the two top metals (M7 and M6) in a dimension of 0.883 mm^2 including the ground plane. The size of the loop antenna is only 490 µm x 490 µm, which corresponds to 0.098 λ_o at each side (Fig. 2). The two layers are connected using an array of vias for better reliability and for reducing the conductor loss (Fig. 1(b)). The center frequency of the antenna is mainly determined by the dimension and gap of the loop. The tolerance of the conductor is one of the limitations impacting variation of the center frequency. By connecting the top metal to the M6 layer, which has better tolerance, the frequency variation can be reduced.

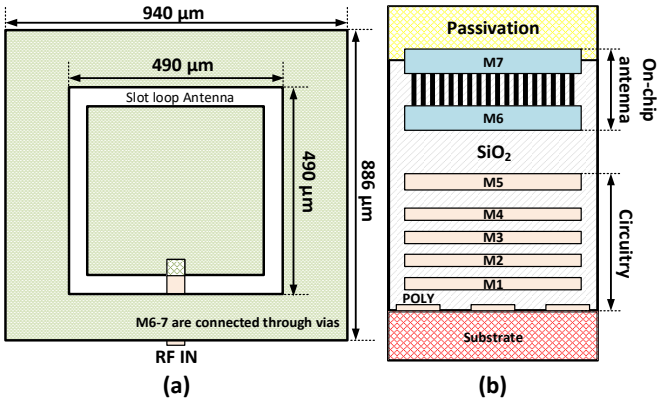

Fig. 1. (a) The designed 60-GHz on-chip slot loop antenna (b) cross section view in a standard 0.13-µm BiCMOS process

This antenna is specifically designed for integration with the RF front-end and baseband circuitry. The baseband circuitry operating at a much lower frequency can be placed anywhere underneath the antenna except the slot loop area. The RF input of the antenna is directly connected to the power amplifier, and the input impedance is carefully designed to match with it.

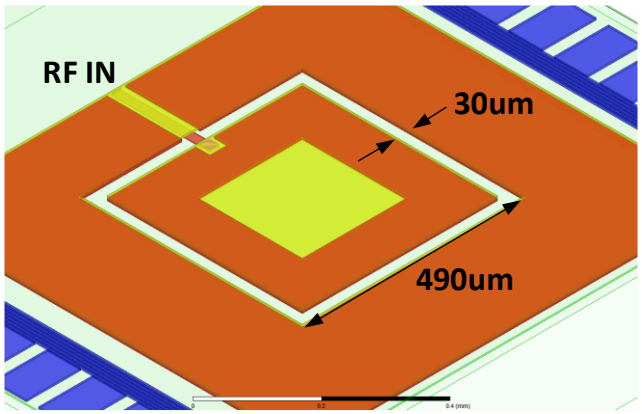

Fig. 2. A 3-D EM simulation model of the antenna

III. Results and Discussions

Fig. 3 shows the input impedance of the slot loop antenna. The design is simulated and optimized in ANSYS Electronics Desktop. The antenna resonates at 59.93 GHz and the bandwidth (at VSWR 3.0) is 5.44 GHz from 57.82 GHz to 63.26 GHz. At the resonance frequency, the input impedance matches to a relatively high impedance of ~ 300 ohms, which is designed intentionally to match with an integrated power amplifier.

Fig. 4 represents the radiation pattern at 57GHz and 60 GHz. The radiation pattern of the slot loop antenna is identical in shape to that of a wire loop except that the E- and H-fields are interchanged. The simulated peak gain at 60 GHz is 2.69 dBi, and the efficiency is 86%. In the 60 GHz band, 57-64 GHz, the radiation efficiency is better than 74% as shown in Fig. 5. This omni-directional radiation pattern and its high efficiency over the band make it suitable for the application of short-range communication systems.

Prior published integrated antennas are mostly designed as wire radiators, but their efficiency and bandwidth suffer due to the design limitations of standard CMOS technology, such as thin metal layers and, metal density rules, and coupling with other routes and circuitry [1]-[5]. By using the slot type antenna, the slot mainly radiates an electromagnetic wave and is not impacted by design rules and coupling issues. The outer dimensions of the loop and the gap are controllable to satisfy the density rule, which eliminates unwanted metal filling dummy. However, because the slot radiates, the actives devices and routes need to be carefully designed near the slot area so that it doesn't degrade the radiation performance. Table II summarizes the performance of the antenna with comparison to the state of the art.

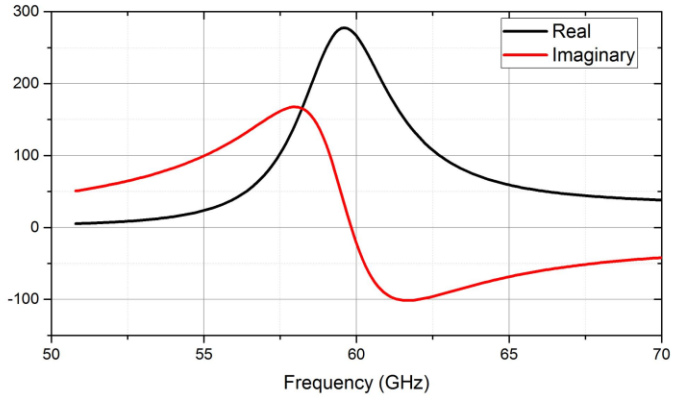

Fig. 3. Input impedance of the slot loop antenna

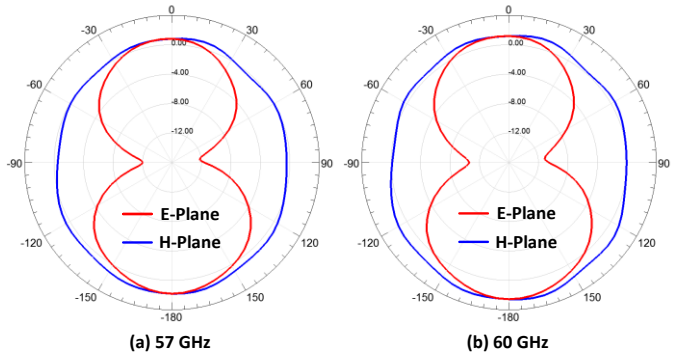

Fig. 4. Radiation patterns (a) at 57 GHz (b) at 60 GHz

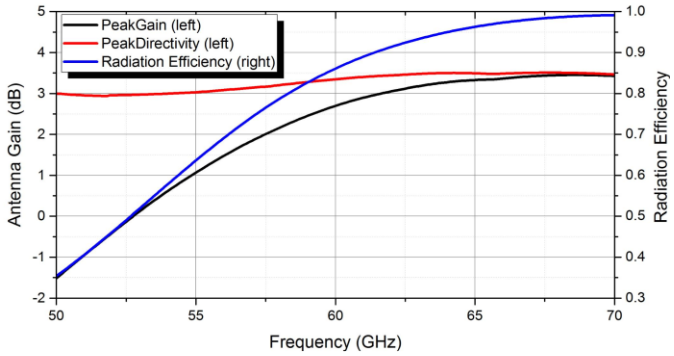

Fig. 5. Simulated radiation performances; Peak directivity, peak gain and radiation efficiency

IV. Conclusion

A slot loop on-chip antenna in an area of 0.883 mm^2 is implemented using a standard 0.13-µm BiCMOS process. By using a slot as the radiator, the antenna can easily satisfy the density rules without requiring dummy metal fill, which can also be integrated with other active circuits underneath the antenna. The antenna is beneficial for mm-scale wireless sensors used in short-range IoT applications due to its wide bandwidth, high efficiency, and small area.

References

[1] P. C. Kuo, S. S. Hsu, C. C. Lin, C. Y. Hsu and H. R. Chuang, "A 60-GHz Millimeter-Wave Triangular Monopole Antenna Fabricated Using 0.18-m m CMOS Technology," *International Conference on Innovative Computing Information and Control*, pp. 237-237, 2008.

[2] P. J. Guo and H. R. Chuang, "A 60-GHz millimeter-wave CMOS RFIC-on-chip meander-line planar inverted-F antenna for WPAN applications," *IEEE Antennas and Propagation Society International Symposium*, pp. 1-4, 2008.

[3] S. S. Hsu, K. C. Wei, C. Y. Hsu, and R. C. Huey, "A 60-GHz millimeter-wave CPW-fed yagi antenna fabricated by using 0.18 um CMOS technology," in *IEEE Electron Device Lett*, vol. 29, no. 6, pp. 625–627, Jun. 2008.

[4] K. Huang and D. D. Wentzloff, "60 GHz on-chip patch antenna integrated in a 0.13-µm CMOS technology," *IEEE International Conference on Ultra-Wideband*, pp. 1-4, 2010.

[5] X. Y. Bao, Y. X. Guo and Y. Z. Xiong, "60-GHz AMC-Based Circularly Polarized On-Chip Antenna Using Standard 0.18-µm CMOS Technology," in *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 5, pp. 2234-2241, 2012.

TABLE II
SUMMARY AND COMPARISON OF THE STATE-OF-THE-ART

	This Work	[1]	[2]	[3]	[4]	[5]
Frequency (GHz)	60	60	60	60	60	65
Type	Slot Loop	Mono-pole	Invert-F	Yagi	Patch	Loop w/ AMC
Gain (dBi)	2.8	-9.4	-15.7	-10.6	-3.32	-4.4
Area (mm^2)	0.883 (0.24)	0.81	0.57	1.05	1.93	3.24
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS