A 486 µW All-Digital Bluetooth Low Energy Transmitter with Ring Oscillator Based ADPLL for IoT applications

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***Abstract*—this paper presents an all-digital Ring Oscillator (RO) based Bluetooth Low-Energy (BLE) transmitter (TX) for ultra-low-power radios in short range IoT applications. It employs a wideband ADPLL featuring an $f_{RF}/4$ RO, with an embedded 5-bit TDC. A 4X frequency edge combiner is used to generate the 2.4GHz signal. This helps reduce the power consumption and enhance its phase noise performance at the same time. A switch-capacitor PA is optimized for high efficiency in low power mode. The TX is designed at the phase noise limit for BLE and in low power mode it consumes 486 µW while configured as a non-connectable advertiser, which has been validated by wirelessly communicating beacon messages to a mobile phone.**

***Index Terms*— Bluetooth Low-Energy (BLE), Ultra-low-power radios, IoT, Transmitter, Ring Oscillator, ADPLL, Phase Noise, Switch-capacitor PA.**

I. Introduction

With the increasing demand for inter-connected IoT devices, ultra-low-power (ULP) radios, especially those with standard compatibilities, are dramatically needed in wireless sensors for a wide range of applications. Bluetooth Low-Energy (BLE) is widely used as the wireless interface for ULP IoT devices, yet due to phase noise (PN) limitations and the complexity of the LO design in a BLE transceiver, state-of-the-art BLE radios consume several milliwatts [1-4], limiting battery lifetime in such applications. Thus, in many short range and energy-harvesting applications, such as wearable sensor nodes and implantable medical devices, current BLE radios are still too high power to be adopted in a large scale. Asymmetric communications are normally used in such systems, but they always suffer from interference and bulky base stations [5]. Thus, by making an asymmetric BLE network in its advertising channel will not only reduce the power consumption of BLE transmitters (TX) in the sensor node to its limit, but could also help resolve the interference and base station issues in ULP wireless sensor systems.

All reported BLE TX use LC oscillators (LCVCO) due to their inherent advantage in phase noise over ring oscillators (RO). However, their power consumption is strictly limited by the quality factor of the integrated LC tank. Furthermore, the PN of LCVCOs at the minimum power point is still 30-40dB better than what is required for BLE based on BER alone. Open loop LCVCOs has been adopted in recent BLE designs to reduce power, but these are still limited by the intrinsic high power of LCVCOs. ROs, on the other hand, have not been demonstrated in BLE designs because of their typically worse PN performance. However, they have the advantage of being able to trade off power for PN and they can further benefit from scaling. This paper explores the PN and PLL trade-offs as they relate to the BLE specs, which results in a PN limit achievable by a RO-based PLL. An all-digital RO-based BLE transmitter, as shown in Fig. 1, is presented that meets this PN limit with a ULP wideband ADPLL and an efficiency-optimized SCDPA. A 32-phase $f_{RF}/4$ RO, that not only forms a 5-bit embedded TDC but also serves as a 4X frequency edge combiner, is adopted to reduce the PLL power and improve its PN performance. The BLE TX consumes 486 µW while configured as a non-connectable advertiser, which is desirable for short-range TX-only beacon devices in an asymmetric BLE network. Its functionality has been validated by wirelessly communicating beacon messages to a mobile phone.

This paper is organized as follows: section II talks about the analysis of PN limit for BLE. Section III discusses the details of design considerations in system level and circuit level to achieve low power and the required noise performance. Section IV discusses the measurement results and the comparison to the state-of-the-art. Finally, section V draws the conclusion.

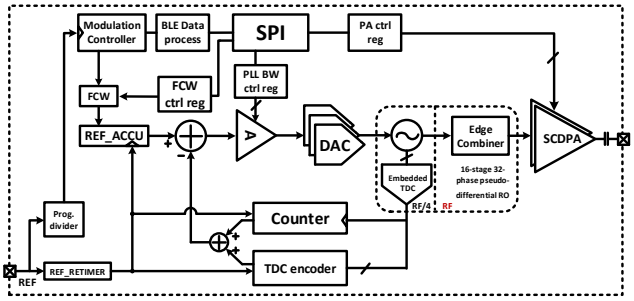

Fig. 1. Simplified block diagram of the proposed all-digital BLE TX

II. Phase Noise Analysis for BLE

Based on the relationship between PN, period jitter and instantaneous frequency variation [6-7], the standard deviation of the frequency variation, σ_f, can be calculated by integrating the PN falling into the RX filter BW:

$$\sigma_f = f_0^2\sigma_\tau = \sqrt{\int_0^{BW} 2L(f)f^2 sinc^2\left(\frac{\pi f}{f_0}\right) df} \quad (1)$$

where $L(f)$ is PN at certain offset, σ_f, σ_τ represent the standard deviation of frequency variation and jitter, and f_0 is the center frequency. Applying this to practical radio systems, if the LO is an open loop oscillator, and ignore flicker noise effect, the resulting frequency variation can be simplified as:

$$\sigma_f = \sqrt{2BW_{rx}L(f)f^2} \quad (2)$$

As for PLL regulated cases, with different PLL BW, the relations can be simplified as (3) and (4) assuming a constant in-band phase noise response:

$$\sigma_f = f_0^2\sqrt{\left\{\begin{array}{c}\frac{1}{2\pi^3 f_0}\left(\frac{2\pi BW_{pll}}{f_0} - \sin\left(\frac{2\pi BW_{pll}}{f_0}\right)\right) + \\ \frac{2}{f_0^4}(BW_{rx} - BW_{pll})BW_{pll}^2\end{array}\right\} L_{in}} \quad (3)$$

$$\sigma_f = f_0^2\sqrt{\frac{1}{2\pi^3 f_0}\left(\frac{2\pi BW_{rx}}{f_0} - \sin\left(\frac{2\pi BW_{rx}}{f_0}\right)\right) L_{in}} \quad (4)$$

where L_{in} is the in-band PN level. [8] has also found this in an integrating format. Considering this in a high SNR regime since the target communication range is within 1-2 meters, PN is the dominant noise source. So from the analysis above, the BLE spec could be achieved by an ULP RO regulated by a wide band PLL, as shown in Fig. 2.

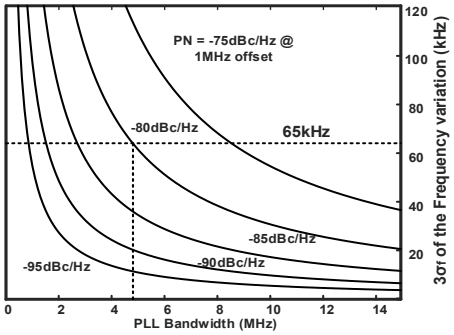

Fig. 2. Simulated PLL bandwidth requirement for different phase noise levels

III. System Level Design and Circuit Details

Fig. 3 shows the top-level block diagram of the proposed design and its major noise sources. To achieve the targeted frequency variation error with the RO, a 5MHz bandwidth ADPLL for aggressive in-band phase noise suppression is implemented. It features a fast settling time and direct reference phase modulation since the PLL BW is much larger than the modulation BW. Several techniques are used to save the PLL power and enhance its in-band PN at the same time. The RO is designed at a frequency of $f_{RF}/4$ and implemented with a 16-stage pseudo-differential architecture with 32 phases directly used as an embedded TDC. Its phases are also used in a windowed edge combiner for 4X frequency multiplication to produce the 2.4GHz RF frequency. The lower frequency RO saves the power of the frequency divider. And it also prevents the noise folding effect from happening when the noisy phases are sub-sampled and folded by the divider in the traditional divider based PLL, thus improving in-band PN performance. At the same time, the high power TDC and its delay normalization circuits are also saved, and the TDC performance can be relaxed by dealing with the same amount of jitter at a lower frequency while maintaining the same resolution. The edge combiner consumes much less power compared to a TDC, and it can maintain the low flicker noise corner from the low frequency RO, which will again, enhance the in-band phase noise [9].

Even though extra deterministic jitter will be introduced because of the mismatches in the different paths of the edge combiner, as shown in Fig. 3, this mismatch is much smaller than the random jitter from the high PN RO. Since this jitter is not correlated with the random jitter, the windowed edge combiner won't affect the overall RF performance. And due to periodical phase shifts, the edge combiner will also introduce spurs at $\pm f_{RF}/4$ off the center frequency with the spur level equal to $20\log(\delta T_0/T_0)$ [10]. In this design, the edge combiner introduced jitter is within 1 ps, thus mismatch introduced spurs are smaller than -50dBc, which are almost negligible compared to PA non-linearity at the output stage.

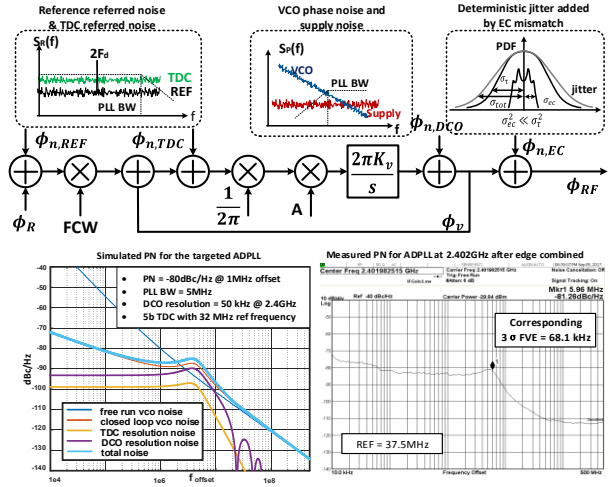

Fig. 3. System-level (top) noise analysis and PLL design & measurement (bottom)

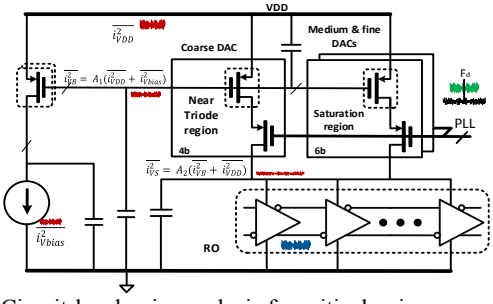

Fig. 4. Circuit-level noise analysis for critical noise sources

Critical noise sources are modelled for the PLL, as shown in Fig. 3. The PLL is designed to achieve a 5MHz

BW with a -85dBc/Hz in-band PN. And the BW is programmable by changing the loop filter gain through an SPI interface, as shown in Fig. 1. Measured results show great agreement with the design. The phase noise performance corresponds to a 68.1 kHz $3\sigma_f$ frequency error, and demonstrates successful BLE communication under the BLE spectrum mask. With this $f_{RF}/4$ RO and edge combiner architecture with its 4X phases embedded TDC, the PLL controller's power consumption is as low as 253 µW in a 40nm technology. Moreover, with the scale of technology, this number could be further improved.

Fig. 4 shows the major noise sources at the transistor level that need to be carefully dealt with. Since the PLL BW is very high for in-band PN suppression and direct reference phase modulation, the decap on the virtual VDD of the RO has to be fairly small to keep the PLL loop stable, thus plenty of noise from the supply and the bias network will pass through. To deal with this, the coarse DAC bank is designed at the edge of the triode region to minimize the noise gain while the medium and fine DAC banks are designed in the saturation region to keep the required tuning linearity while the PLL is locked. Additional large decaps are added to the gate of the DAC cells to filter the accumulated supply and bias noise. The medium and fine current steering DACs are 6b each that covers 70 MHz range with approximately 20 kHz LSB tuning step for the RO and the coarse DAC is 4b and can cover up to 300 MHz.

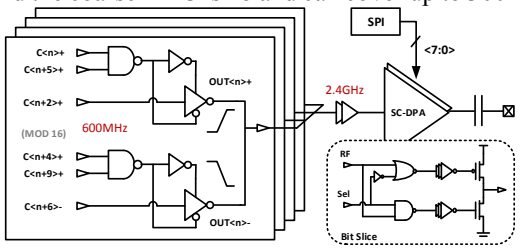

Fig. 5. Schematic for the windowed edge combiner and the switch-capacitor digital PA

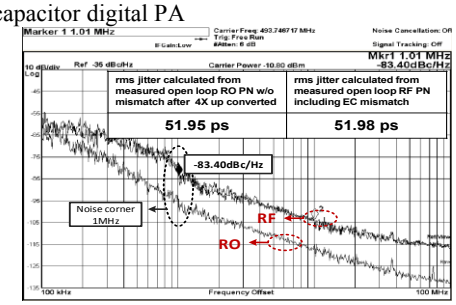

Fig. 6. Measured phase noise of the open loop RO and EC output due to mismatch

Fig. 5 shows the windowed EC and the SCDPA. 24 of the 32 RO phases are used to implement a windowed edge combiner. 6 phases are used for each rising and falling edge to be combined, in which the 2 windows are spaced by 4 RO delays and the window width is 5 delays to ensure all selected phases pass through in different PVT corners. Tristate gates are used to pass the selected phase and buffer the interference from other phases. The measured phase noise for the open loop RO working at 493MHz before and after edge combining is shown in Fig. 6 and it shows that the combined RF output follows the same noise corner as the low frequency RO. The impact of the EC on the integrated PN jitter calculated from the phase noise measurement shown in Fig. 6 is 1.7ps and the resulting spurs are at -49.4dBc from calculation (cannot be directly measured with the PA). Both are insignificant compared to the PLL jitter and PA non-linearity. The low power SC-DPA is thermometer coded with 8-bit slices and is matched and optimized for the highest efficiency for -10dBm operation.

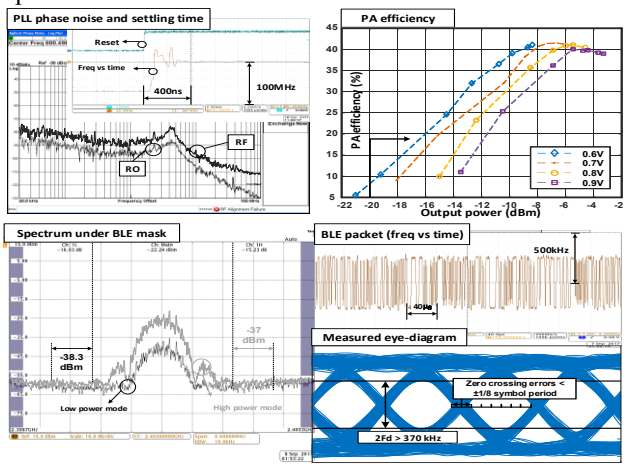

Fig. 7. Measurement results including PLL phase noise and settling time (top left), PA efficiency (top right), output spectrum @ 2.402GHz (bottom left), and captured BLE packets with eye diagram (bottom right)

IV. Measurement Result

Fig. 7 presents the measured PLL and the BLE TX performance. The PLL is locked at 600.5MHz and combined to 2.402GHz, with a BW larger than 5 MHz. With the large BW, the PLL settles within 0.4µs from reset, as shown in the frequency vs time measurement. The measured PA drain efficiencies are also shown. It consumes 107 µW when the output is -19.2 dBm with a 10.8% efficiency using a 0.6V supply. In high power mode, it can deliver -3.3 dBm while consuming 1.2 mW with a 39% efficiency using a 0.9V supply. The maximum efficiency of 41% is achieved at around -10dBm output power. The TX spectrum is also measured while transmitting a repeated BLE packet, which meet the BLE spectrum mask requirement. The measured frequency vs. time for part of the BLE packets are also shown. The eye-diagram is calculated from the captured frequency domain signal. The phase noise from the RO does degrade the eye performance, but as designed, both the symbol timing and frequency error meet the BLE communication limit.

Fig. 8 shows the wireless test setup. Here, the BLE TX is configured to transmit an iBeacon message, which is

picked up by the iBeacon app, and shows the correct packet information. While working at the low power mode with a 37.5MHz off chip reference, the RO with the DAC bias network consumes 126 µW, and the PLL blocks with the edge combiner consumes 253 µW. The all-digital RO based BLE TX consumes a total 486 µW power with an active area of only 0.0166 mm^2 in a 40nm technology, as shown in the die photo. The comparison to the state-of-the-art is shown in Table I.

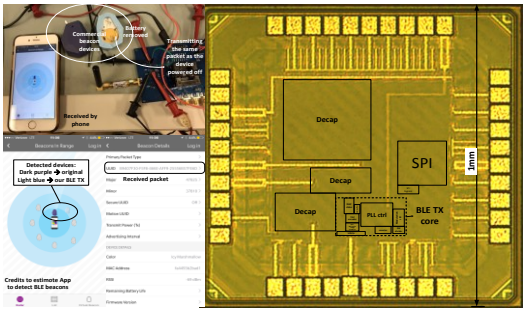

Fig. 8. Wireless test setup and die photo

V. Conclusion

In this work, an all-digital ULP BLE TX with a $f_{RF}/4$ RO based TDC-less ADPLL and 4X edge combiner is presented. Ring Oscillator is proved in theory and demonstrated in circuits to be feasible for BLE TX design with low power. The transmitter consumes 486 µW in its low power mode while talking to a phone and is extremely low cost due to the implementation with RO. Moreover, because of the all-digital nature of this design, it can further benefit from technology scaling, and is suitable for short-range wireless sensor networks in ULP IoT applications.

Acknowledgment

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TABLE I
Comparison with State-of-the-Art BLE Transmitters

	This work		ISSCC15[1]	ISSCC15[2]	ISSCC15[3]	JSSC16[4]	
Technology (nm)	40		40	55	40	28	
Supply voltage (v)	0.6-0.9		1	0.9-3.3	1.1	0.5/1	
PLL REF frequency (MHz)	32-48 (37.5 as tested)		32	16	32	5/40	
PLL settling time (µs)	0.4		15	15	N/A	14	
PLL In-band PN (dBc/Hz)	-85		-90	N/A	N/A	-92/-101	
Max output power (dBm)	-10.6	@0.6V	-2/1	0	0	3	
	-3.3	@0.9V					
Max PA efficiency	41%		25%	30%	<30%	41%	
TX Power consumption	0.49mW	1.55mW	4.2mW	10.1mW	7.7mW	4.4mW	3.8mW*
	@-19dBm	@-3dBm	@-2dBm	@0dBm	@0dBm	@0dBm	@-3dBm
Core Area (mm^2)	0.0166		0.6**	0.6**	0.6**	0.65	

*Estimated from PA efficiency **Estimated from die photo for only TX