



Design Considerations for Next Generation Wireless Power Aware Microsensor Nodes

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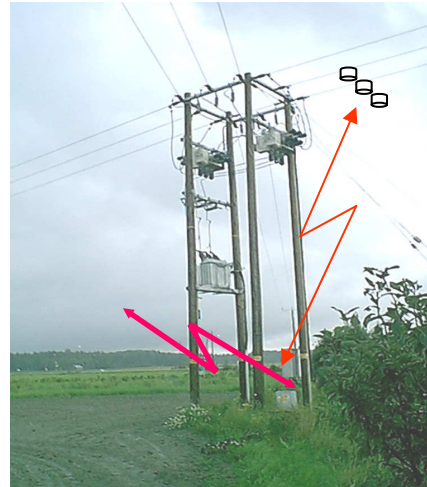




Emerging Microsensor Applications



Industrial Plants and Power Line Monitoring (courtesy ABB)



Operating Room of the Future (courtesy John Gutttag)



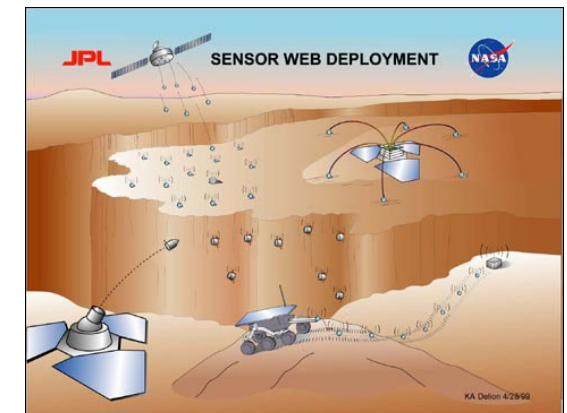
Target Tracking & Detection (Courtesy of ARL)



Location Awareness (Courtesy of Mark Smith, HP)



NASA/JPL sensorwebs





Sensor System Requirements



Predictable Constraints

Application Characteristics	Typical Values
Data Rate	bps to kbps
Spatial Density	0.1-10 nodes/m ²
Transmission Distance	10 – 100m
Extended Lifetime	5 years
Small Size	1 “AA” battery

Application-specific designs provide energy efficient point solutions

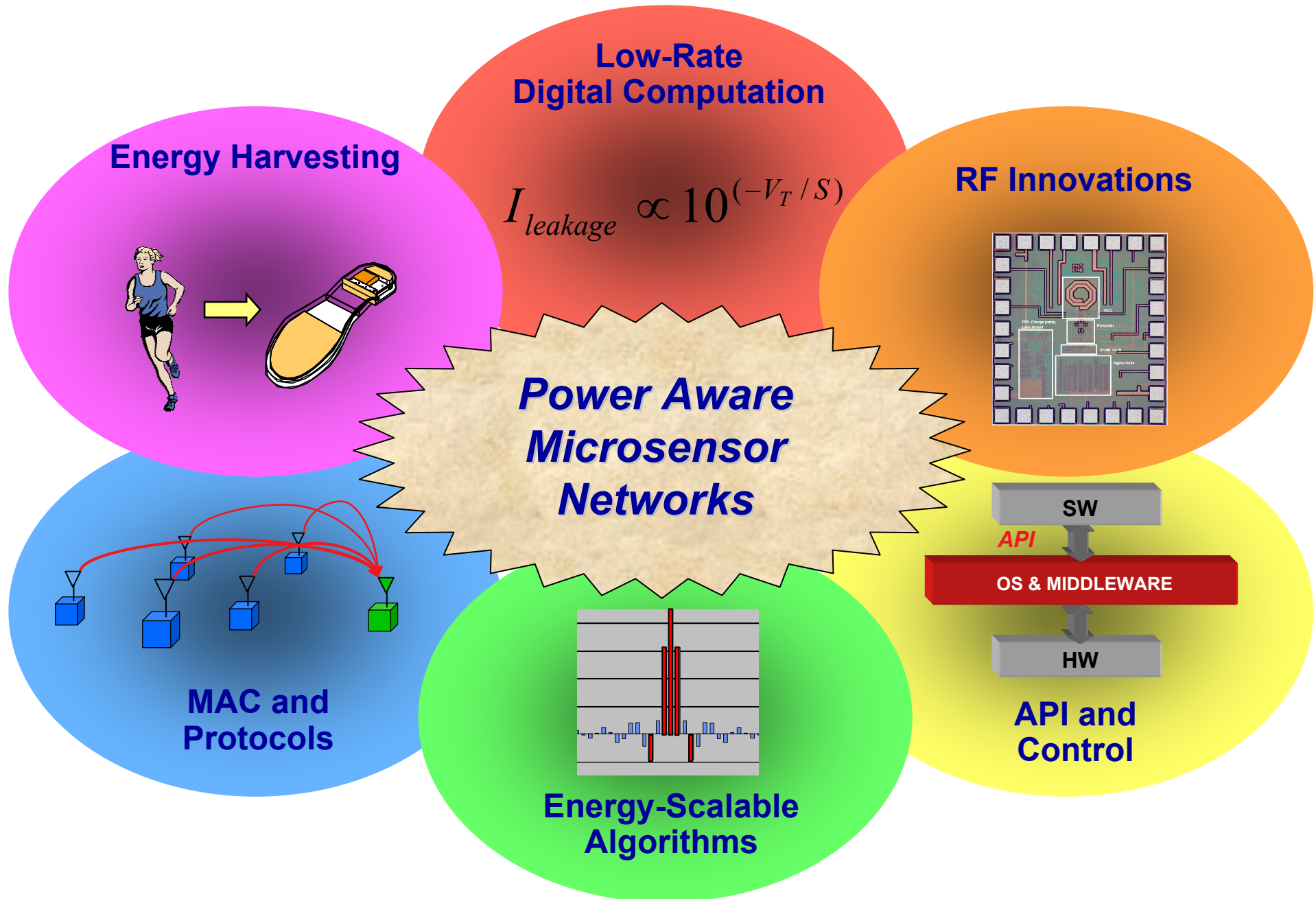
Unpredictable Diversity

- *Network roles:*
relay, sensor, aggregator
- *Environment:*
event and signal statistics
- *User/Application:*
required latency, quality

Power-aware designs adapt energy consumption to operating conditions

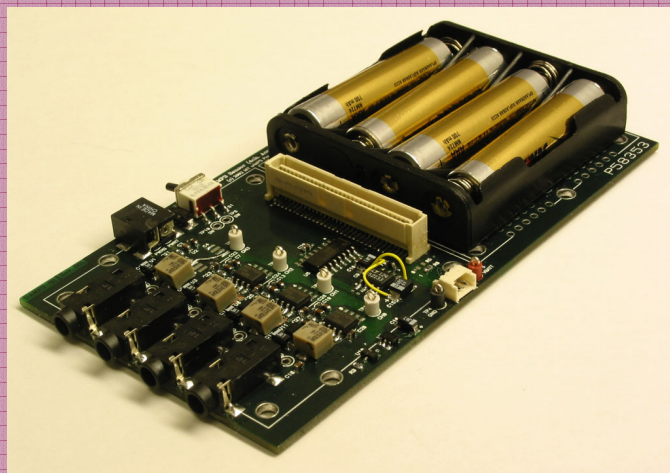
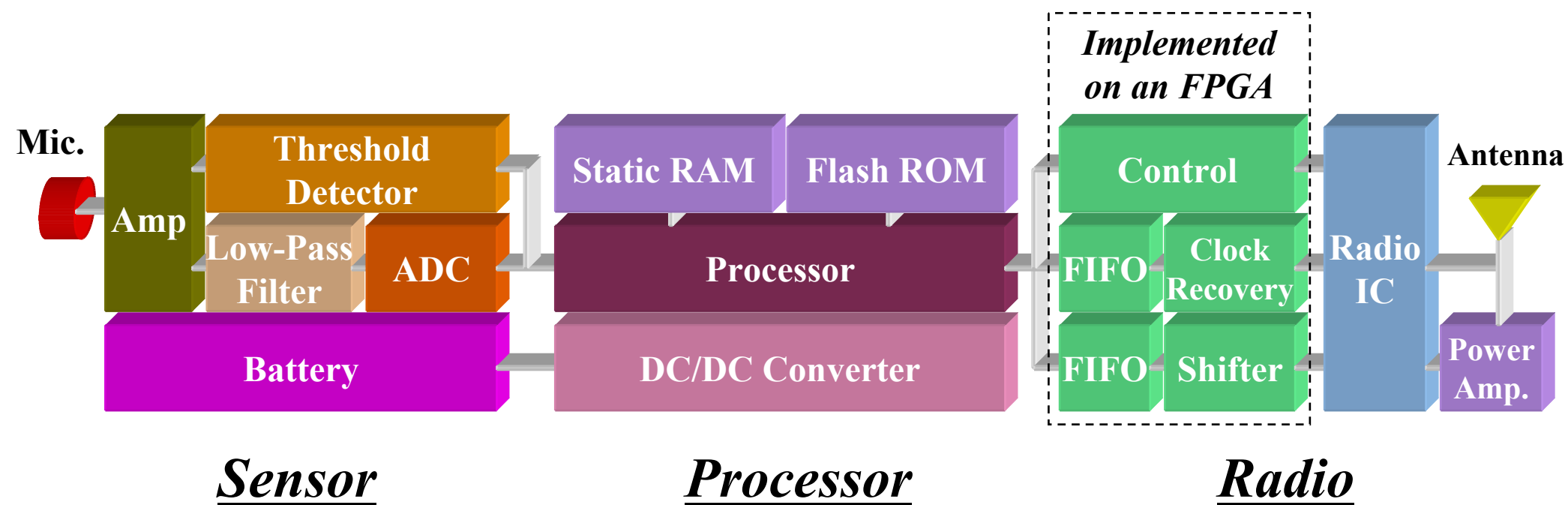


Power Aware Microsensor Considerations

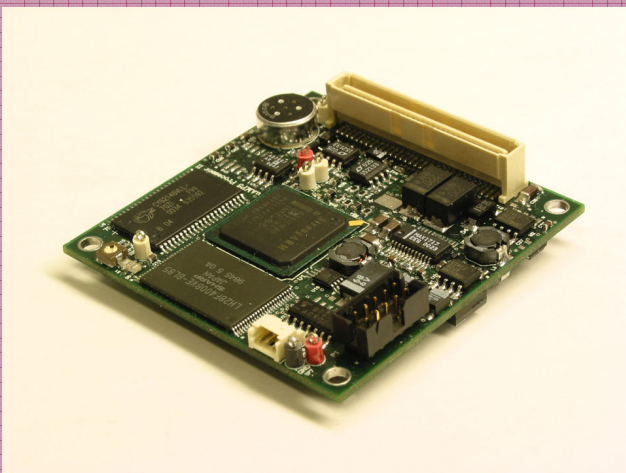




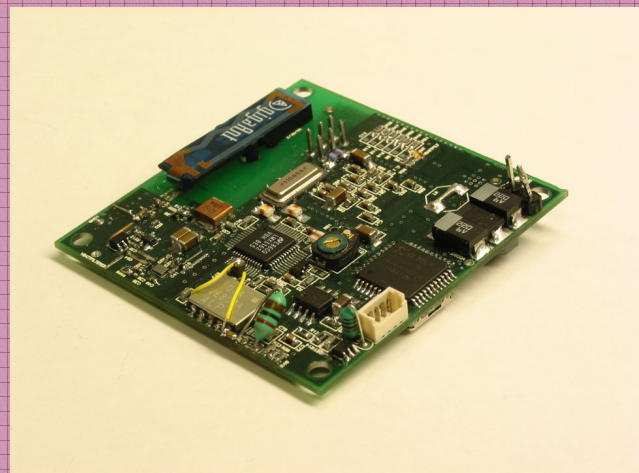
First Generation Wireless Microsensor



4-channel acoustic



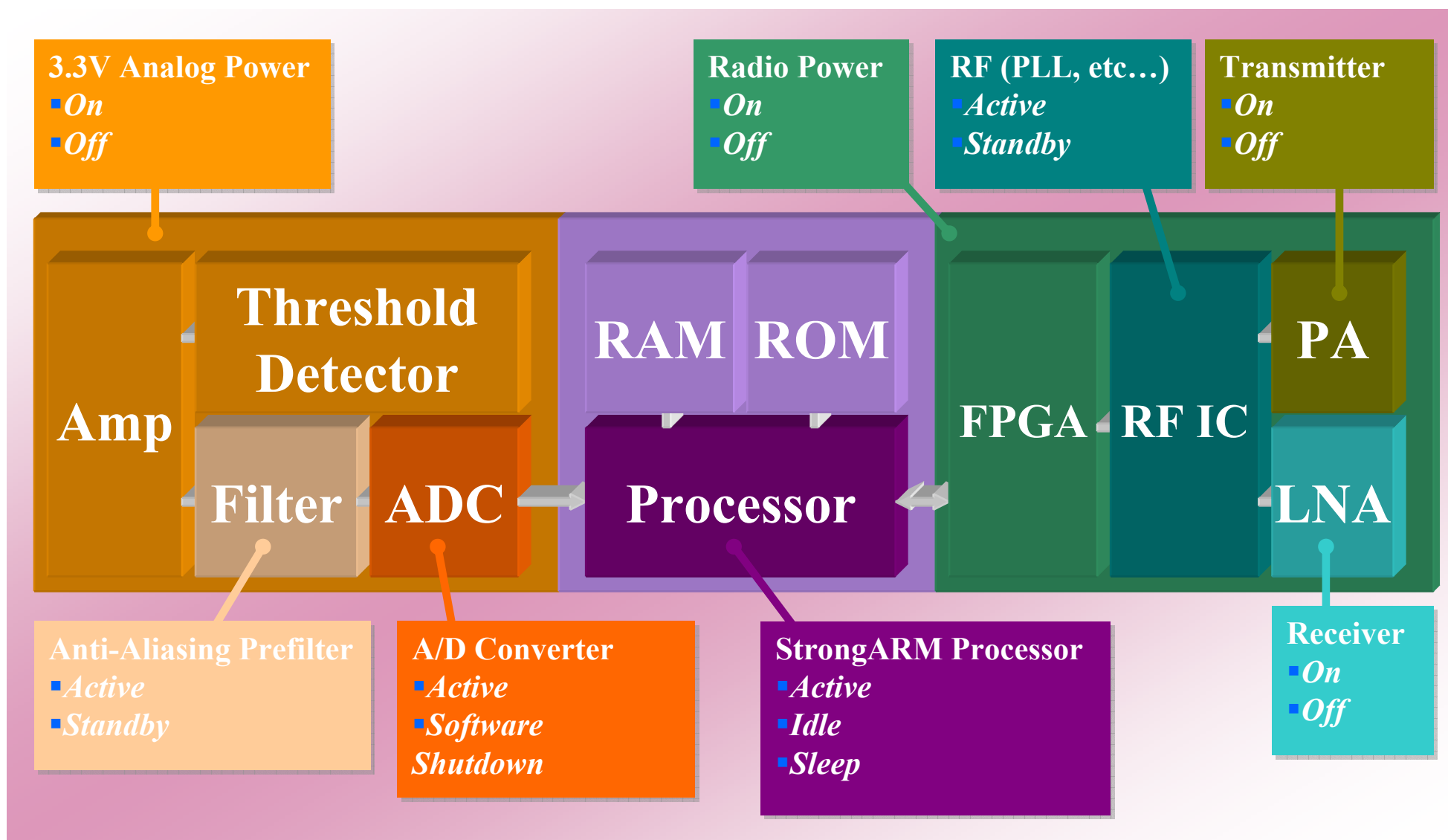
206MHz StrongARM



2.4GHz ISM band



Fine Grain Shut Down Control



- **Active Power Management:** DVS, variable ECC and packet size, variable transmit power, agile algorithms



OS-Controlled Power Down Modes

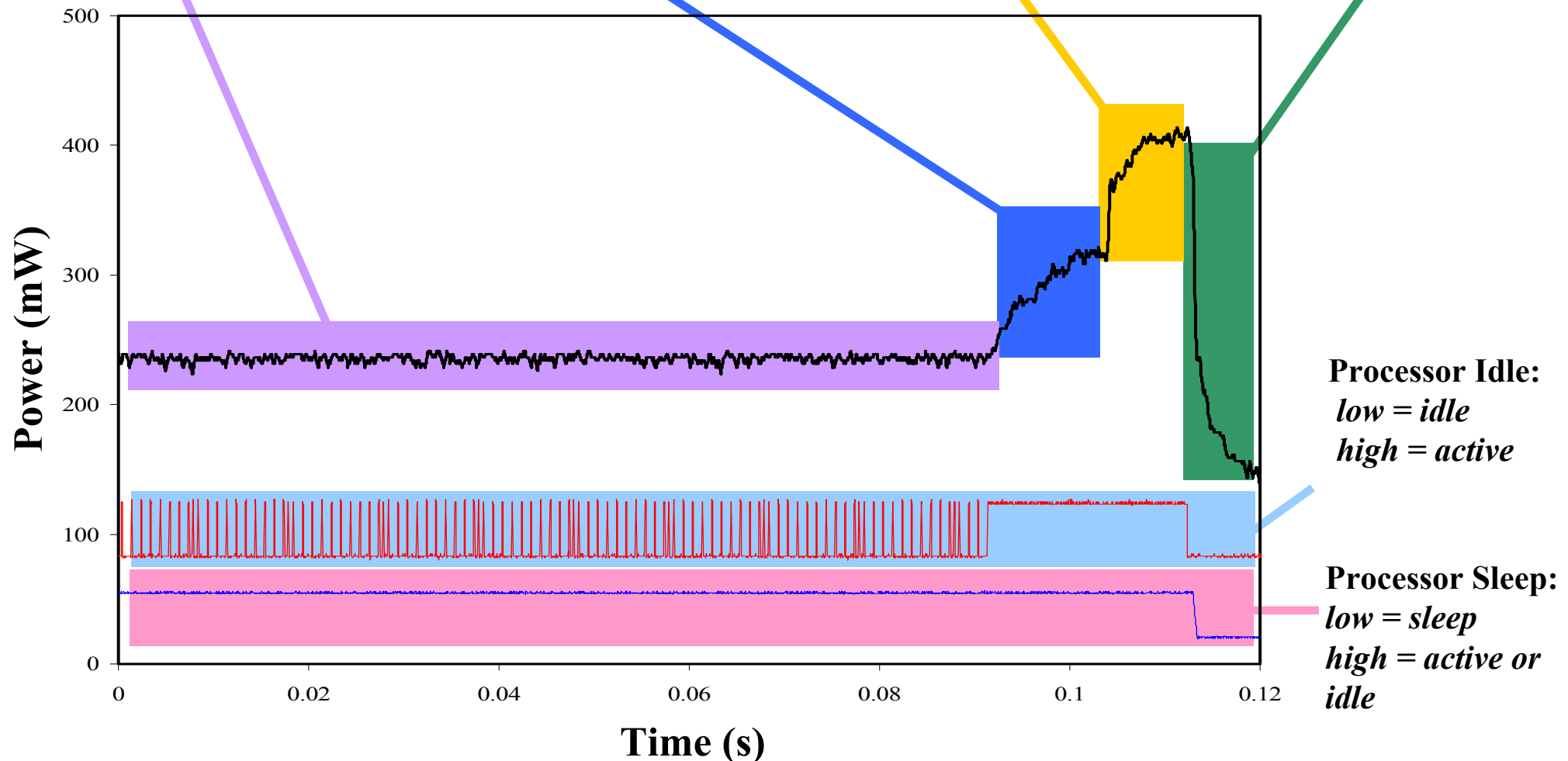


Data collection: 1024 samples at 1kSPS
(Processor alternates between idle/active)

LOB Calculation
(Processor active full-time)

Data transmission
(Radio transmitter active)

Sleep
(All systems power down)

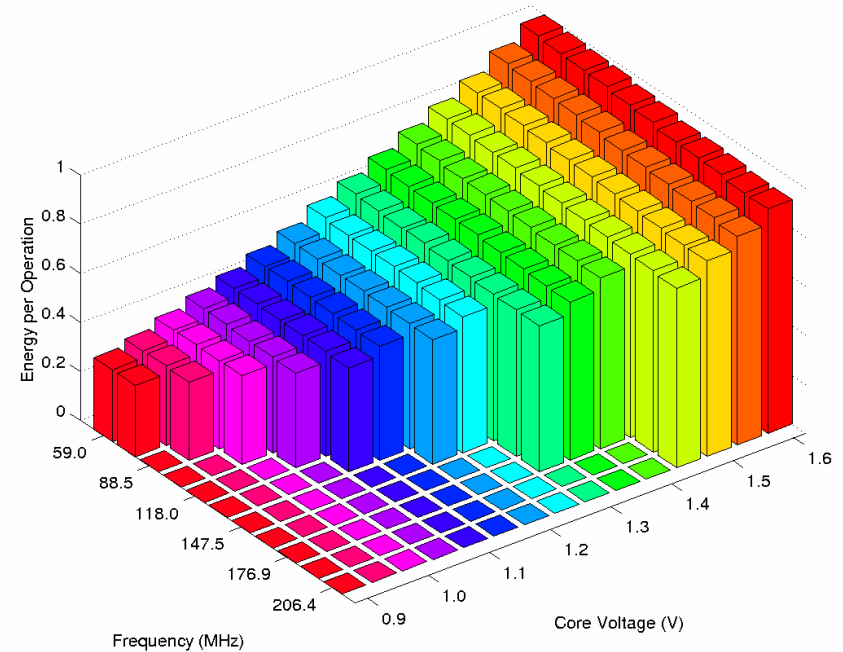
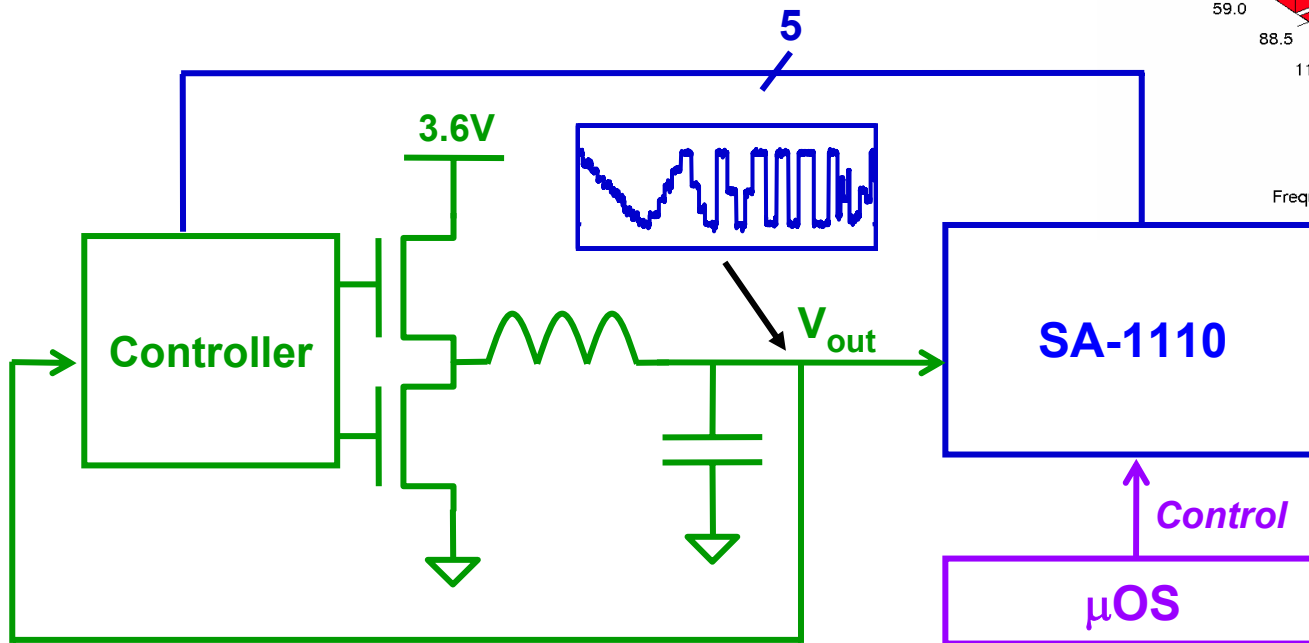




Dynamic Voltage Scaling



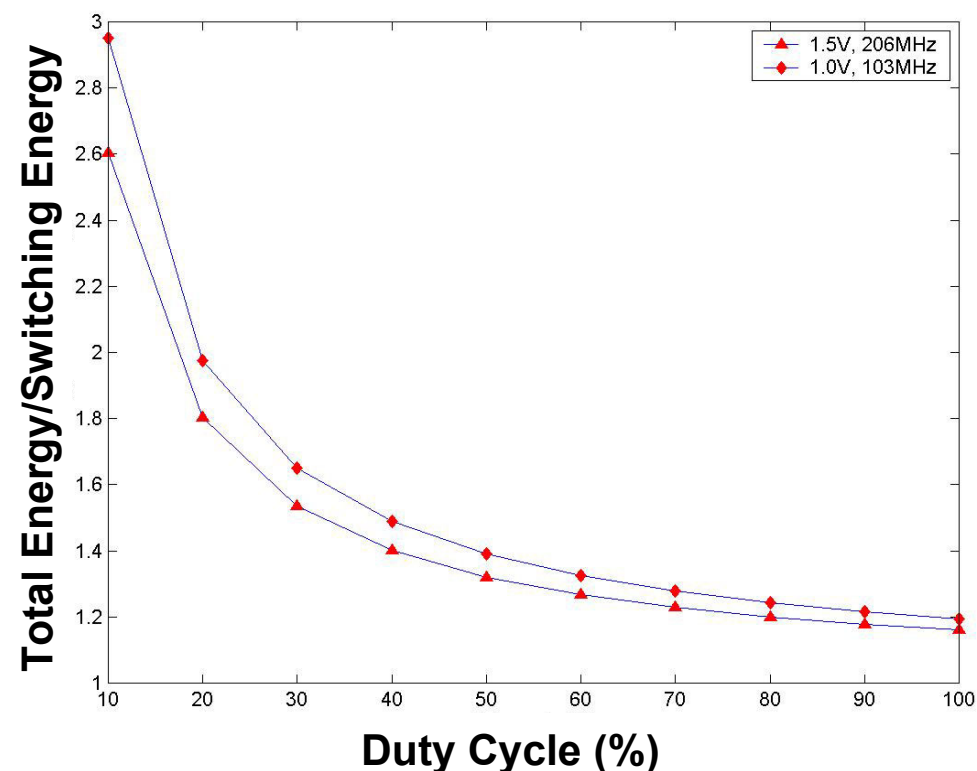
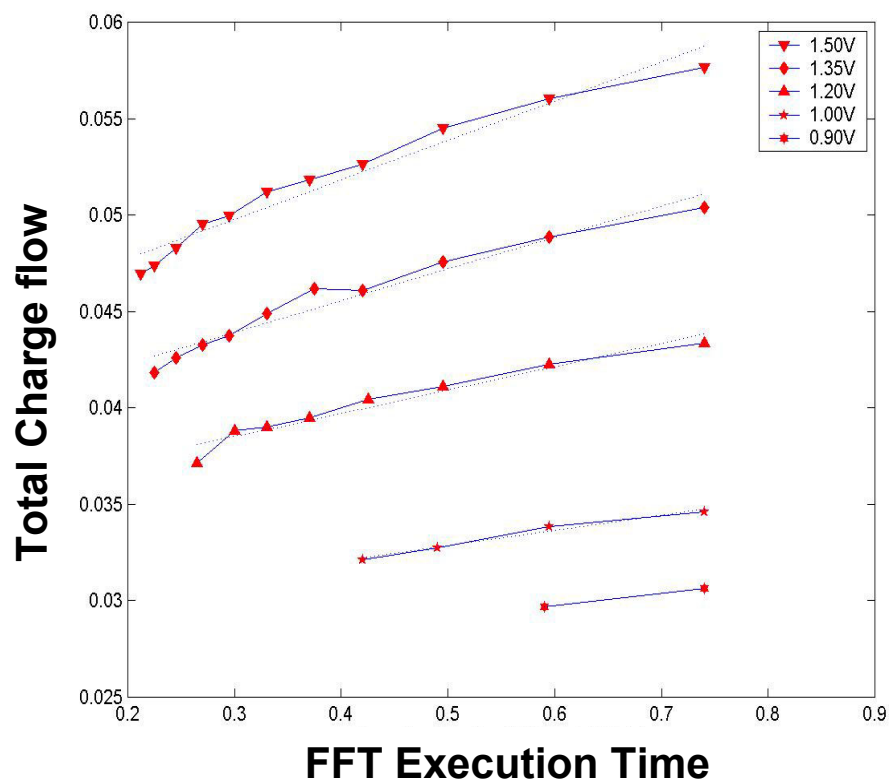
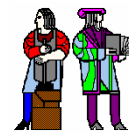
Digitally adjustable DC-DC converter powers SA-1110 core



μOS selects appropriate clock frequency based on workload and latency constraints



Leakage : Low Duty Cycle Concern

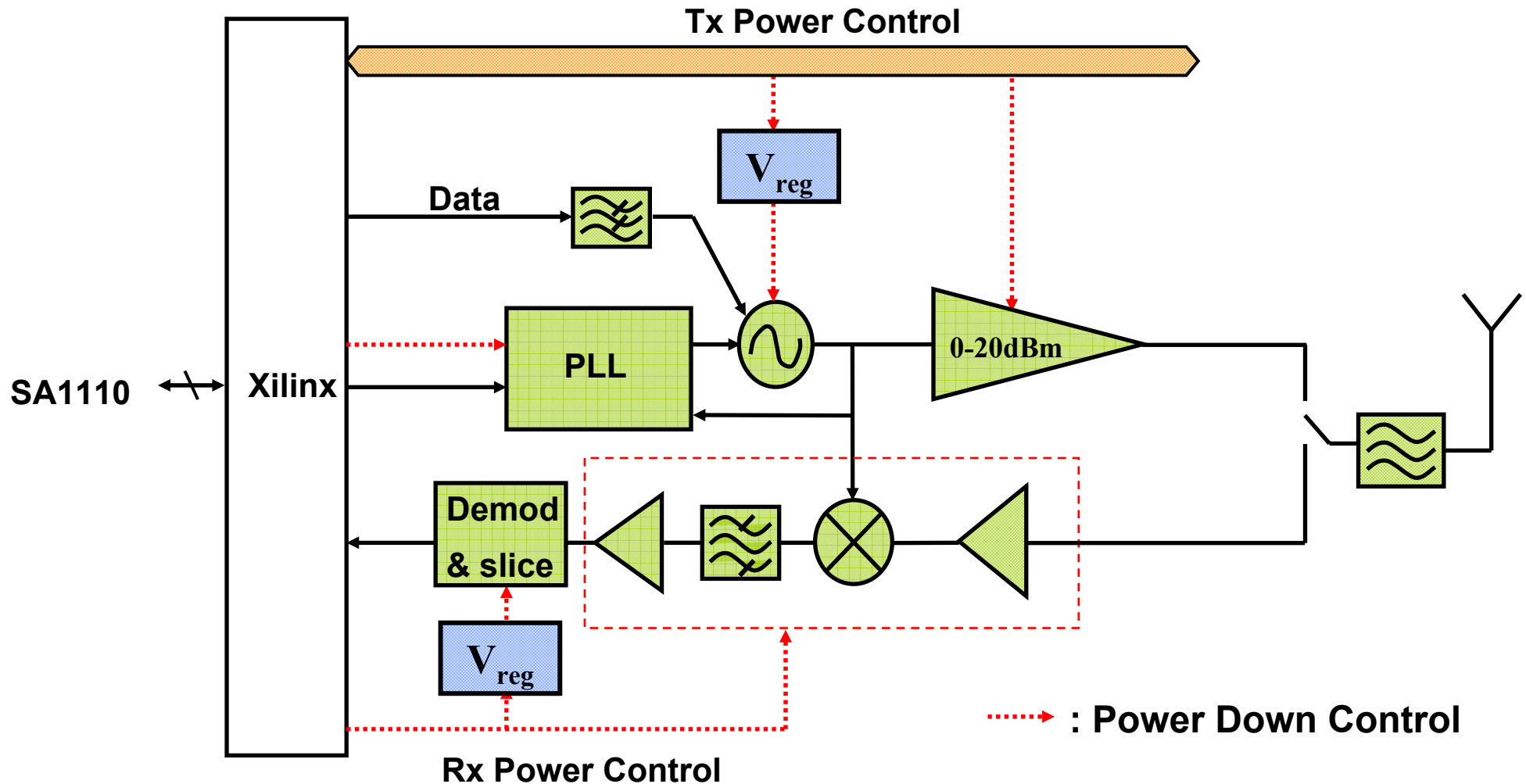


$$I_{leakage} \propto 10^{(-V_T / S)}$$

Leakage Dominates Switching Energy for Low Duty Cycles – “Off” State-centric Optimization



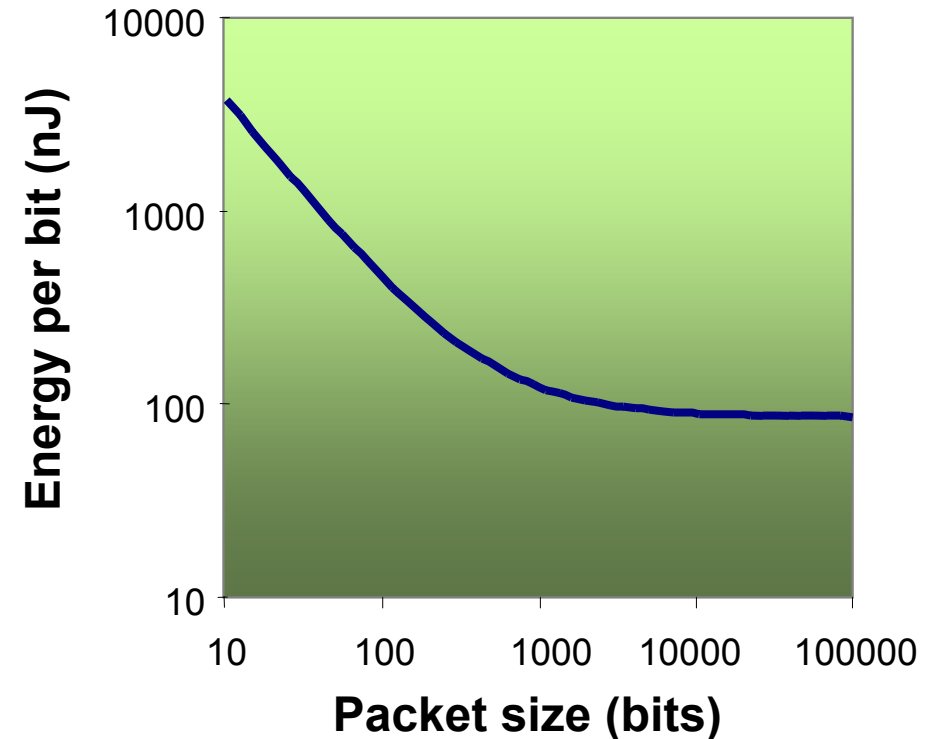
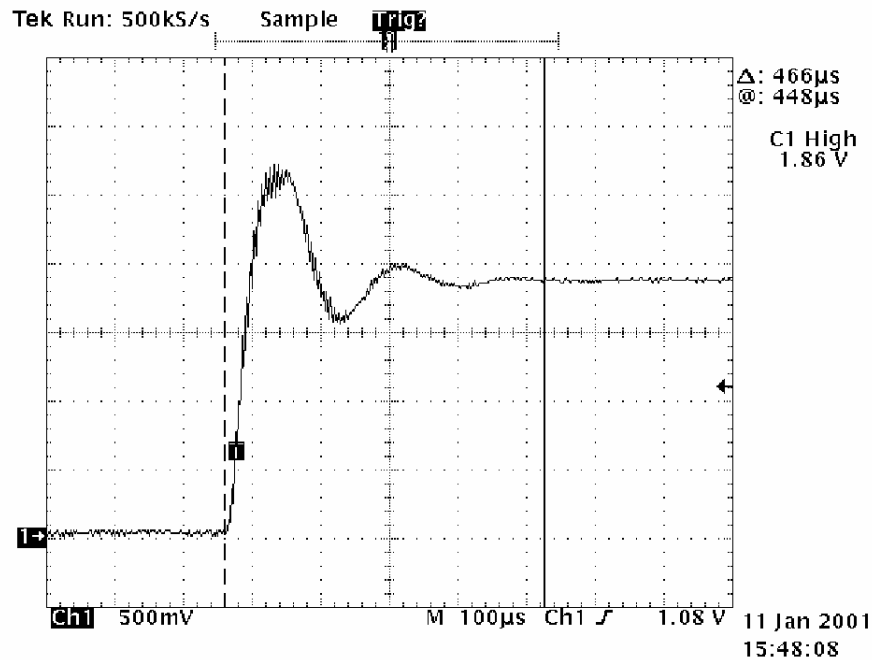
Power Aware Radio



- Fine-grain shutdown through regulators and bias control
- Variable 6-level PA allows efficient transmission for 10m to 100m



RF Start-up Energy Overhead



$$Energy = P_{tx_electronics} (T_{transmit} + T_{start}) + P_{out} T_{transmit}$$

- Significant loss in energy efficiency for small packet sizes

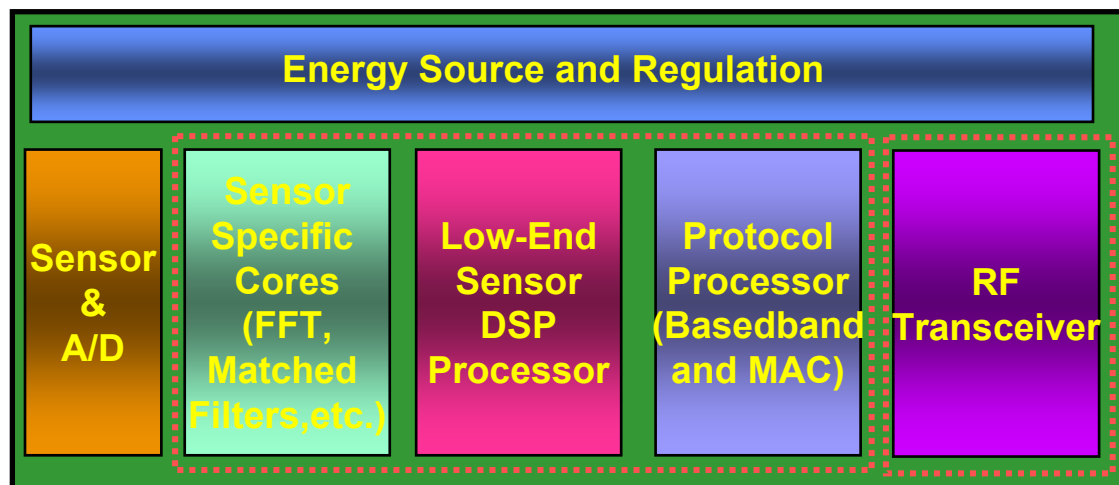
**Startup Costs are Fundamental –
Innovative Circuits and Protocols Required**



Next Generation Sensor Nodes



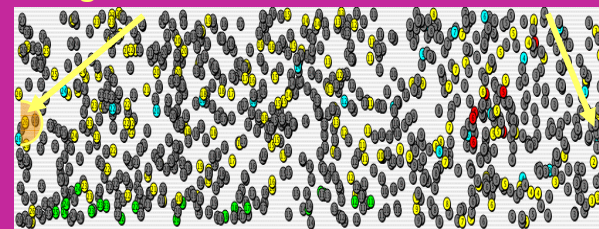
Sensor System-on-a-Chip



- Compact Form Factor ($\text{mm}^3 - \text{cm}^3$)
- Low Rate Radio link (10-100kbs)
- System Power $< 100\mu\text{W}$

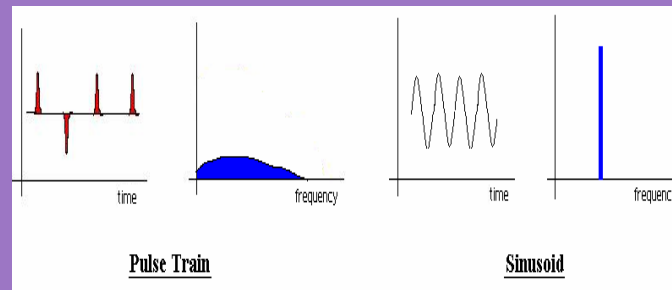
Network API/Simulation

Region of Observation Base Station



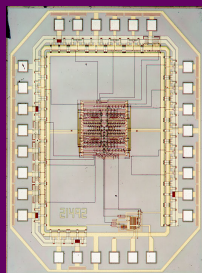
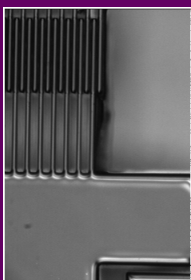
How to simulate 1000's nodes?

Ultra-Wideband Radio



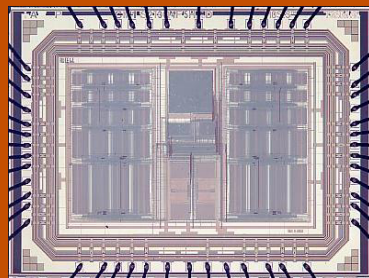
High-speed & Low-power Time Domain Processing

Energy Processing



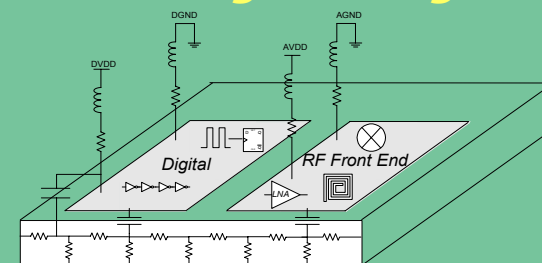
How to Scavenge $100\mu\text{W}$?

Ultra Low-Voltage Digital Circuits



Design for 100mV Supply

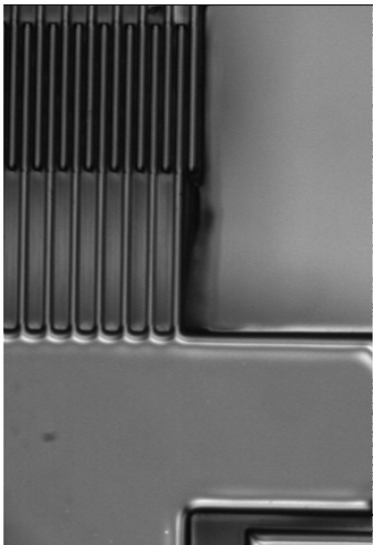
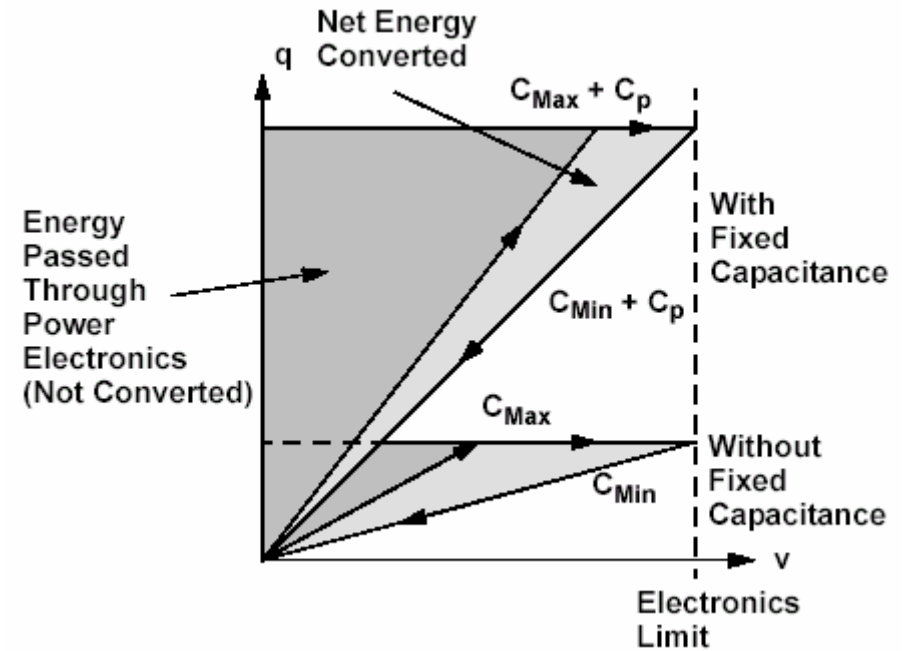
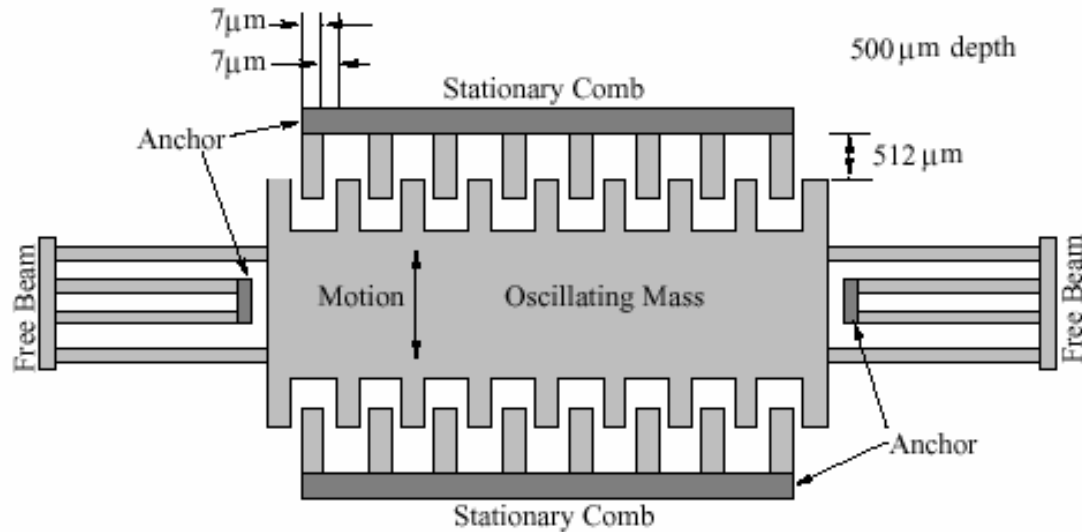
Mixed-Signal Design



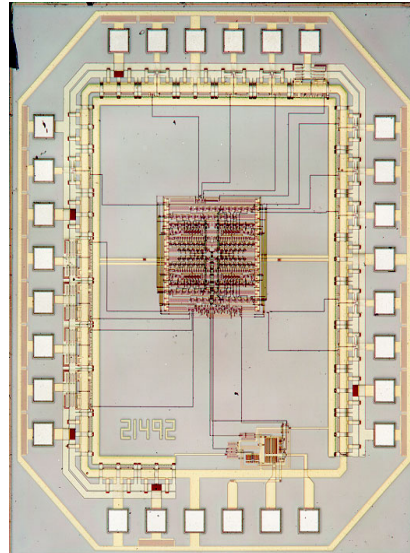
How to Integrate RF & Digital?



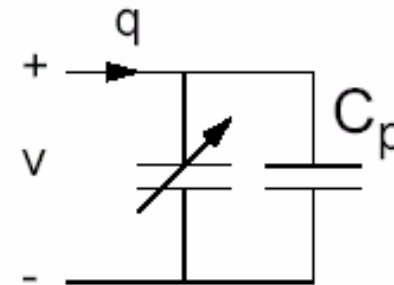
Energy Scavenging: Vibration-to-Electric Energy



MEMS Generator



Controller



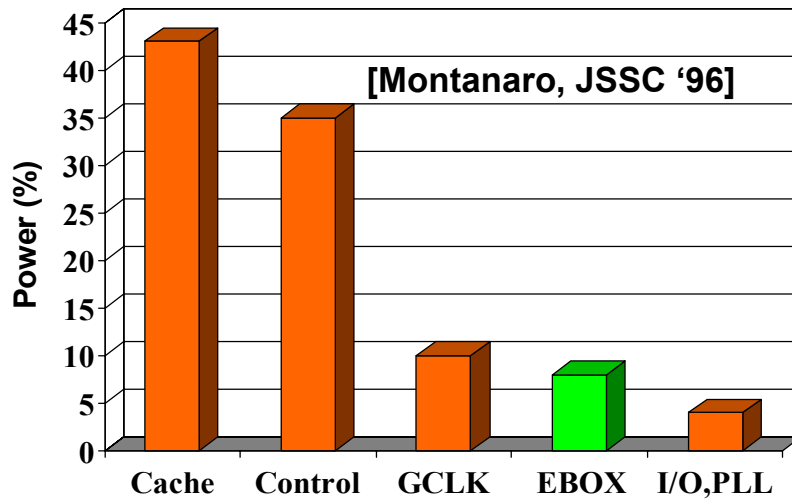
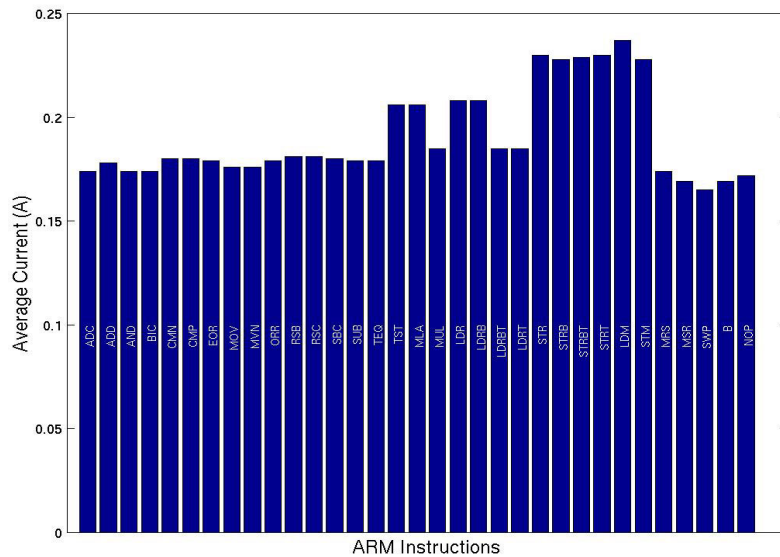
10 μW from generator possible



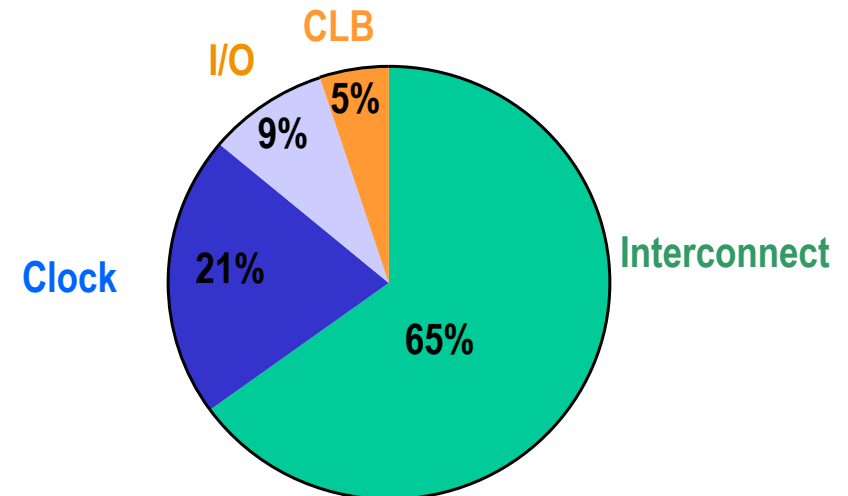
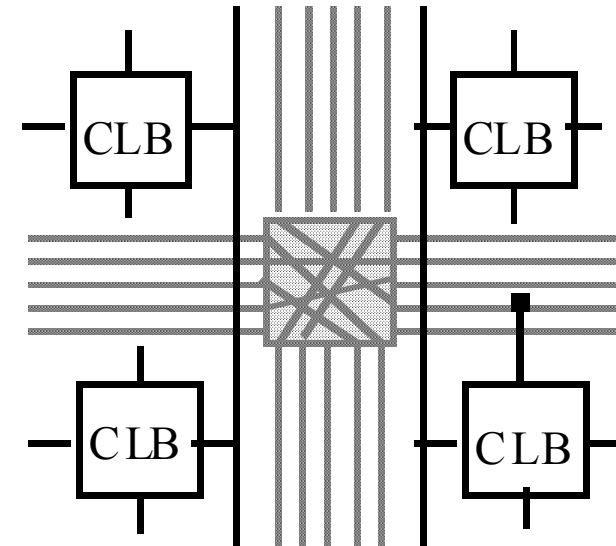
Programmable Software Fabrics



Processor (StrongARM-1100)



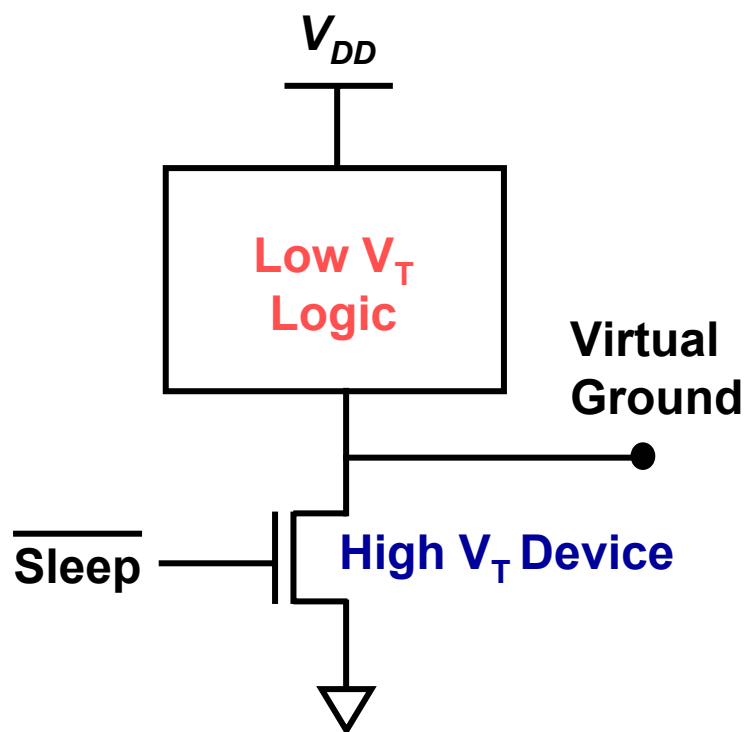
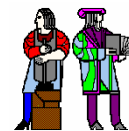
FPGA (Xilinx)



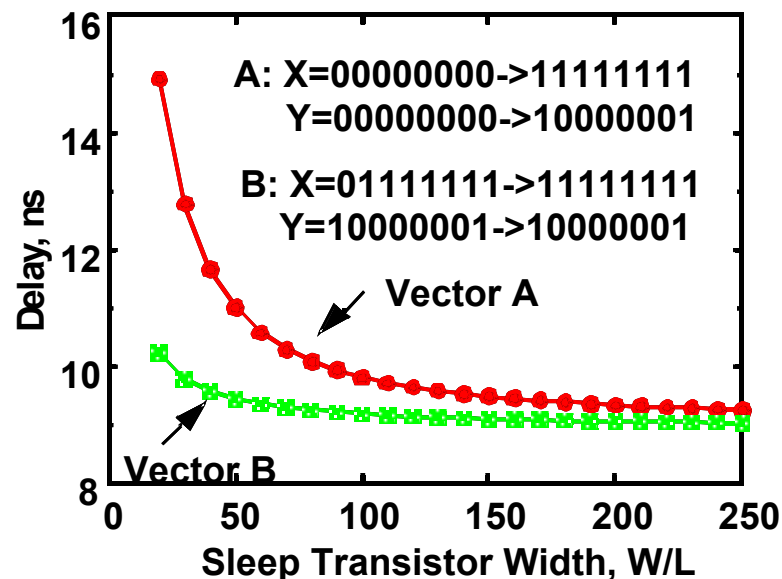
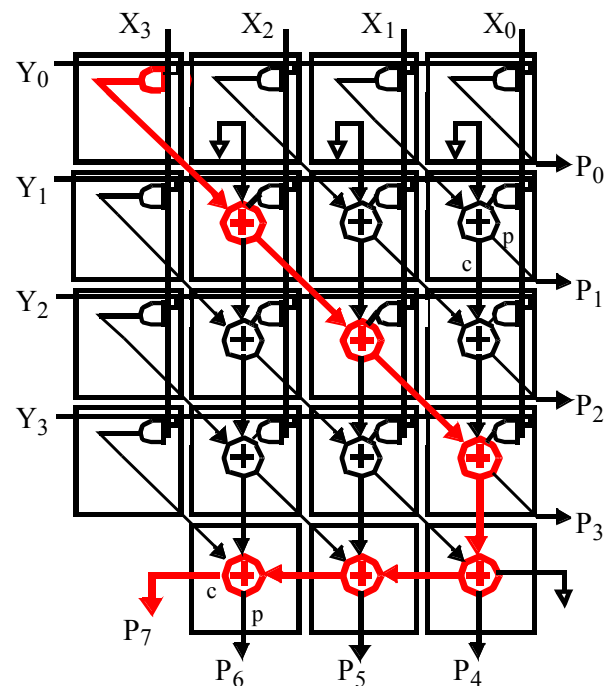
“Software” Energy Dissipation is Dominated by Overhead and NOT by Useful Work



Leakage Mitigation Using MTCMOS



Device Sizing is a Major Concern in Multiple Threshold CMOS

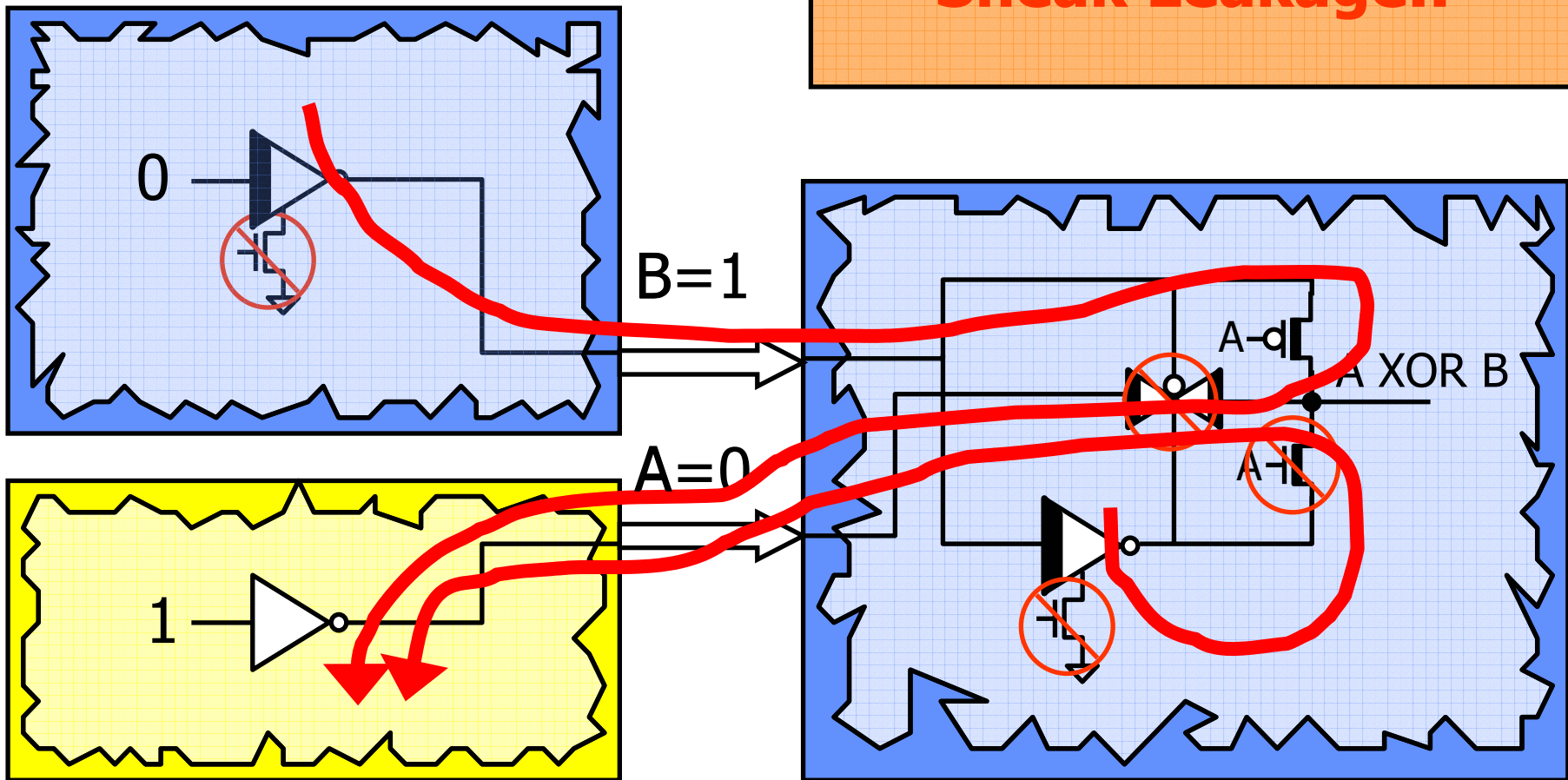




Leakage Reduction Using MTCMOS



**Look at A=0 and B=1.
Sneak Leakage!!**

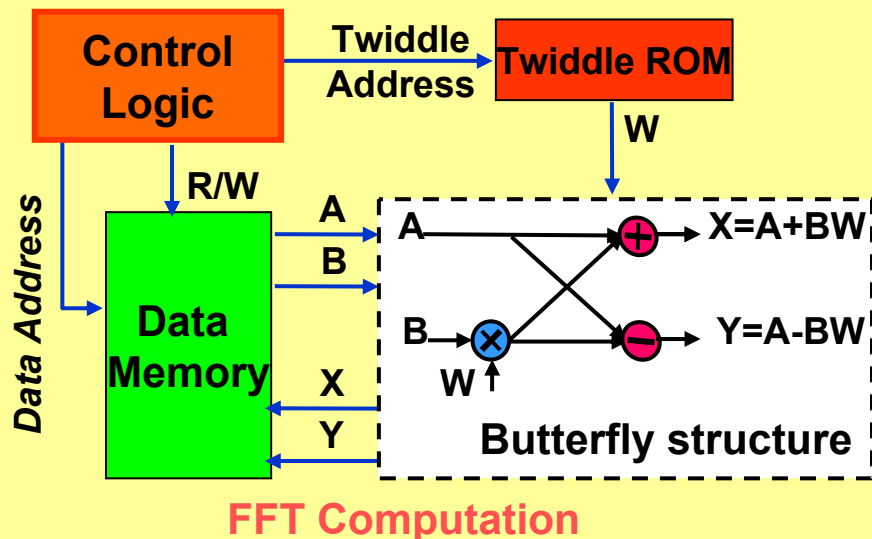




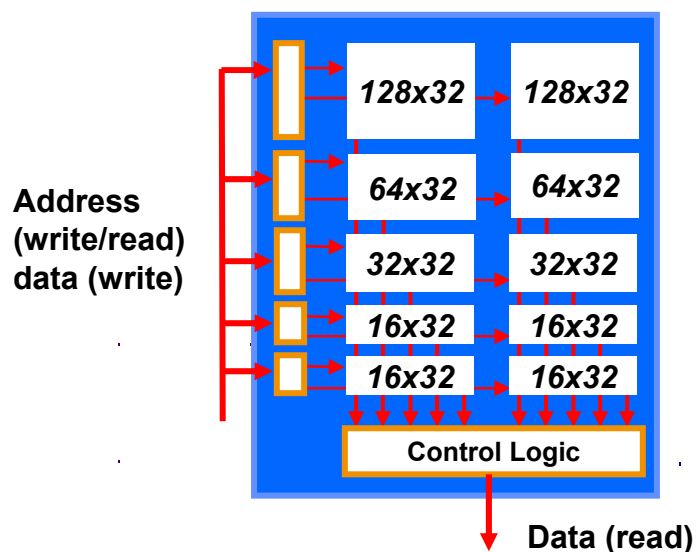
Power Aware Architectures



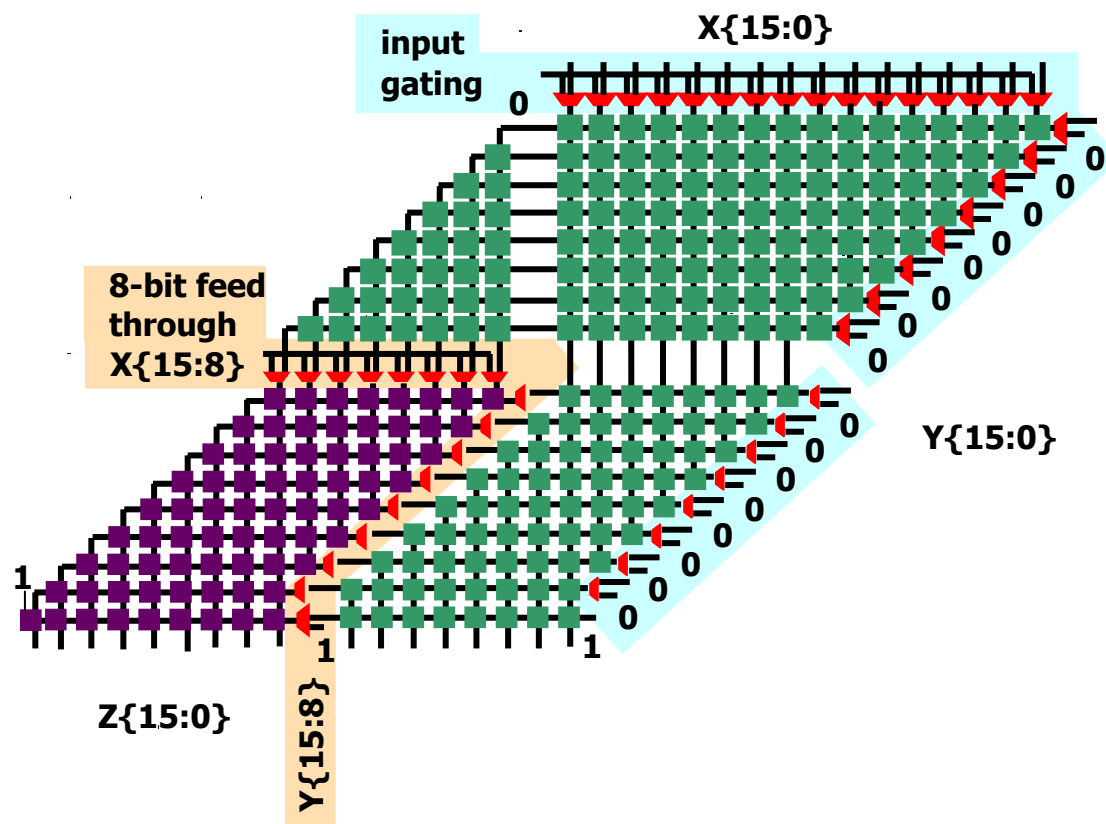
Single butterfly architecture (4 multipliers, 6 adders)



Power Scalable Memory



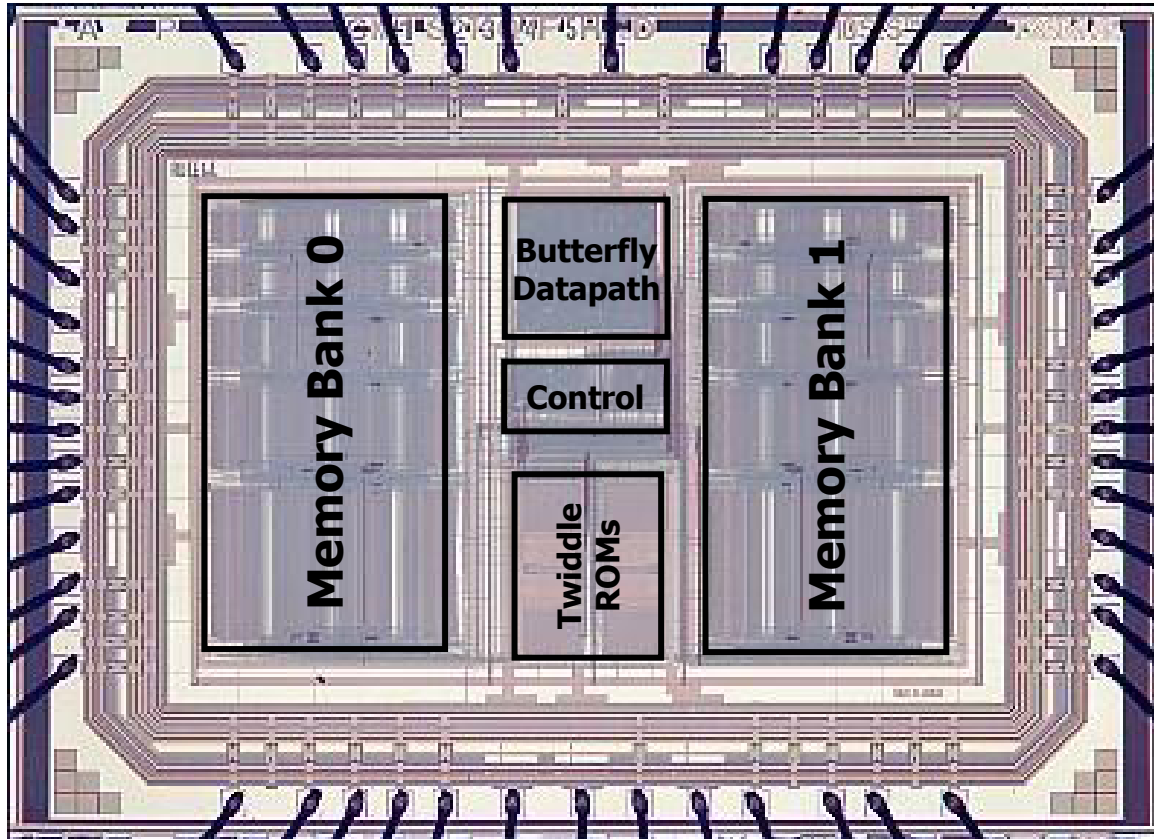
Power Scalable Multiplier (modified Baugh-Wooley)



- Adder used only in 16-bit mode
- Adder used in 8-bit And 16-bit mode



First Generation Power Aware FFT



Technology Parameters

- 0.18 μ m process
- 2.1mm x 3mm
- $V_{T0n} = 0.45V$, $V_{T0p} = -0.44V$
- $V_{dd} = 1.8V$

Measured energy dissipation

	8-bit	16-bit
128 pt.	46 nJ	81 nJ
256 pt.	121 nJ	216 nJ
512 pt.	304 nJ	564 nJ

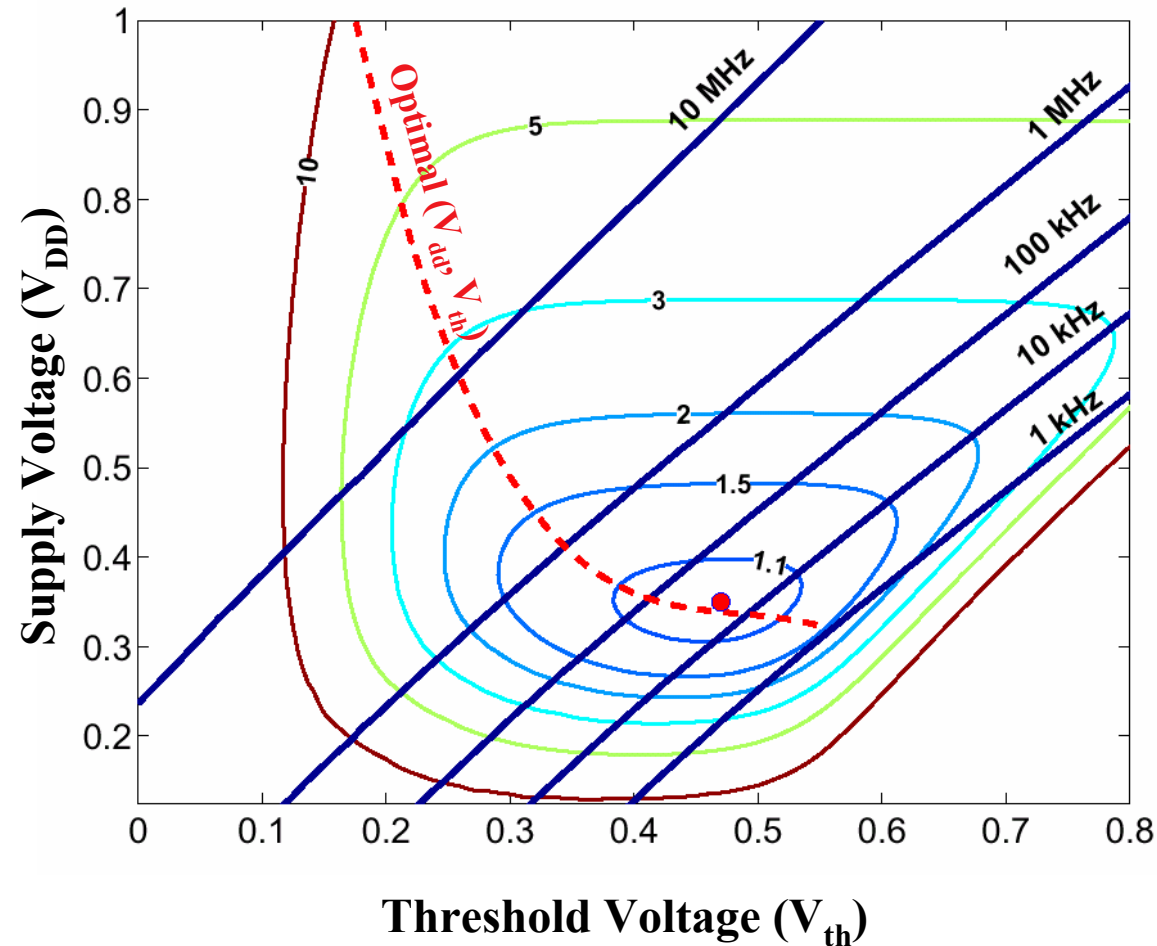
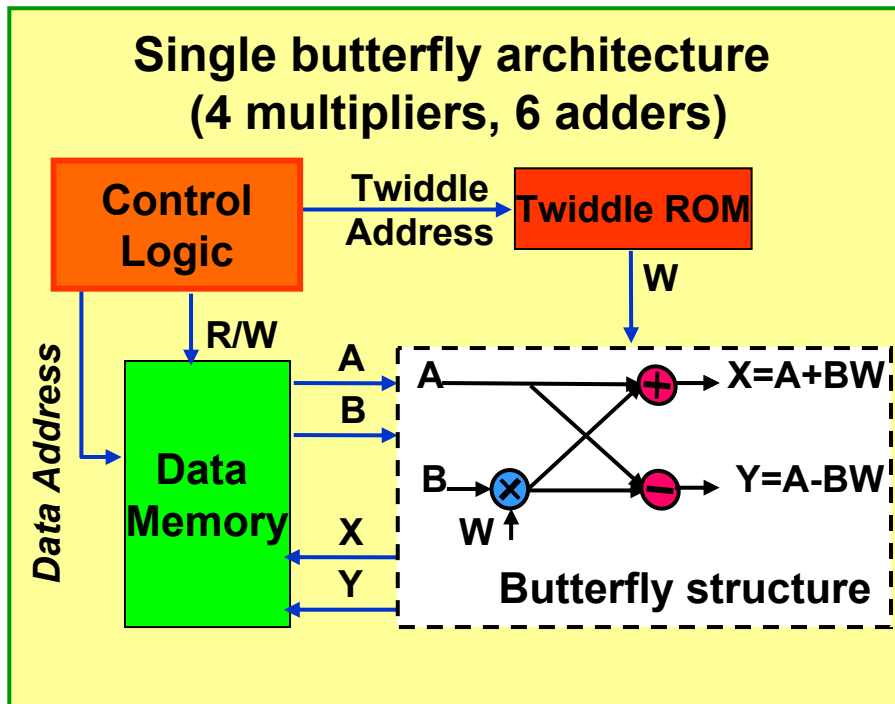
Power programmable from 128pts to 512pts
and 8 bits and 16 bits



Energy Efficiency of Digital Computation



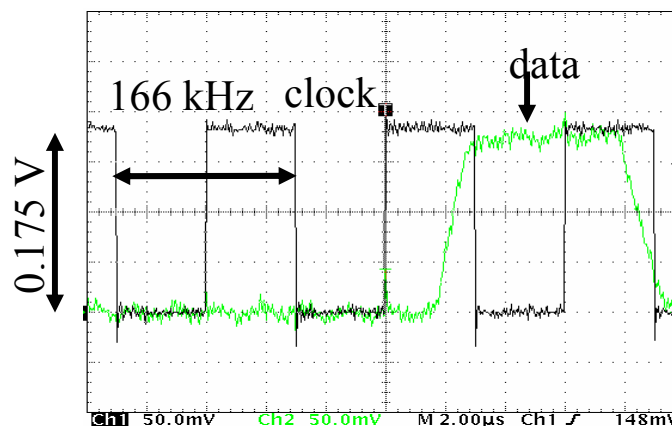
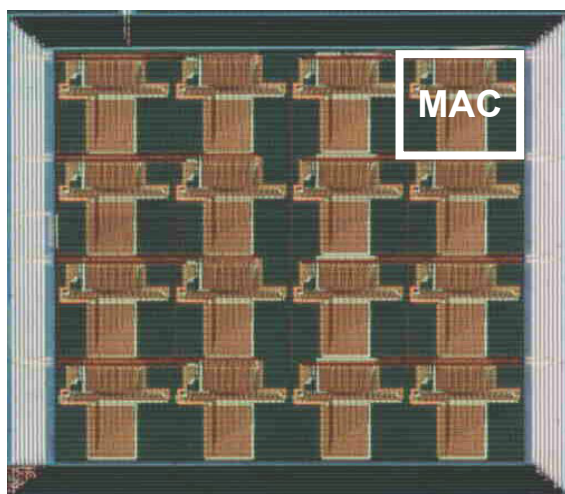
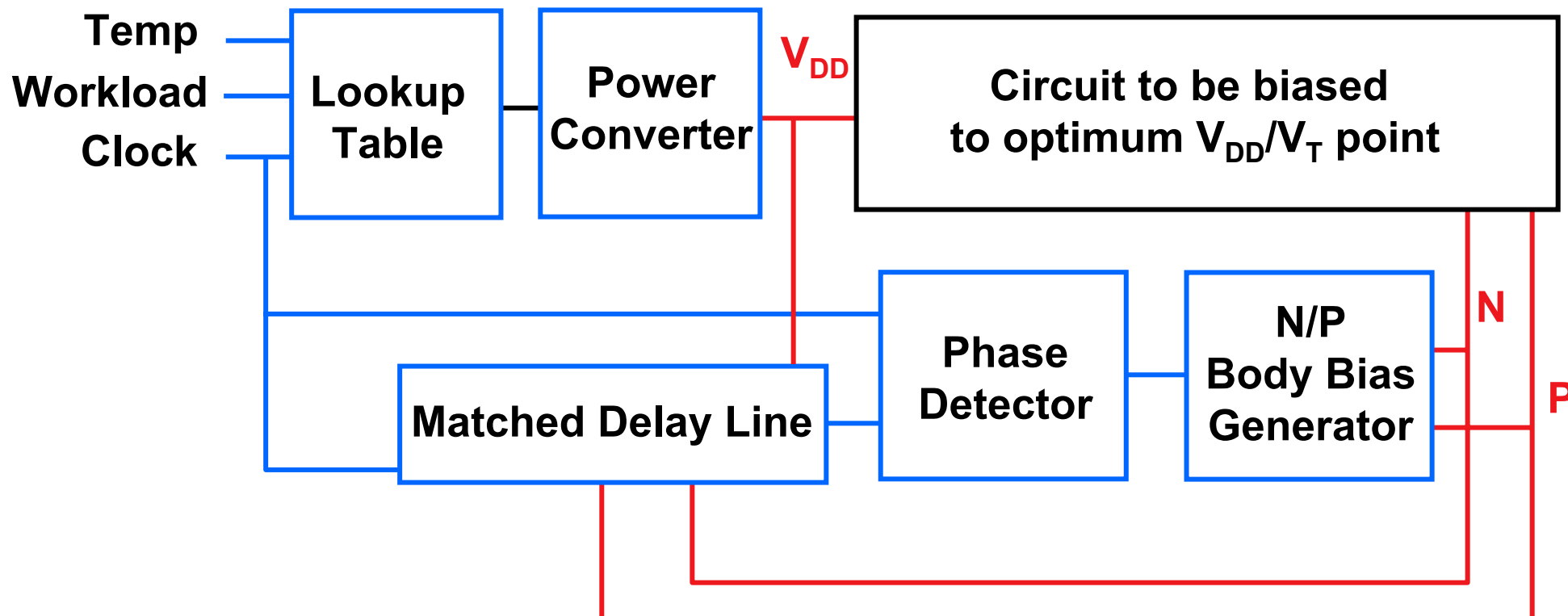
FFT Computation



Exploit Sub-threshold Operation for Sensor Circuits



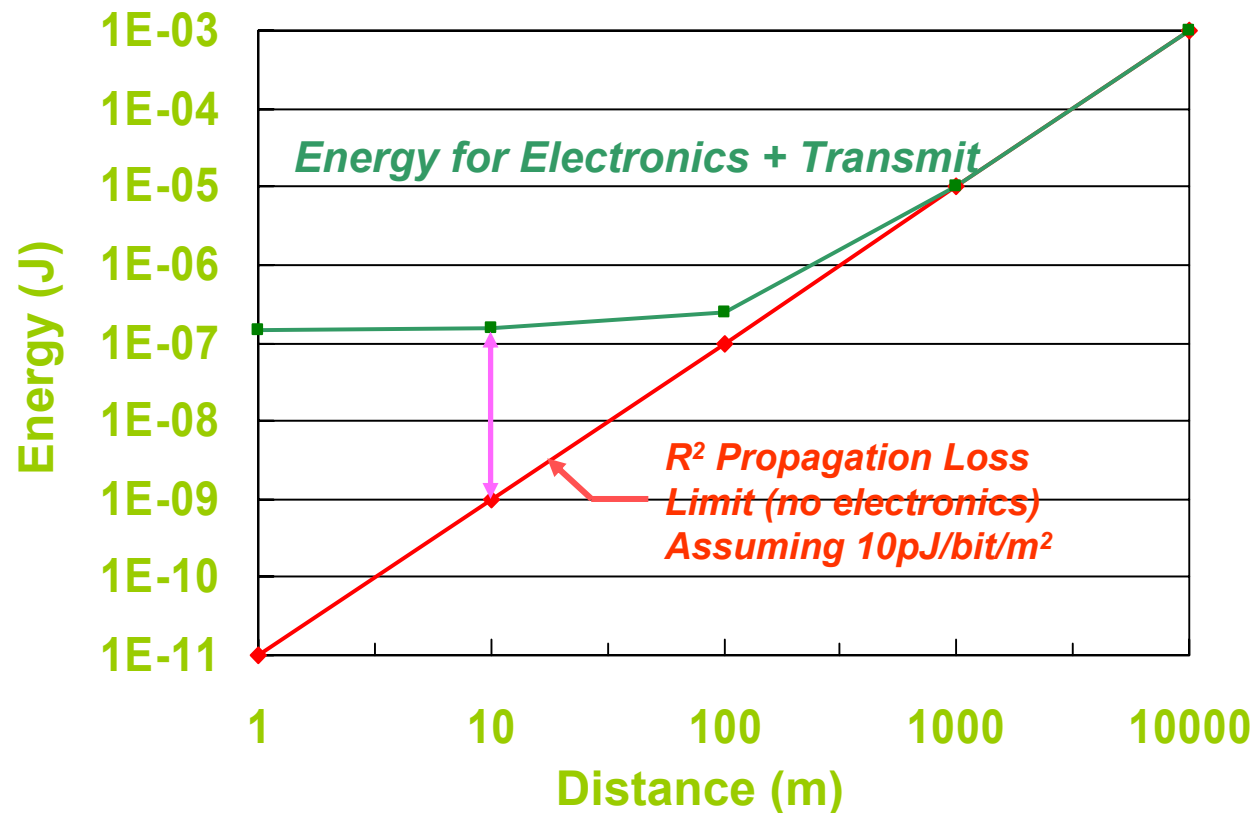
Adaptive V_{DD}/V_T Architecture



[Miyazaki, ISSCC '02]



Computation vs. Communication

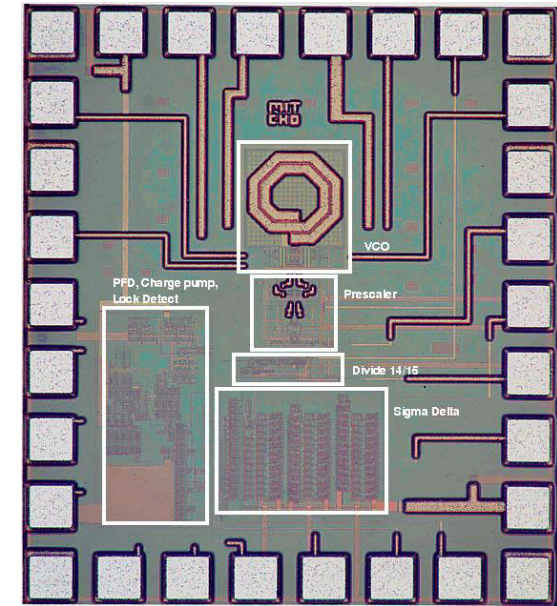
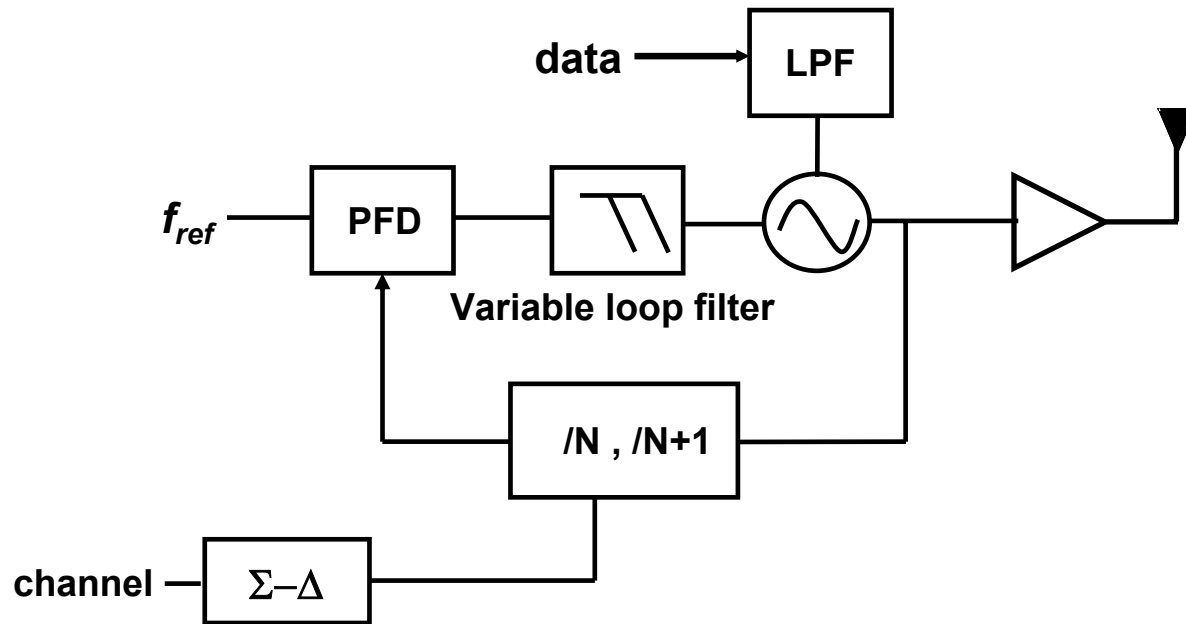


- Computation: 1nJ/op (μ -Processor) and Communication (@10m): 150nJ/bit
- @10 m: ~ 150 instructions/transmitted bit on a low-power processor
- @10m: $> 1\text{Million}$ instructions/transmitted bit using dedicated hardware

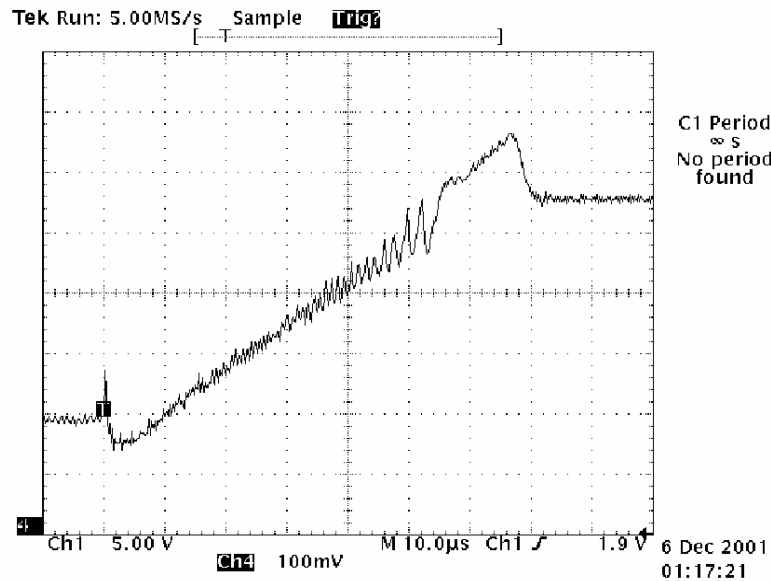
Compute, Don't Communicate



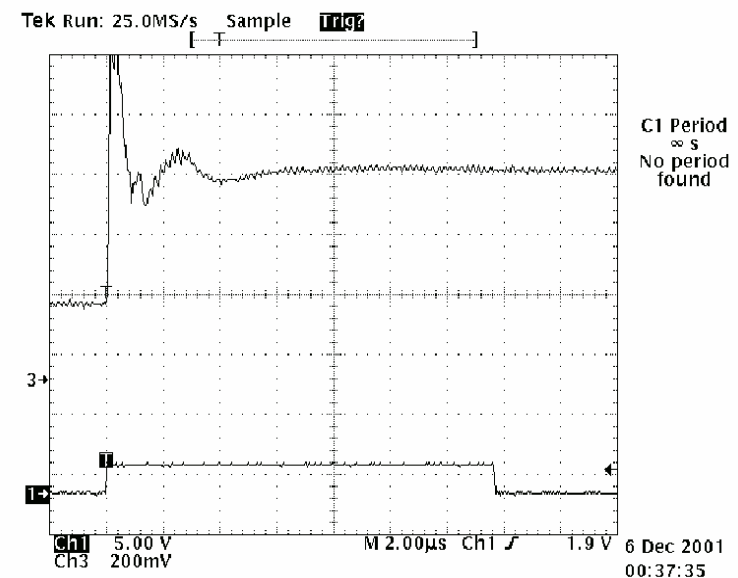
Fast Startup Transmitter



$$E/bit = 10nJ/bit$$



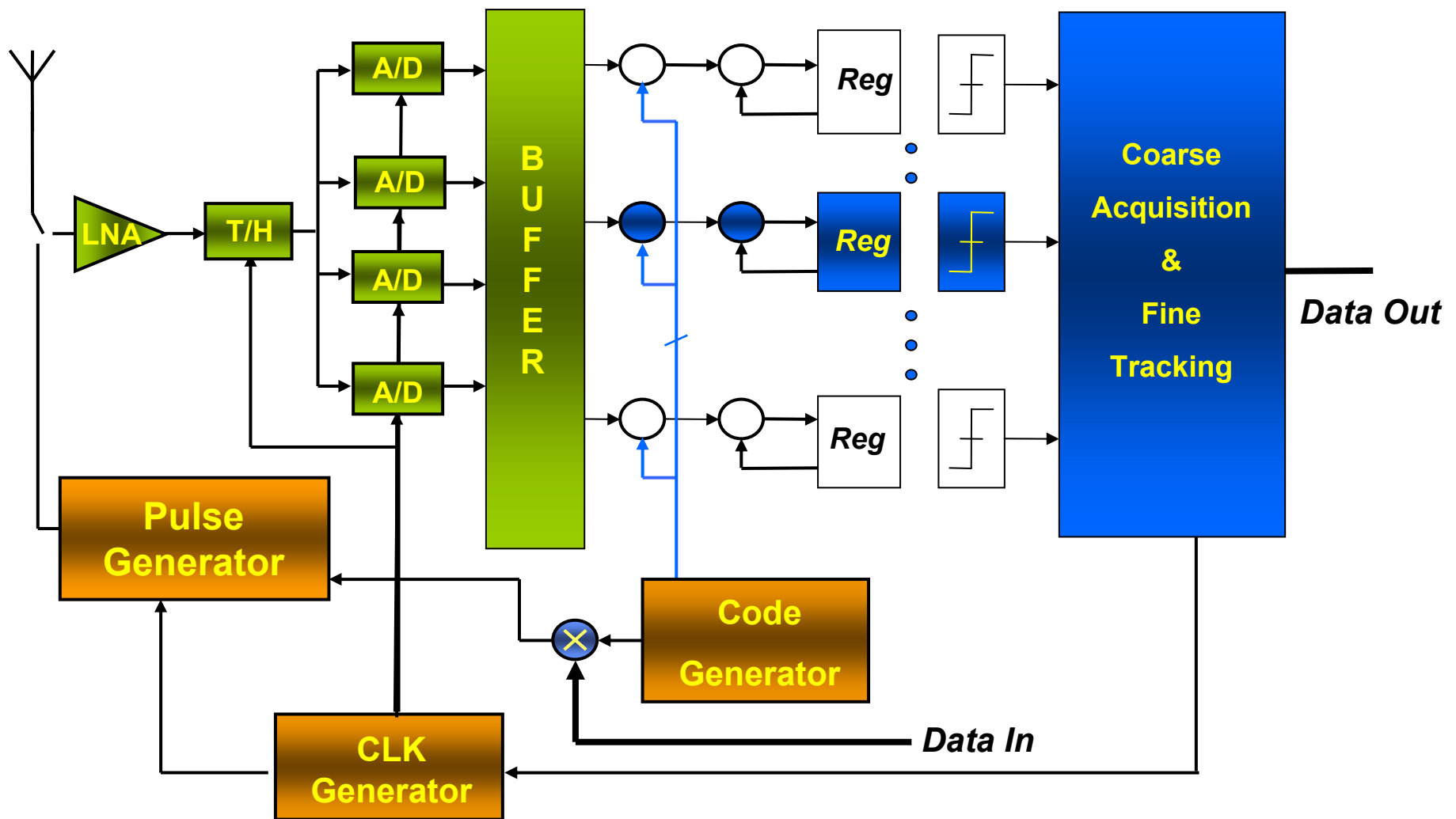
Fixed loop bandwidth



Variable loop bandwidth



New Opportunities: “Digital” UWB Radio



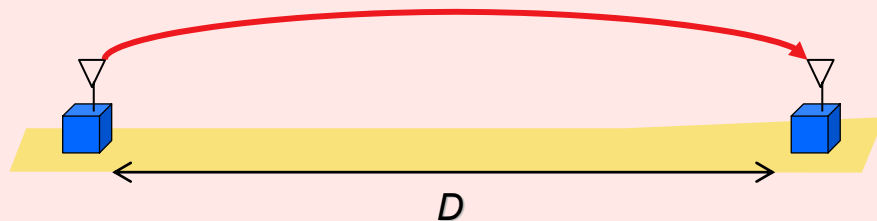
- Minimal Front-end components: leverage low-power digital circuits
- 3-4 bits A/D sufficient (Newaskar, Blazquez, Chandrakasan, SIPS '02)



Multihop and the Characteristic Distance

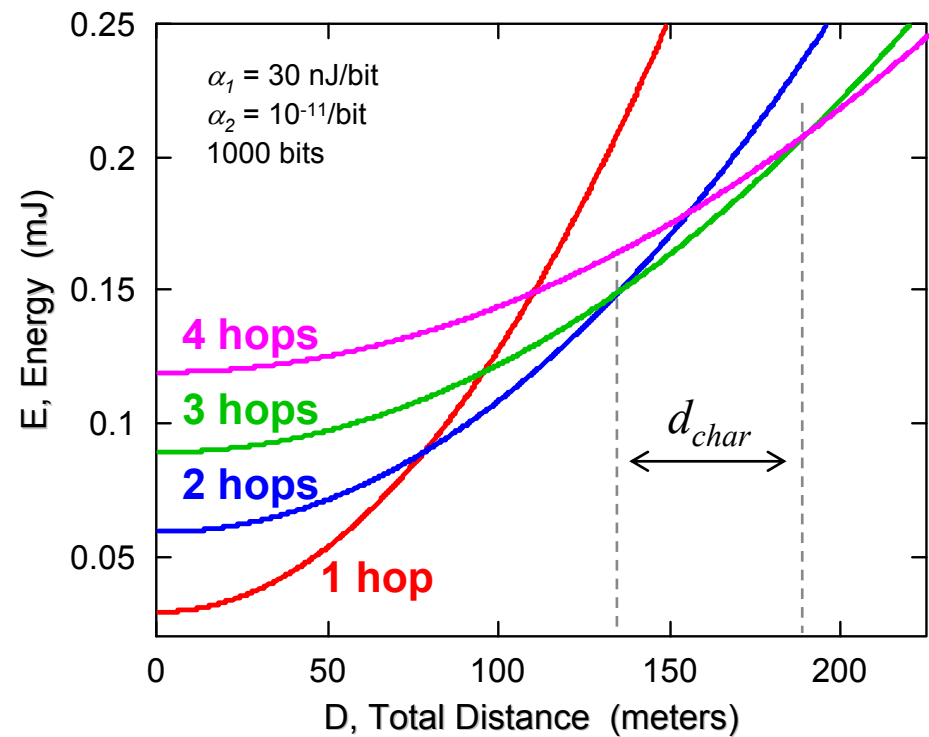


Direct Transmission

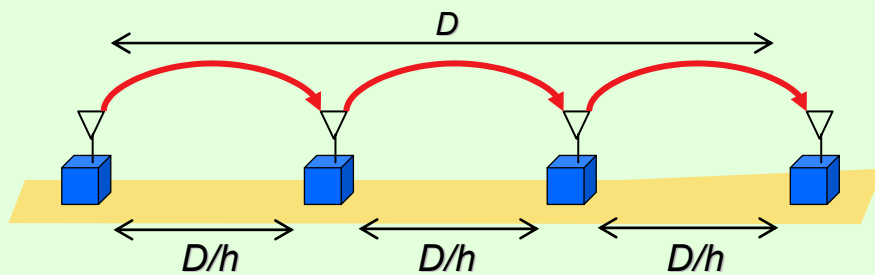


$$E = \alpha_1 + \alpha_2 D^2$$

α_1 : Tx & Rx Radio Electronics
 α_2 : attenuation, power amp
path loss exponent



Multihop Transmission



$$E = h \left[\alpha_1 + \alpha_2 \left(\frac{D}{h} \right)^2 \right]$$

h : number of hops
per-hop distance

Characteristic Distance for Multihop Transmission

$$\min_h E = 2\alpha_1 \frac{D}{d_{char}}$$

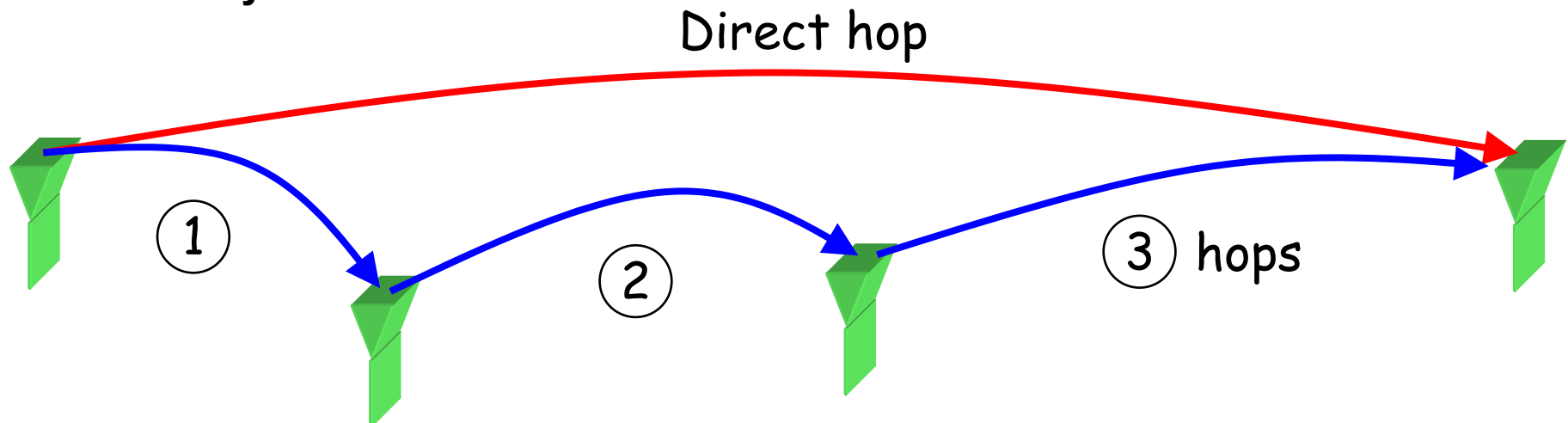
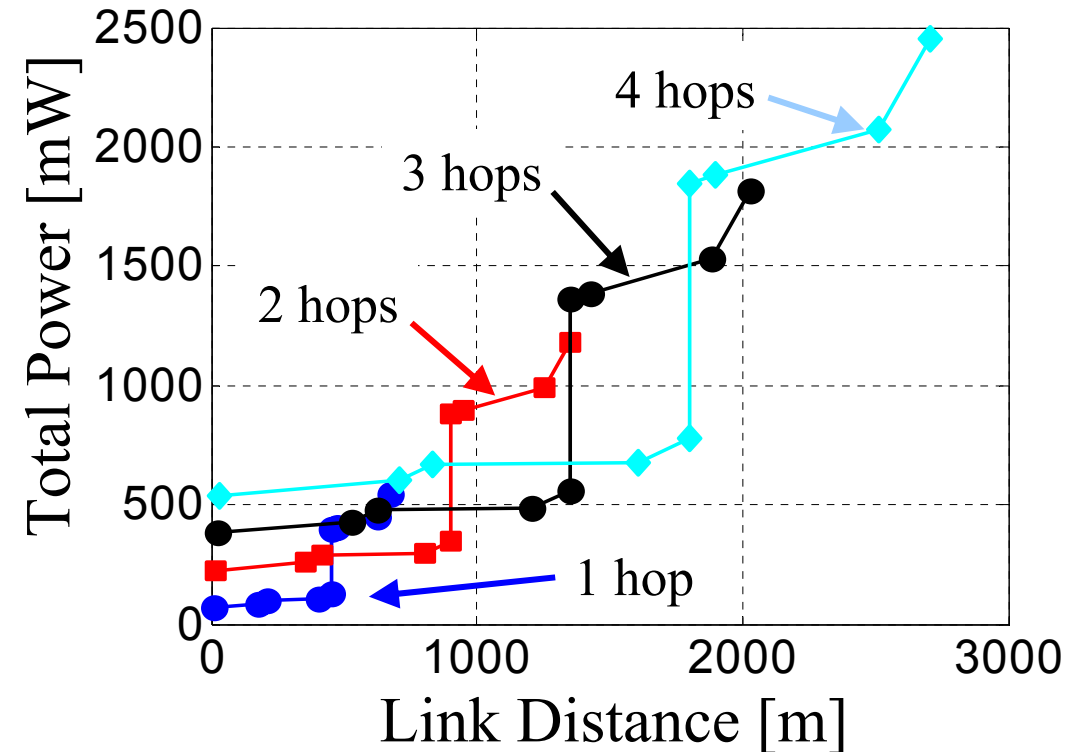
$$\text{where } d_{char} = \sqrt{\alpha_1 / \alpha_2}$$



Multi-Hop Routing Analysis

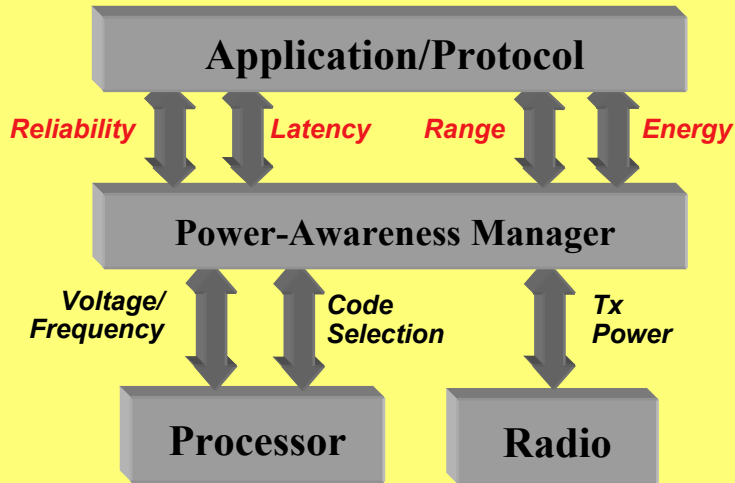


- Take advantage of dense sensor networks by using several shorter hops to transmit long distances
- Plot of total power used to transmit a given distance for 1, 2, 3, and 4 hops
 - Large power step in each trace from turning on external PA
 - Trace out lowest curve for energy efficiency (i.e. use 3 hops @ 1000 m)
- Multi-hop routing is more energy efficient for this particular radio
 - Adds overhead to the protocol
 - Adds latency to the network





API and Middleware Layer



Power Aware API: performance of communication defined and exposed as a basis for trade-offs

- set_max_energy(Energy energy)
- set_max_latency(Time latency)
- set_min_reliability(Prob probReception)
- set_range(int nearestNodes, Node[] who, float meters)

Quality of communication defined along four axes:

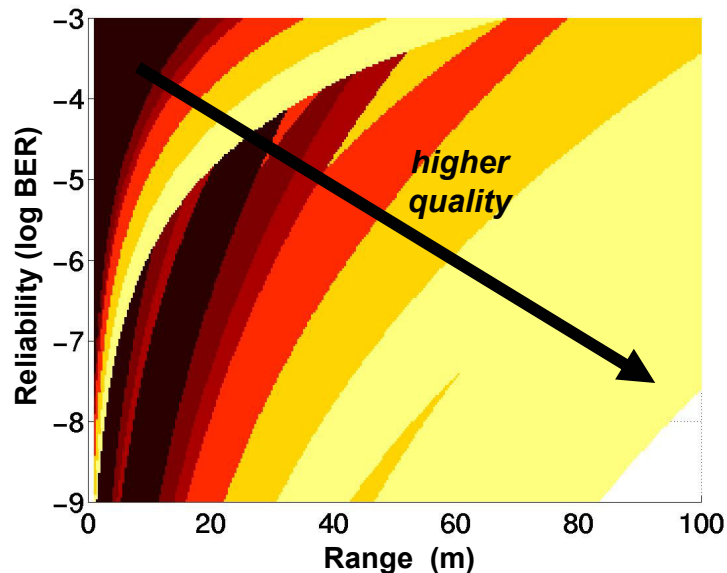
Concern	Metric
“To whom?”	Range (m)
“How soon?”	Latency (ms)
“How reliably?”	Reliability (BER)
“How much energy?”	Energy (μ J)



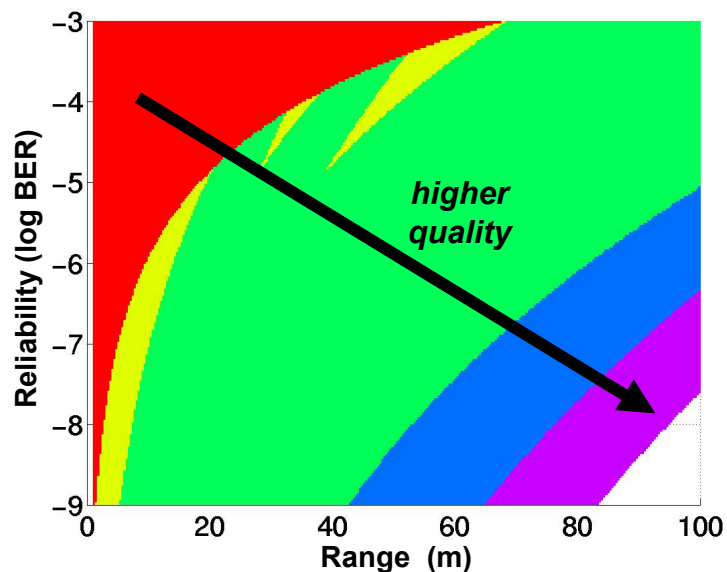
API-Controlled Operational Policy



Radiated Power

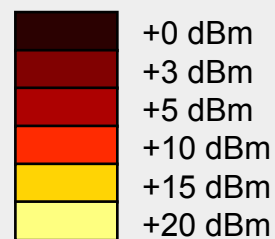


Convolutional Code



Operational Policies

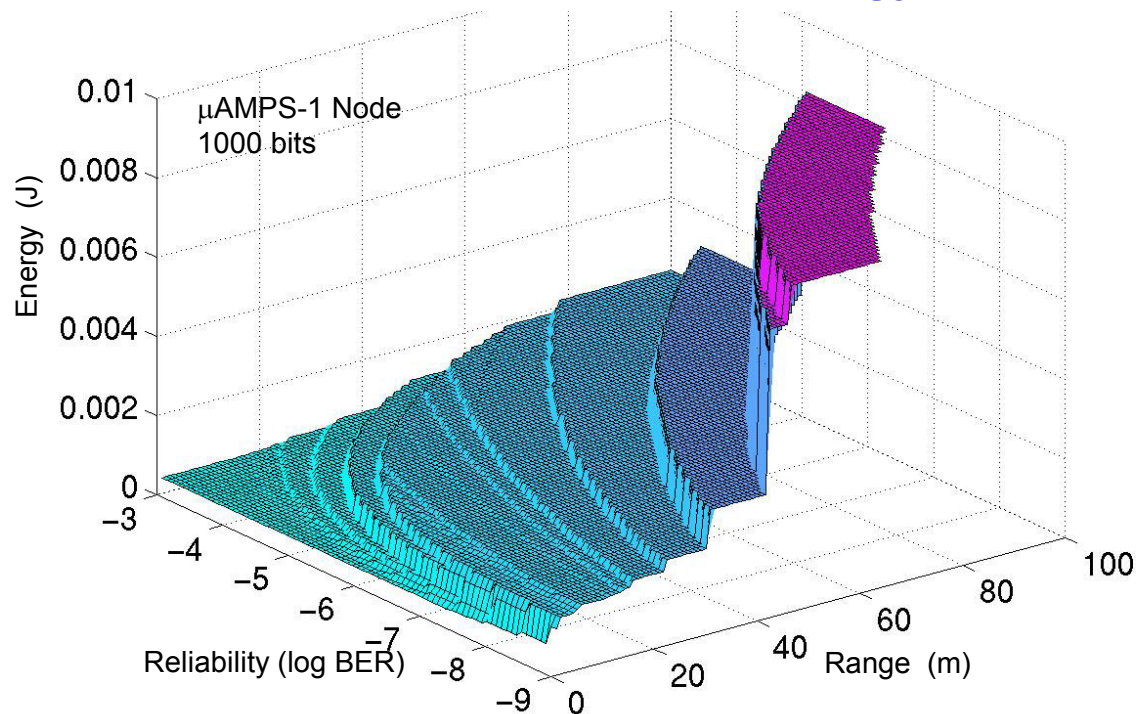
Radiated Power



Convolutional Code



Total Communication Energy



Energy scales gracefully with communication quality



Conclusions



- Exciting new applications enabled by a network of low-power wireless sensing devices
- Power Aware Design Methodology supersedes Energy Efficient Design
- ***Slower is Better*** – exploit sub-threshold operation as fastest switching speed is not needed
- ***Communication-centric design***
 - Energy per operation (mW/MIPS) will scale with technology
 - Communication costs (nJ/bit) will not scale at the same rate

Low Energy Sensor Design Requires a System-level Approach – Tight Coupling Between Fabrics, Algorithms and Protocols