A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS

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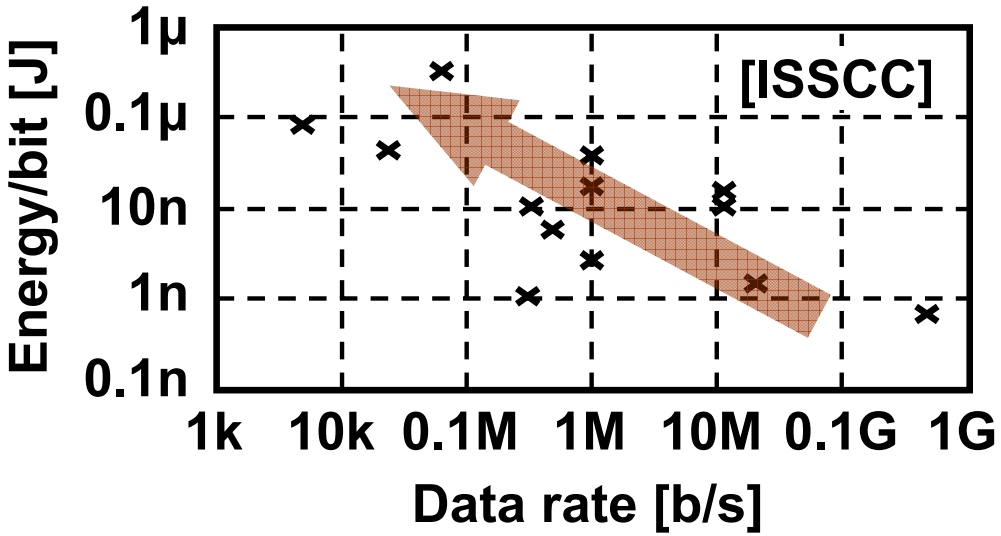
Motivation

- **Low-data rate, energy-constrained apps.**

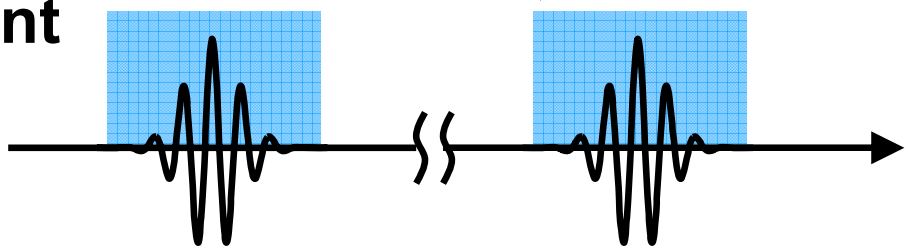


Trend:
Data rate ▼
Energy/bit ▲

- **Pulsed-UWB signaling inherently duty-cycled**

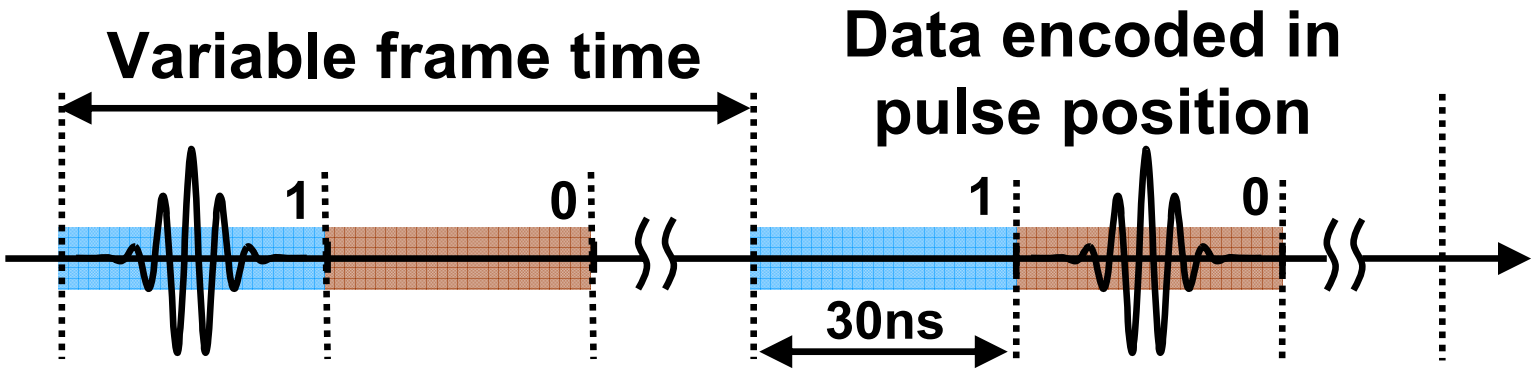
TX and RX on only when a pulse is present

Fast (2ns) turn-on time

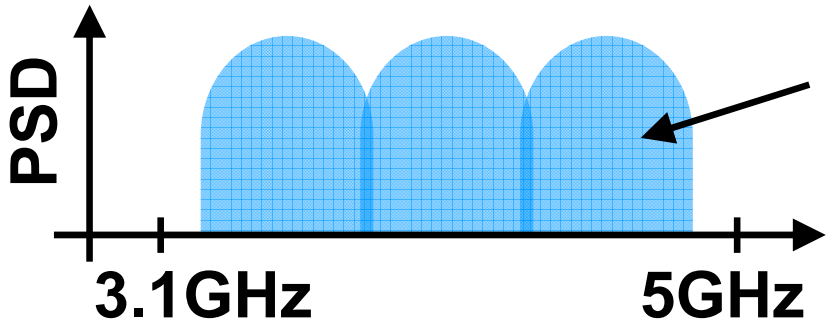


System Specifications

- PPM signaling with non-coherent receiver



- Three channel frequency plan



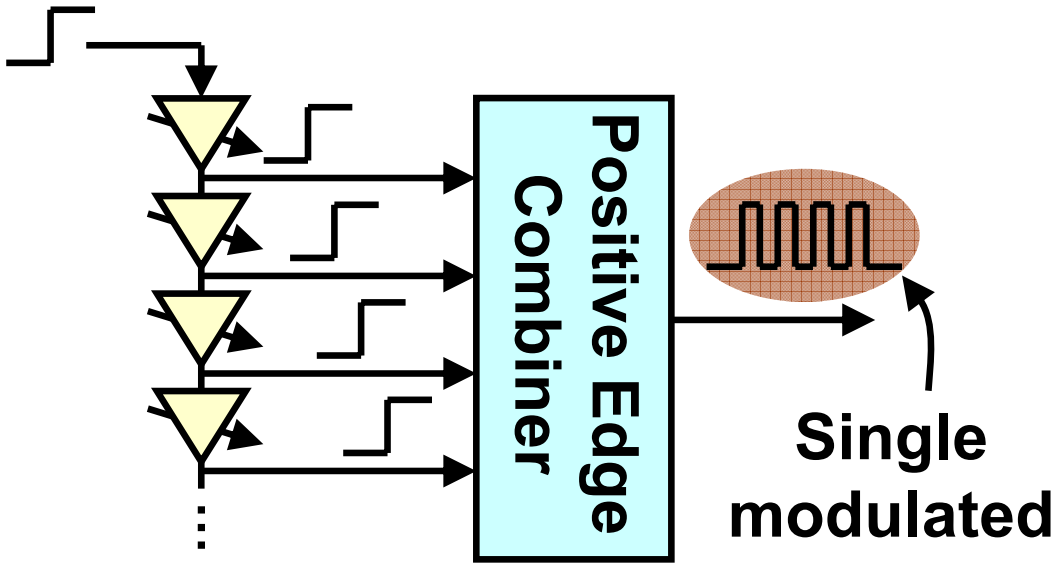
Each channel 550MHz wide

Center frequency: 6000ppm

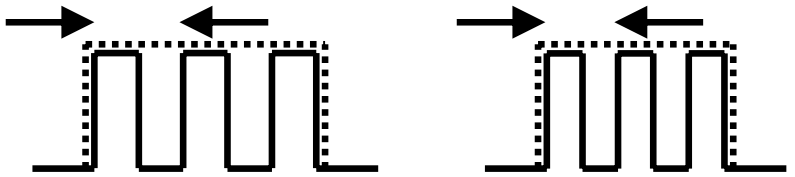
Self-mixing receiver → Relaxed RF tolerance → **All-Digital Transmitter**

Pulse Generation Principle

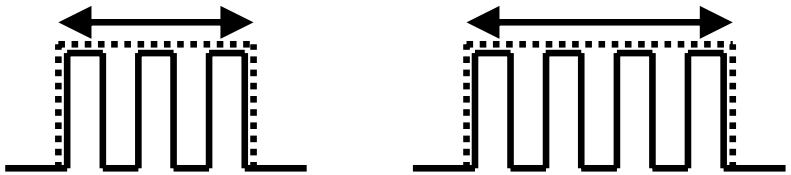
- Use a tapped variable delay line and edge combiner to synthesize a pulse



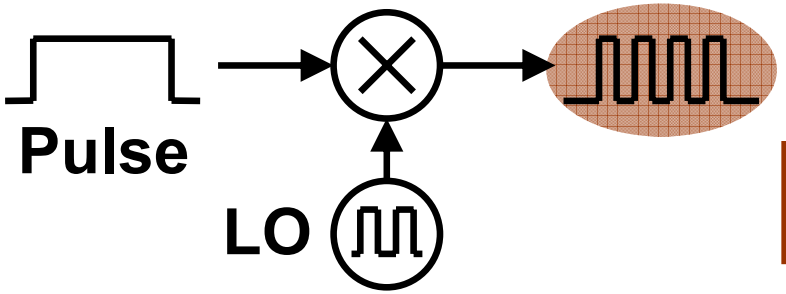
Center frequency depends on delay



Width depends on number of edges combined

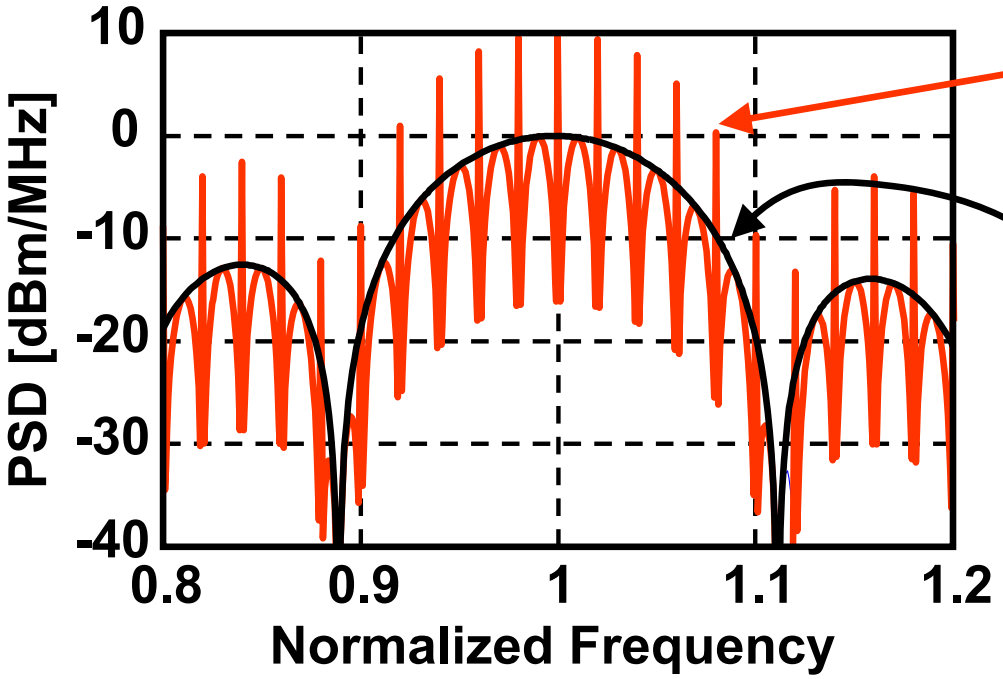


Equivalent to…



Frequency selectivity without LO

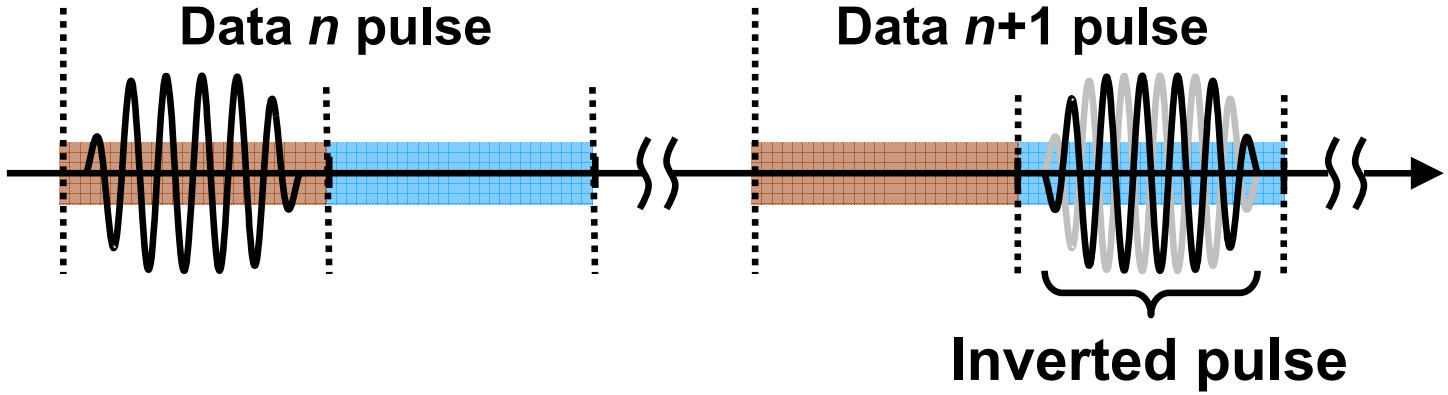
Spectrum cSarbmlgin



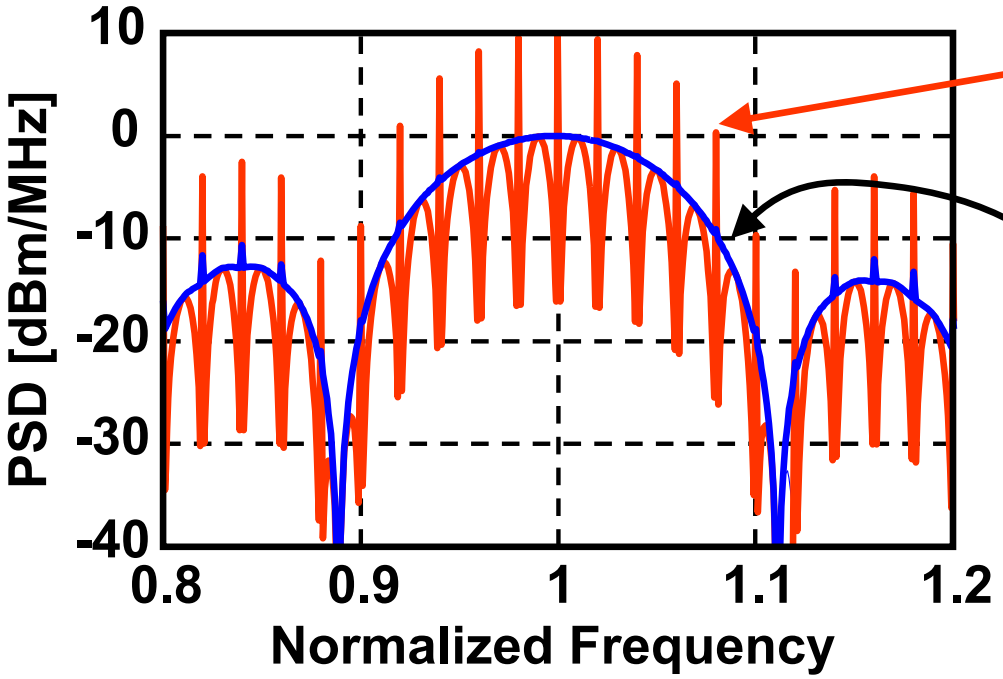
Randomly modulated PPM signals have spectral lines

PPM+BPSK scrambling eliminates tones

Conventional PPM+BPSK



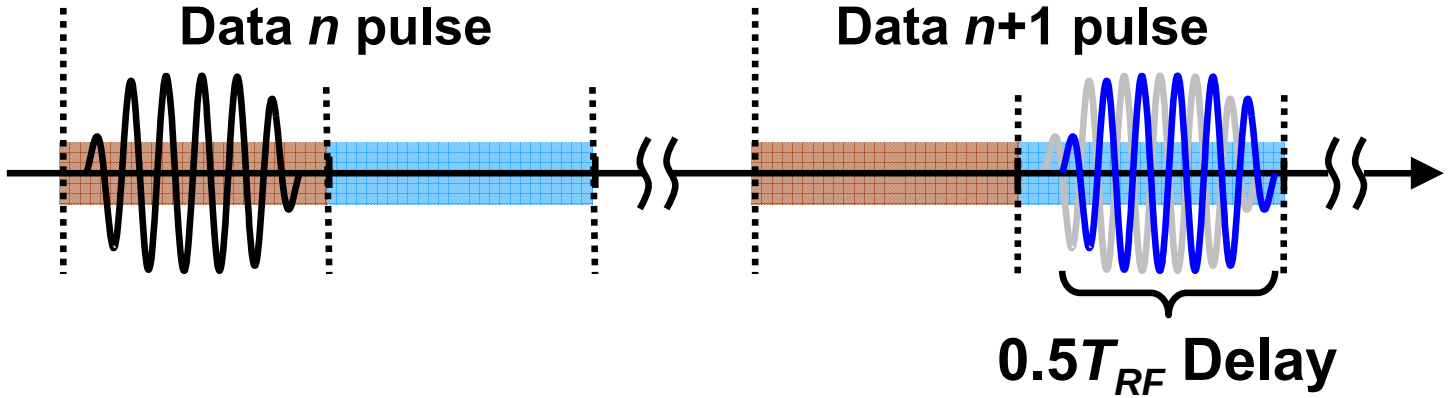
Spectrum cSarbmlgin



Randomly modulated PPM signals have spectral lines

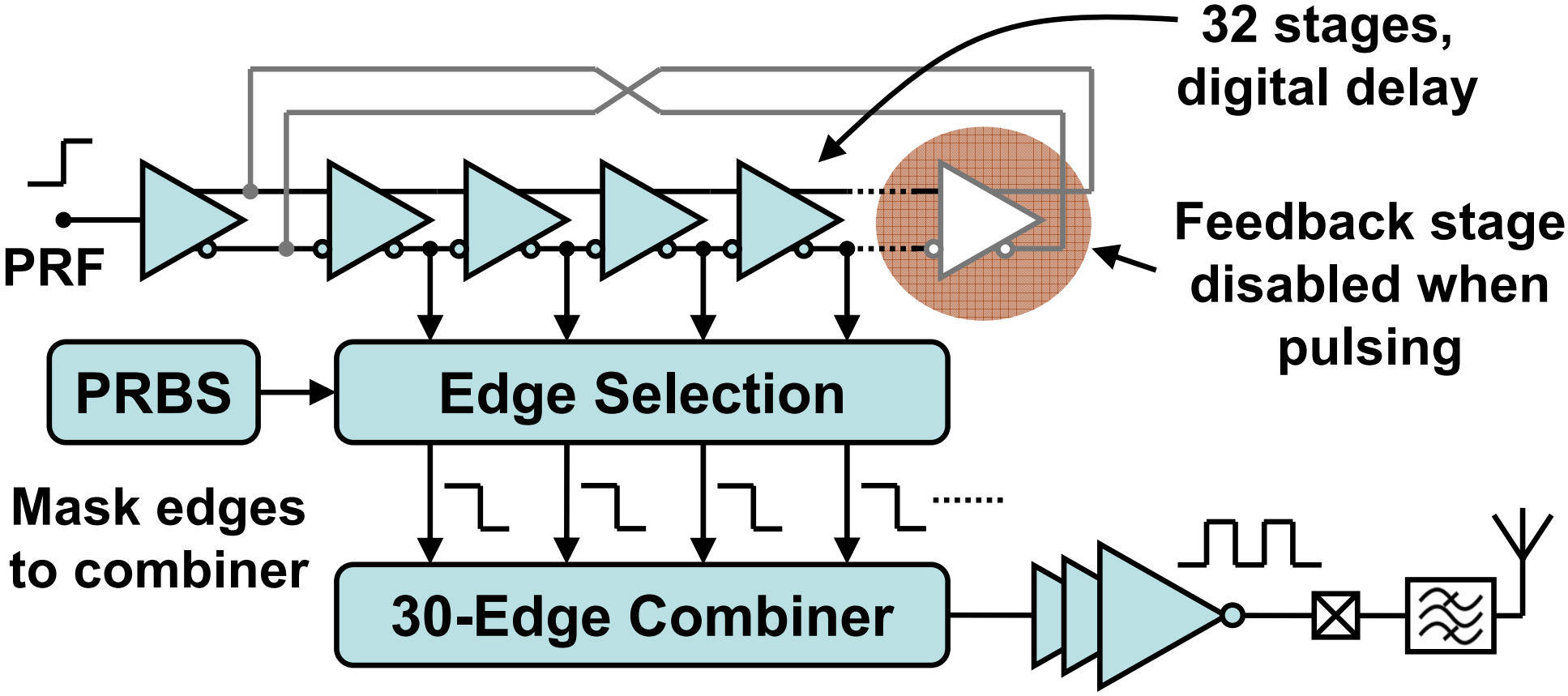
PPM+Delay-Based BPSK scrambling eliminates tones in the main lobe

Proposed PPM+DB-BPSK



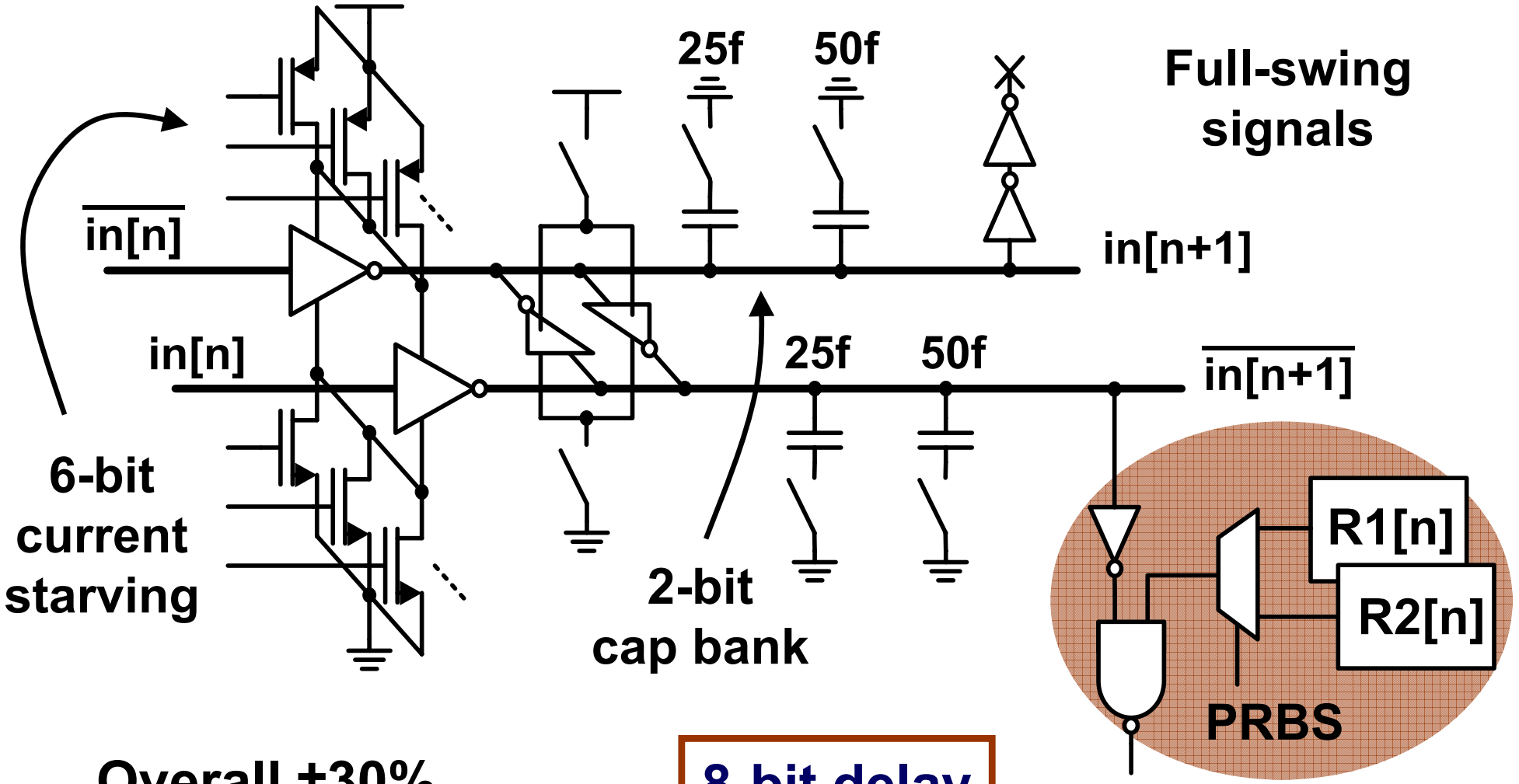
DB-BPSK: Minimal Overhead

Transmitter Block Diagram



Positive edge in ► one RF pulse out

Digital Delay Stage

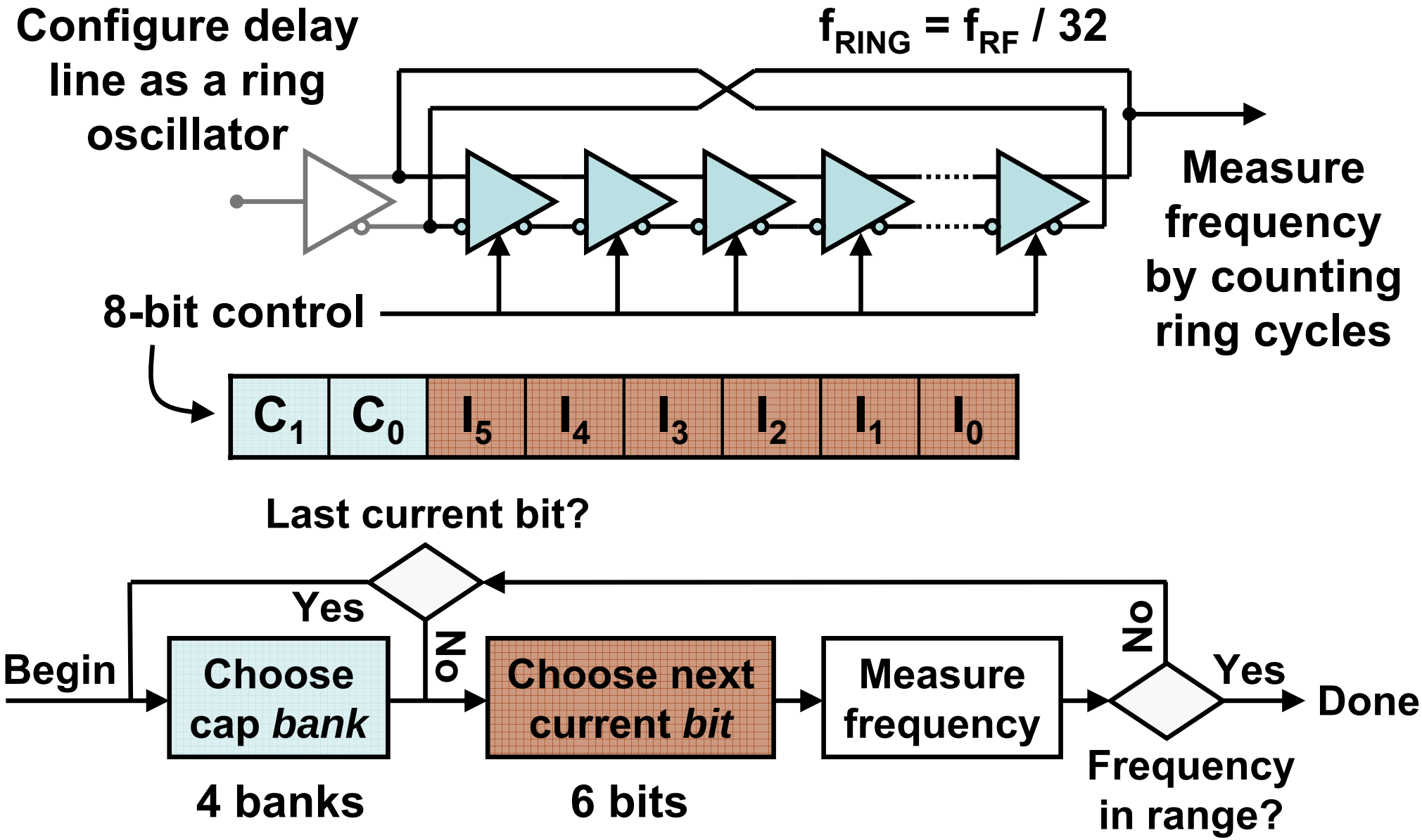


Overall ±30% variation in delay

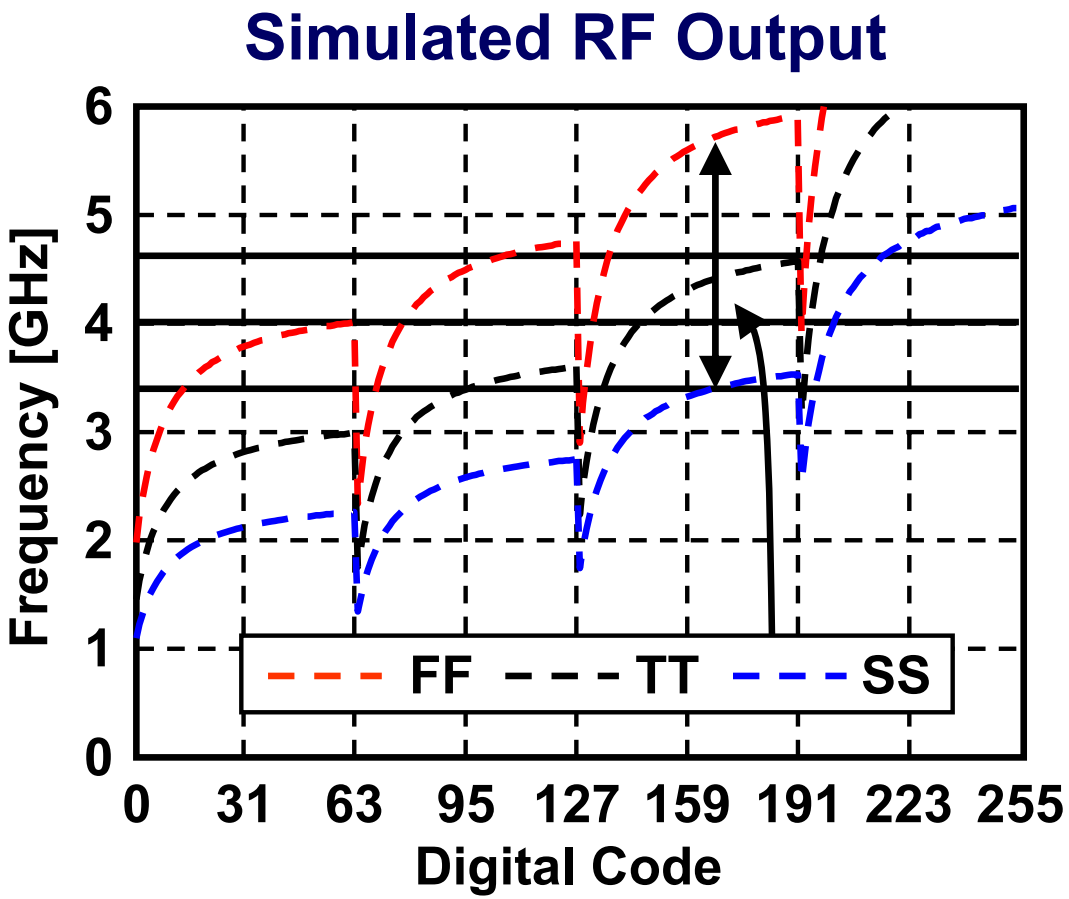
→ 8-bit delay control

Only selected edges are combined

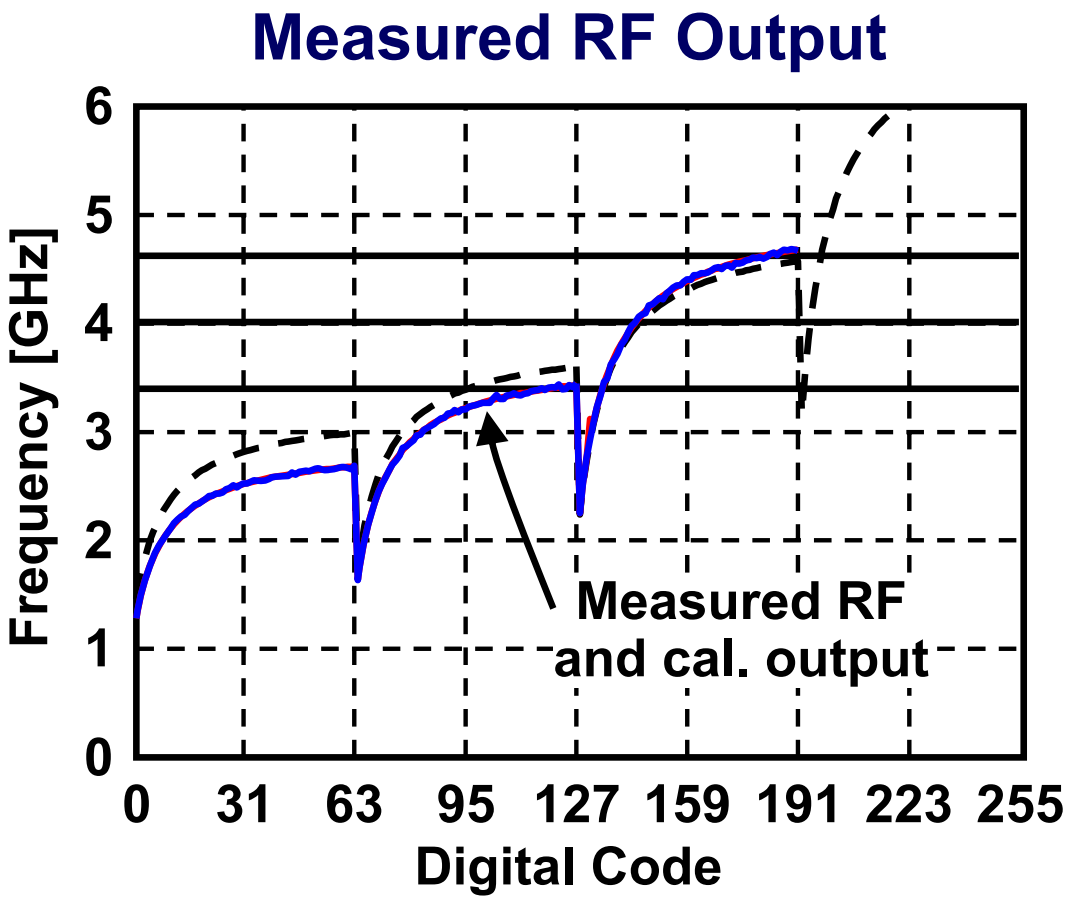
Delay Line Calibration

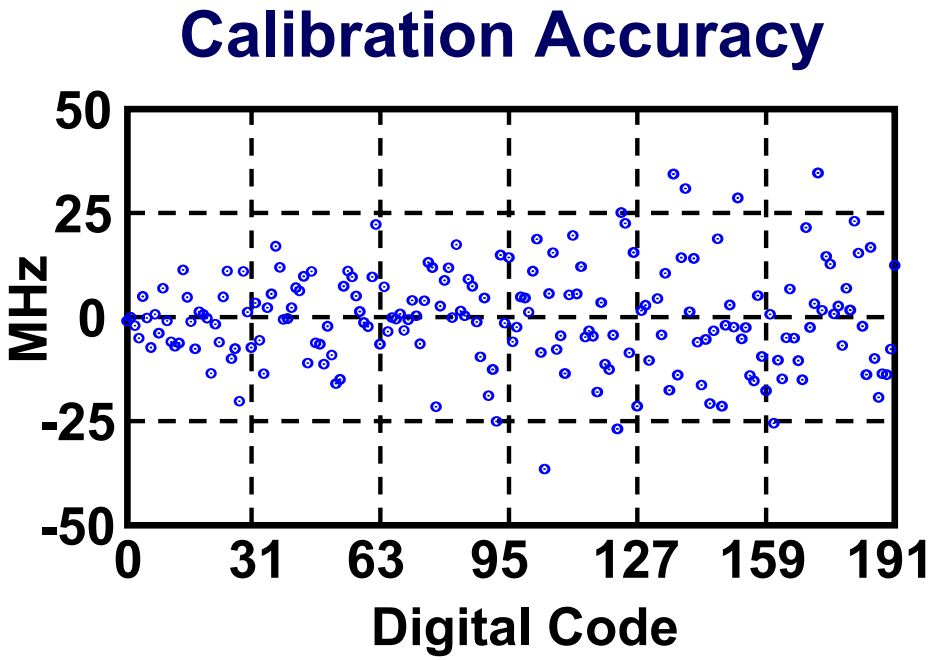


Delay Range and Accuracy



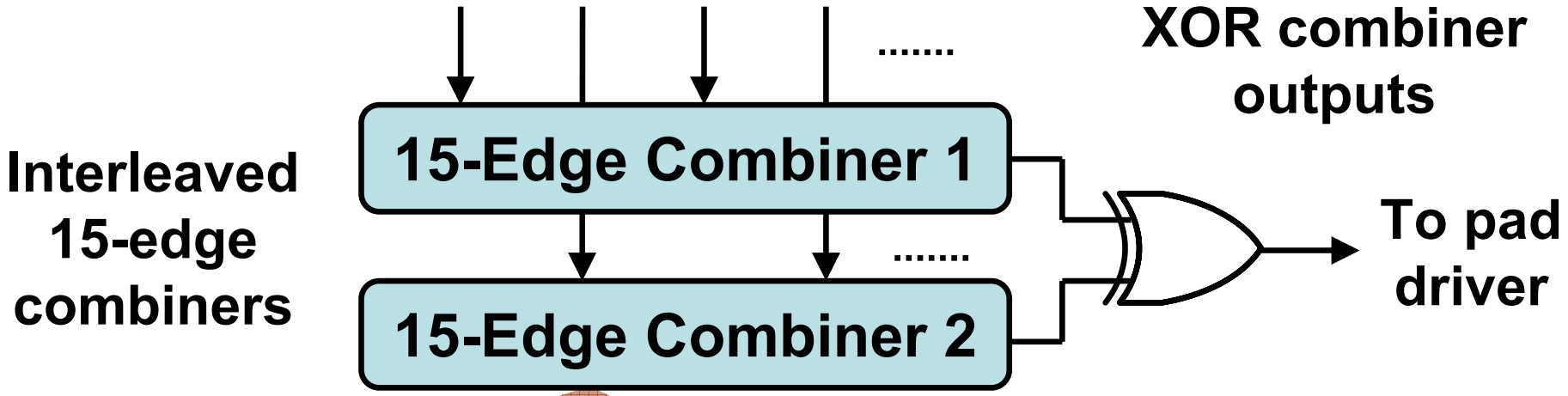
Delay Range and Accuracy

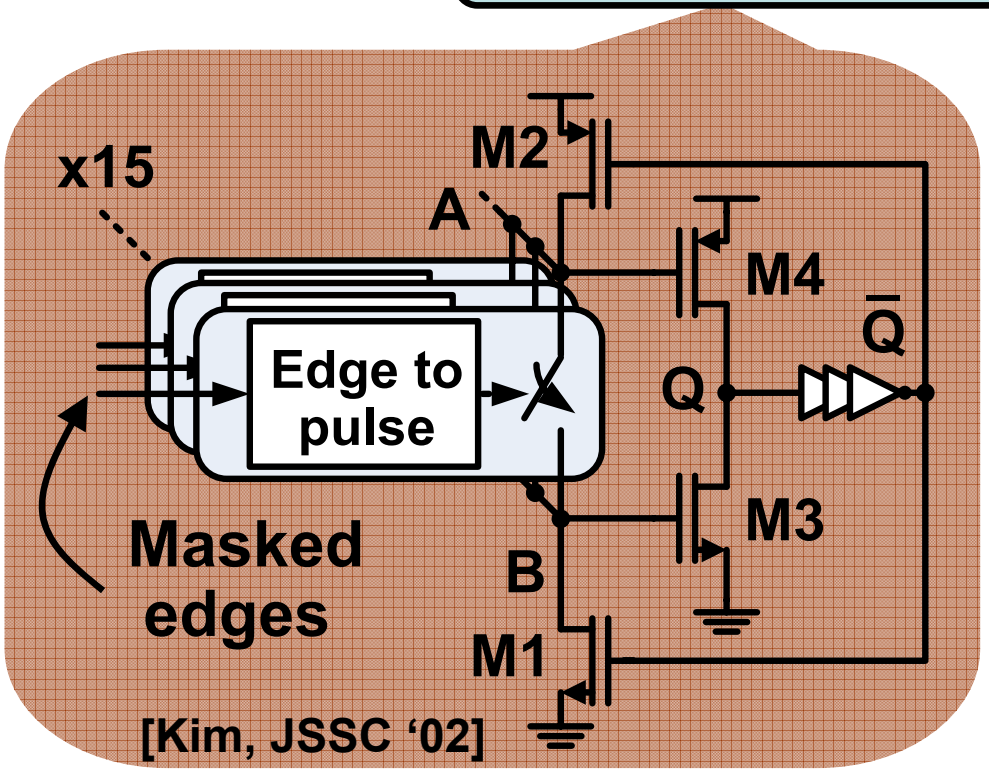


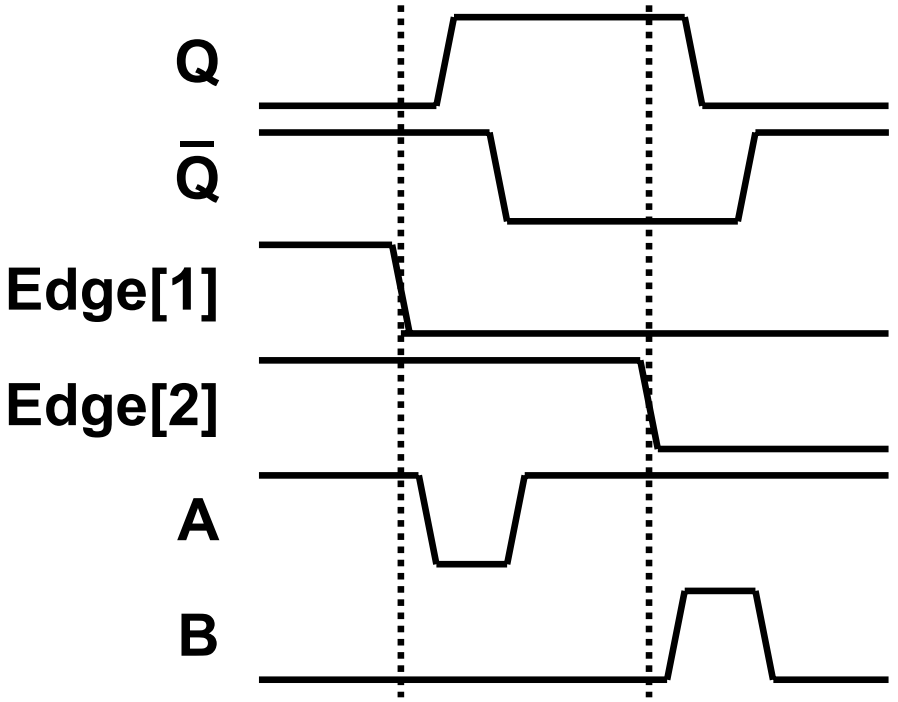


Ring output is an accurate measure of pulse center frequency

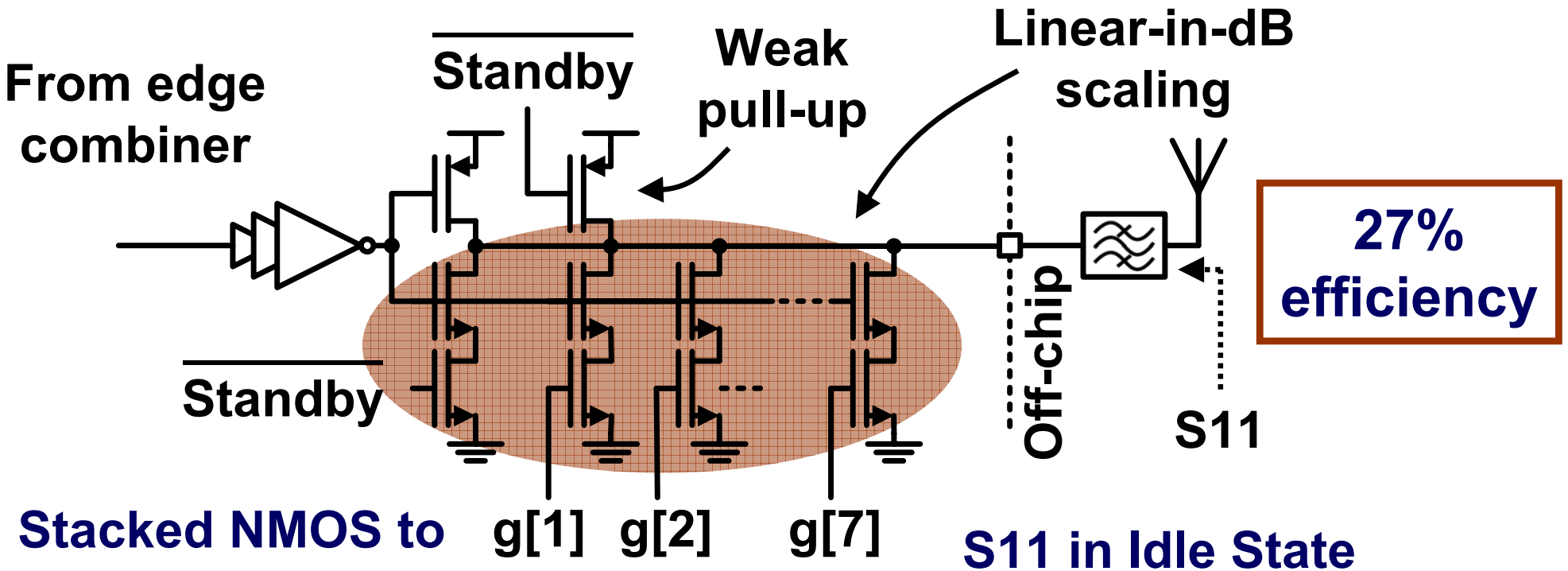
30-Edge Combiner





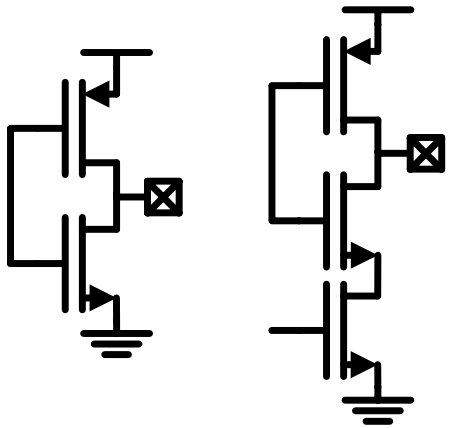


RF Pad Driver

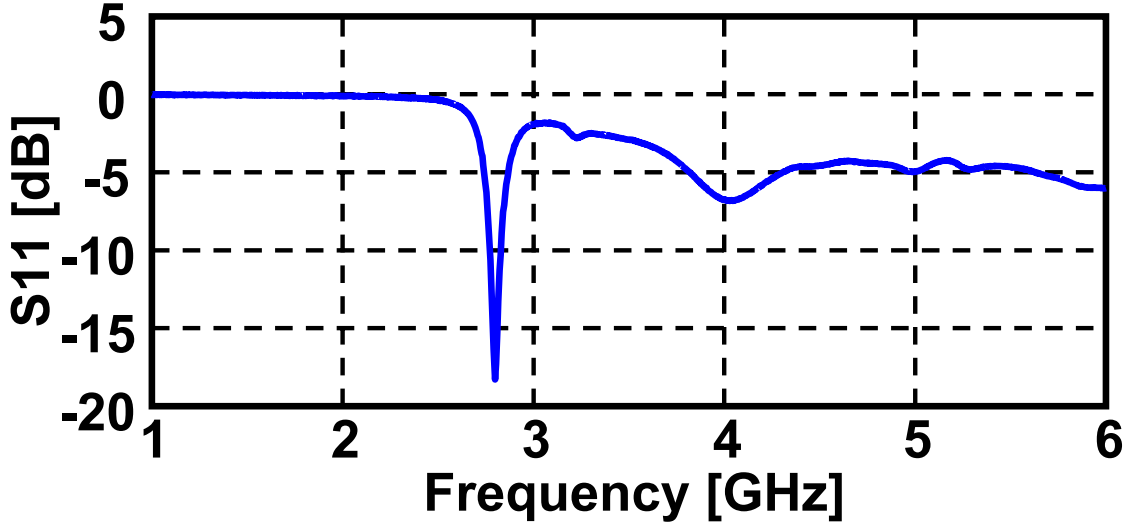


27% efficiency

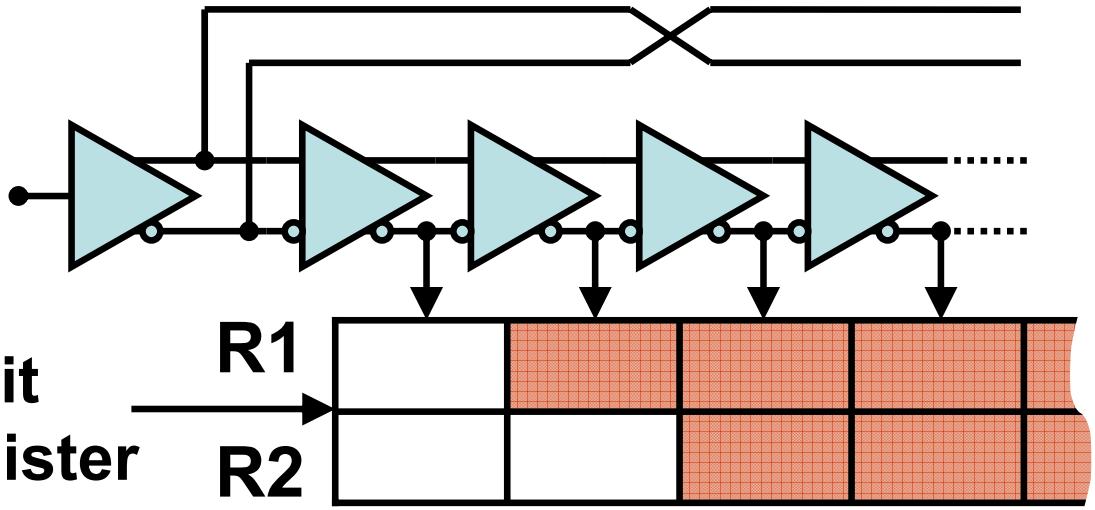
Stacked NMOS to reduce leakage



S11 in Idle State



DB-BPSK Implementation

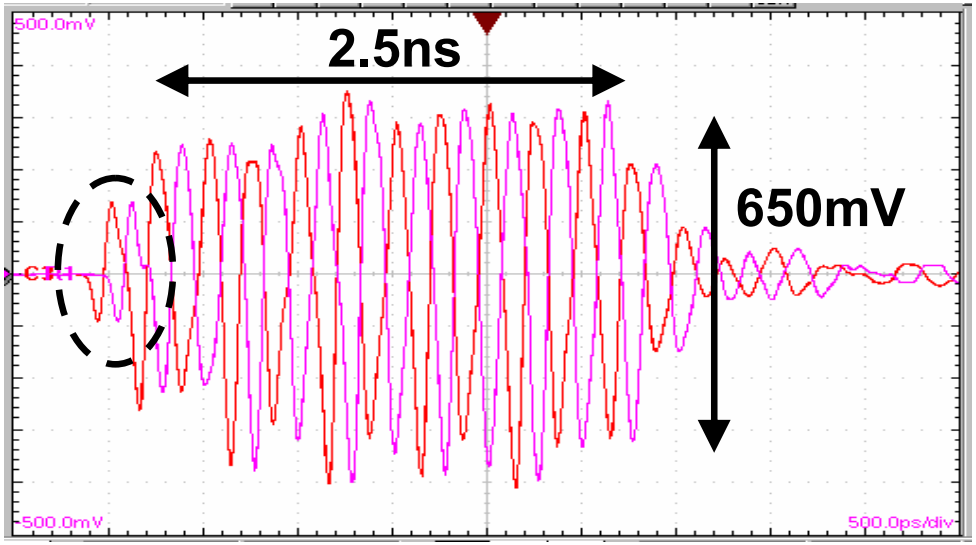


PRBS bit selects register

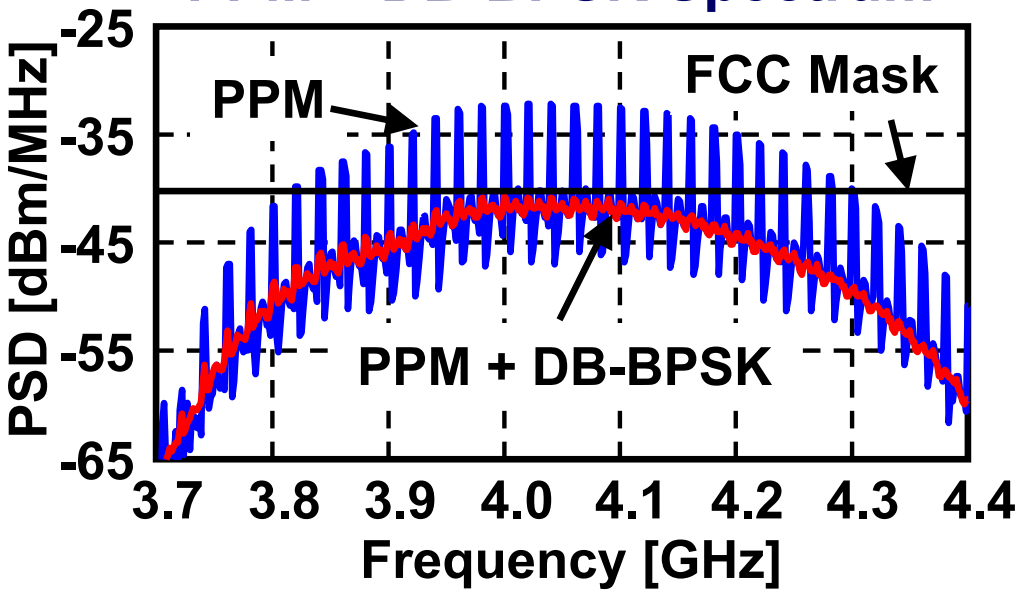
Per-stage delay is ½ RF period

Mask values offset by 1 bit

DB-BPSK Pulses

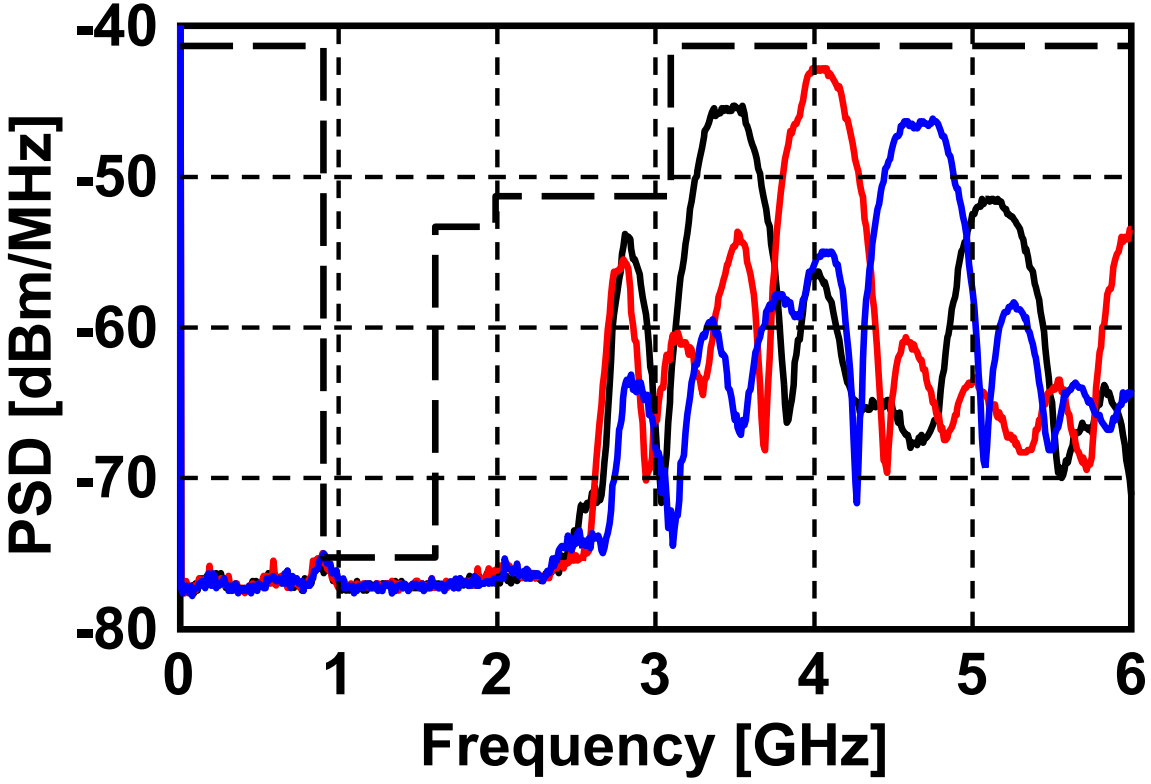


PPM + DB-BPSK Spectrum

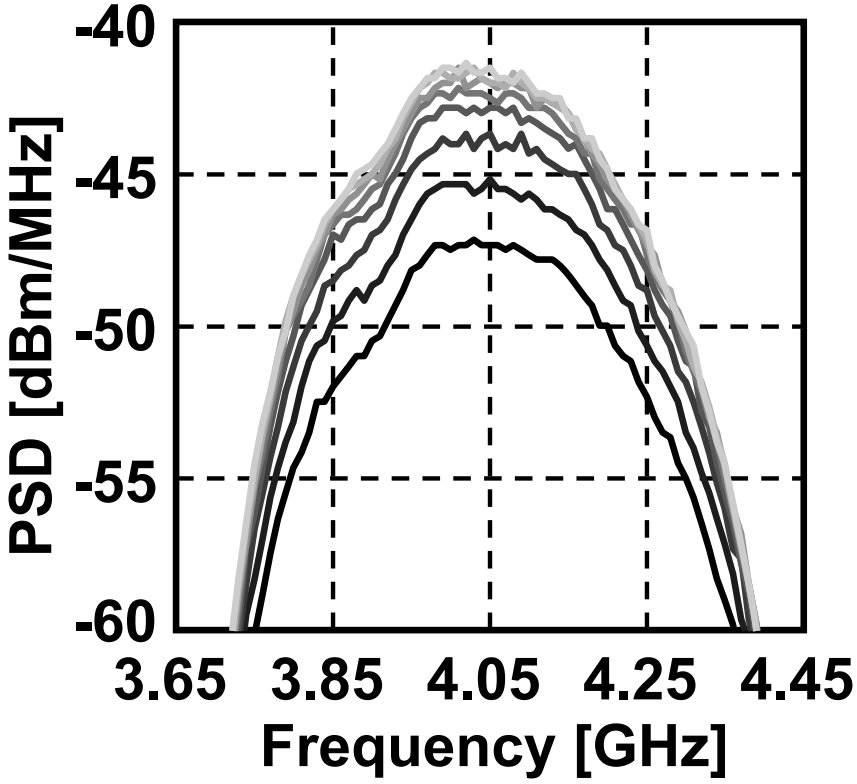


Measured Spectrum

3-Channel Spectrum

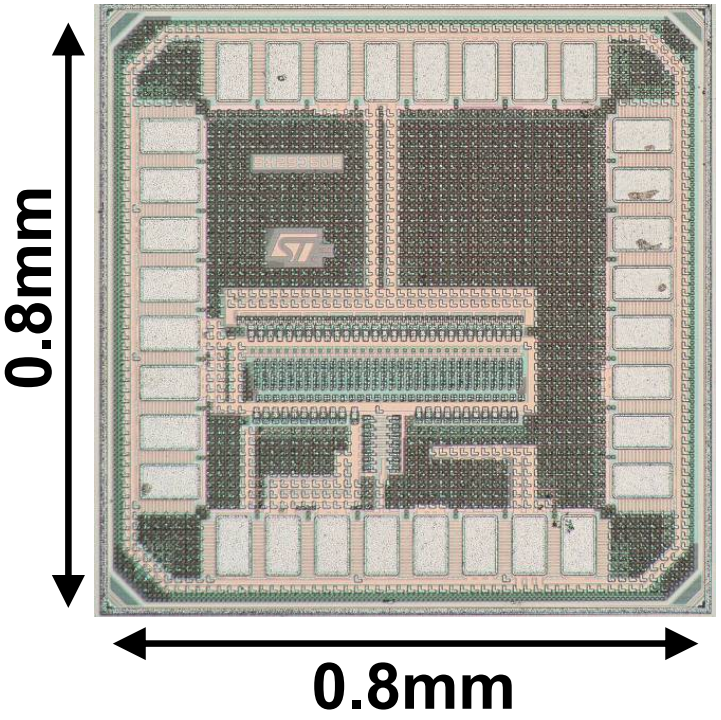


CH2 Gain Settings



Summary

Technology	90nm CMOS
Active Area	0.2x0.4mm^2
Modulation	PPM
Scrambling	DB-BPSK
Supply	1V
Leakage Power	96µW
Active E/pulse	37pJ/pulse
PRF Range	10kHz to 16.7MHz
Total E/bit	9.6nJ/bit to 43pJ/bit



- Energy consumed in sub-V_t leakage and CV^2
- Digital architecture practical for non-coherent RX

Acknowledgements – MARCO/DARPA Focus Center for Circuit & System Solutions (C2S2), National Science Foundation (NSF), and STMicroelectronics for chip fabrication