MichiganEngineering

IR-UWB Transmitters Synthesized from Standard Digital Library Components

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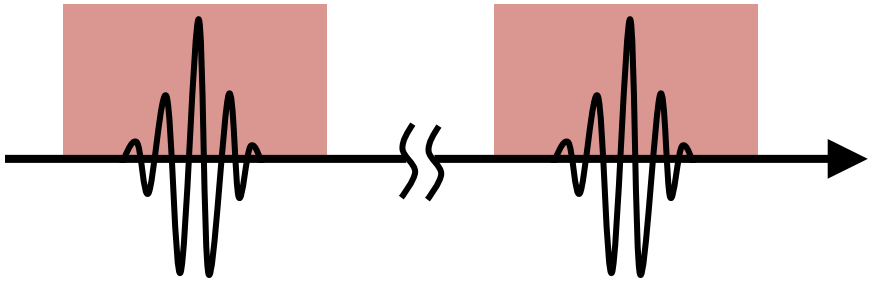
Motivation

- Digital circuits take more advantages of process scaling
- Digitally-assisted / digitally-intensive circuits replace conventional analog circuits
- IR-UWB communication is ideal for all-digital transmitter architectures
- UWB Transmitter with fully automated design flow

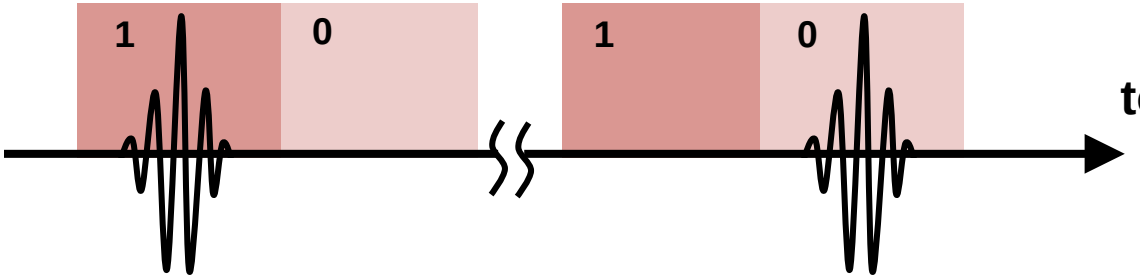
UWB Pulses & Modulation

- **IR-UWB signaling inherently duty-cycled**



Digital circuits can be off between pulses, minimizing power consumption

- **PPM signaling with non-coherent receiver**

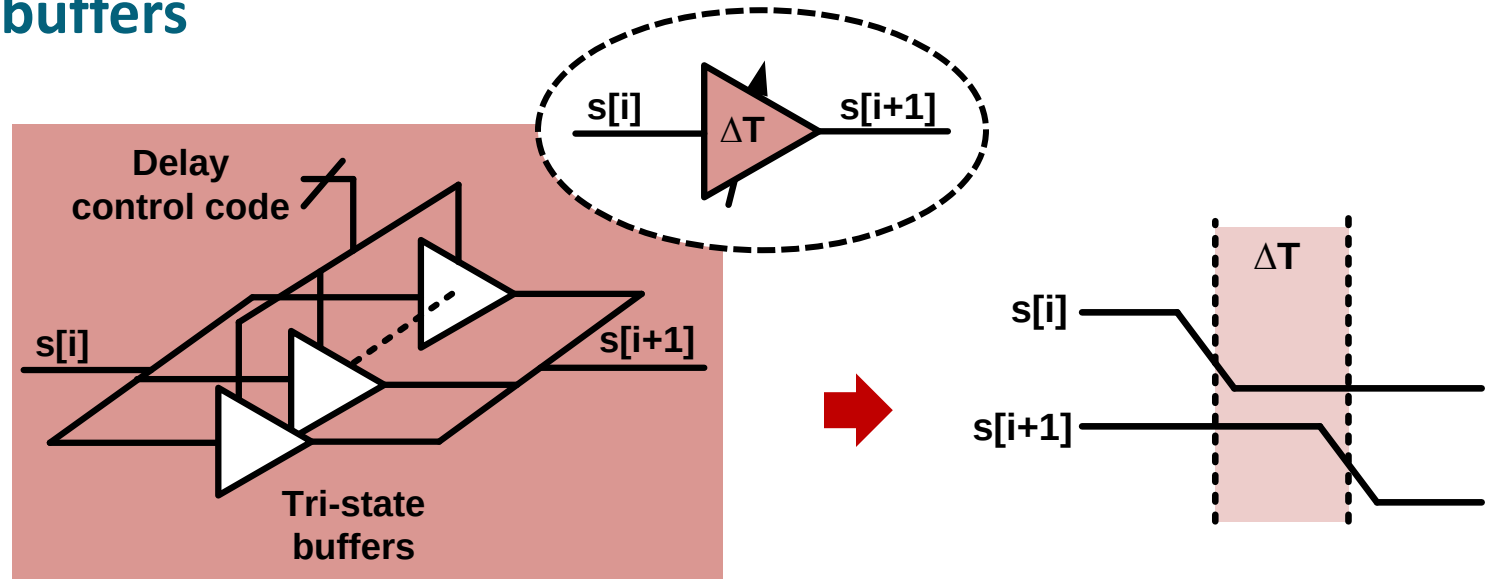


Relaxed frequency tolerance is affordable for digital circuits

Favorable to all-digital architecture

Tunable Delay Cell

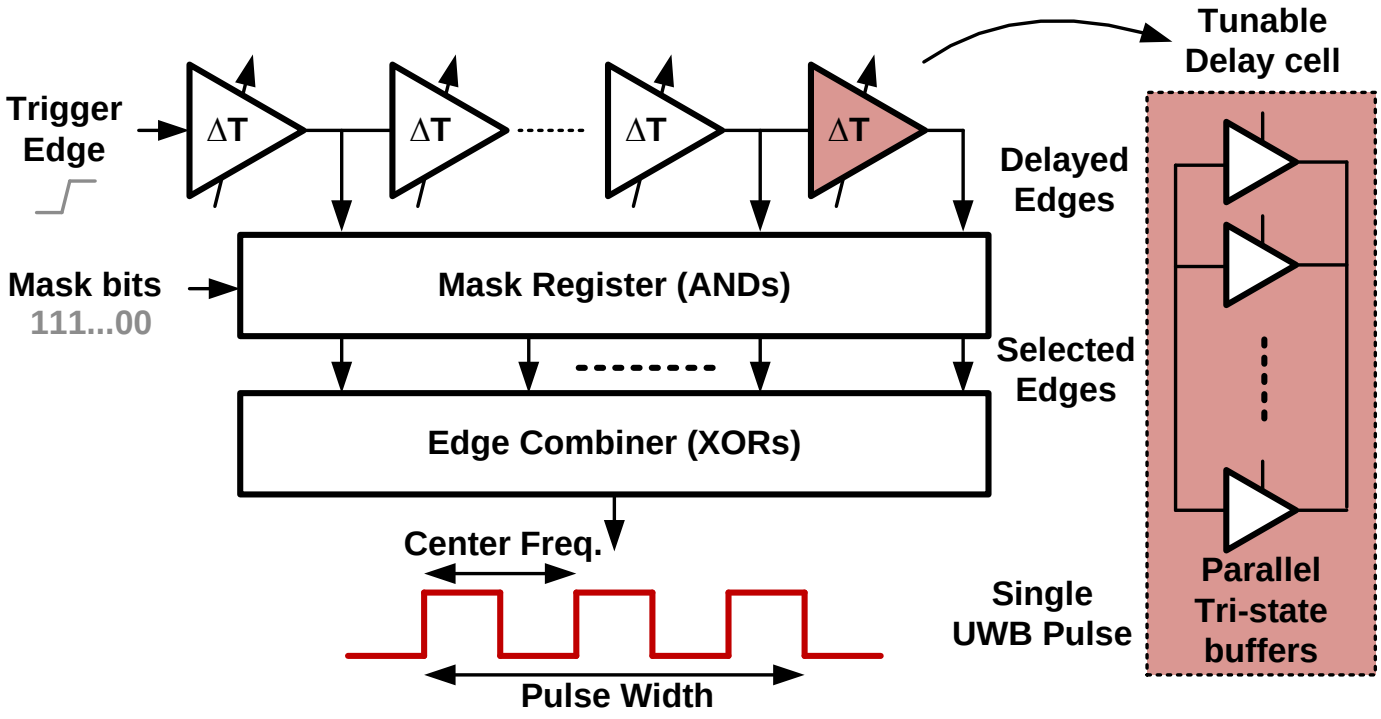
- **Delay tuned by digital code**
  - **Implemented with digital logic cells**
  - **Tuning range and resolution determine by number of buffers**



Digital building block for analog function

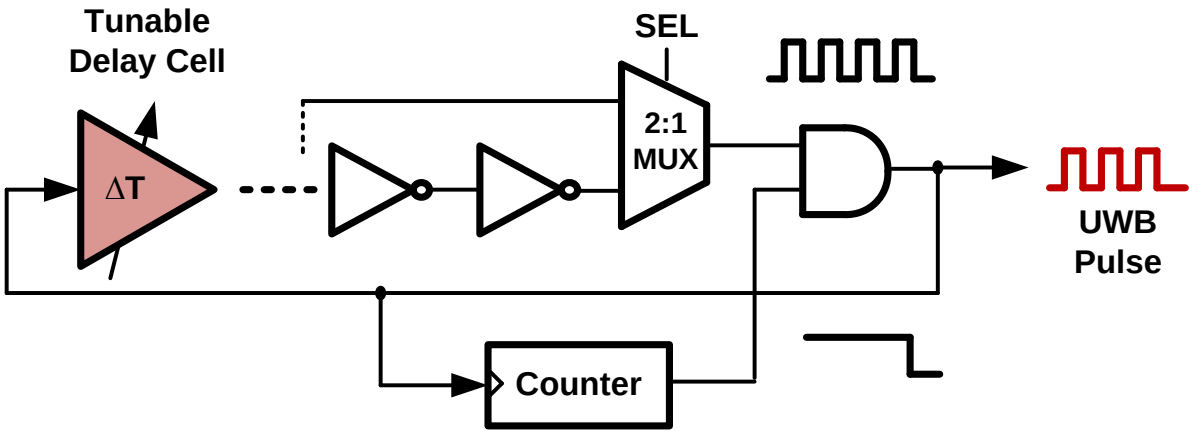
Delay Line Pulse Generator

- **Combine delayed edges to generate pulse**
  - **Center frequency controlled by delay cells**
  - **Pulse width controlled by selecting edges**



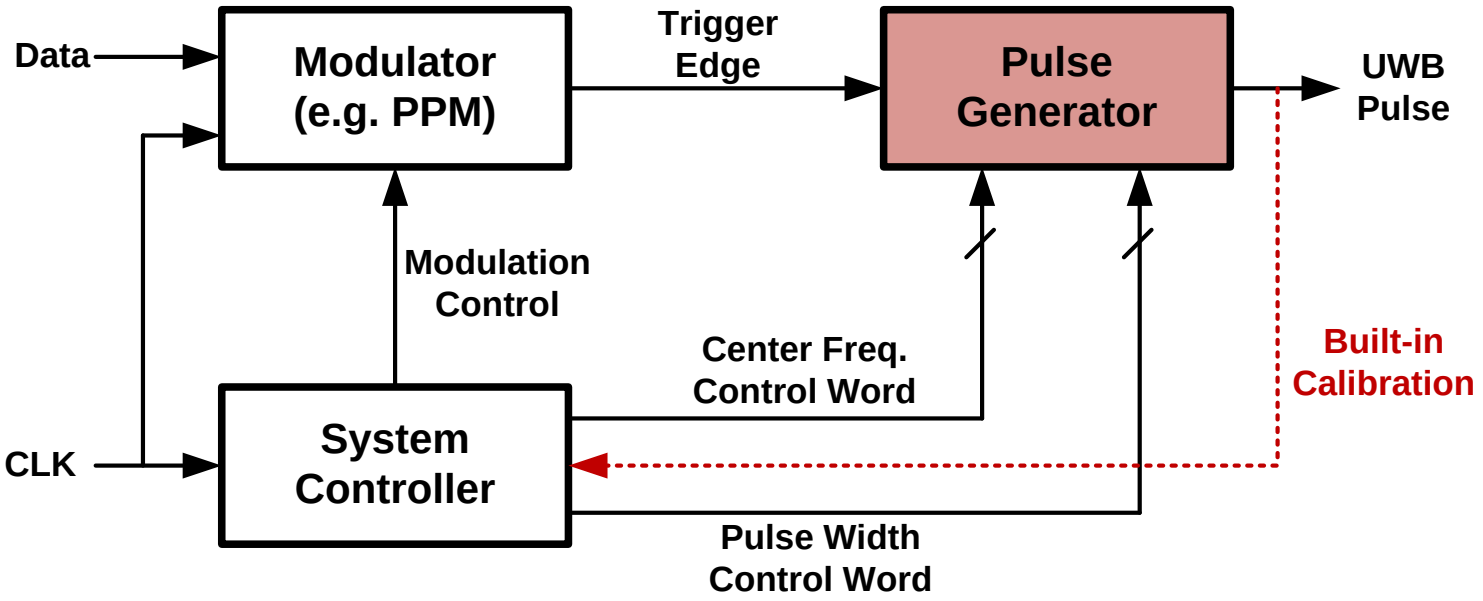
Ring Pulse Generator

- **Ring structured pulse generator**
  - **Center frequency controlled by delay cell and MUX**
  - **Pulse width controlled by counting cycles**



Transmitter Block Diagram

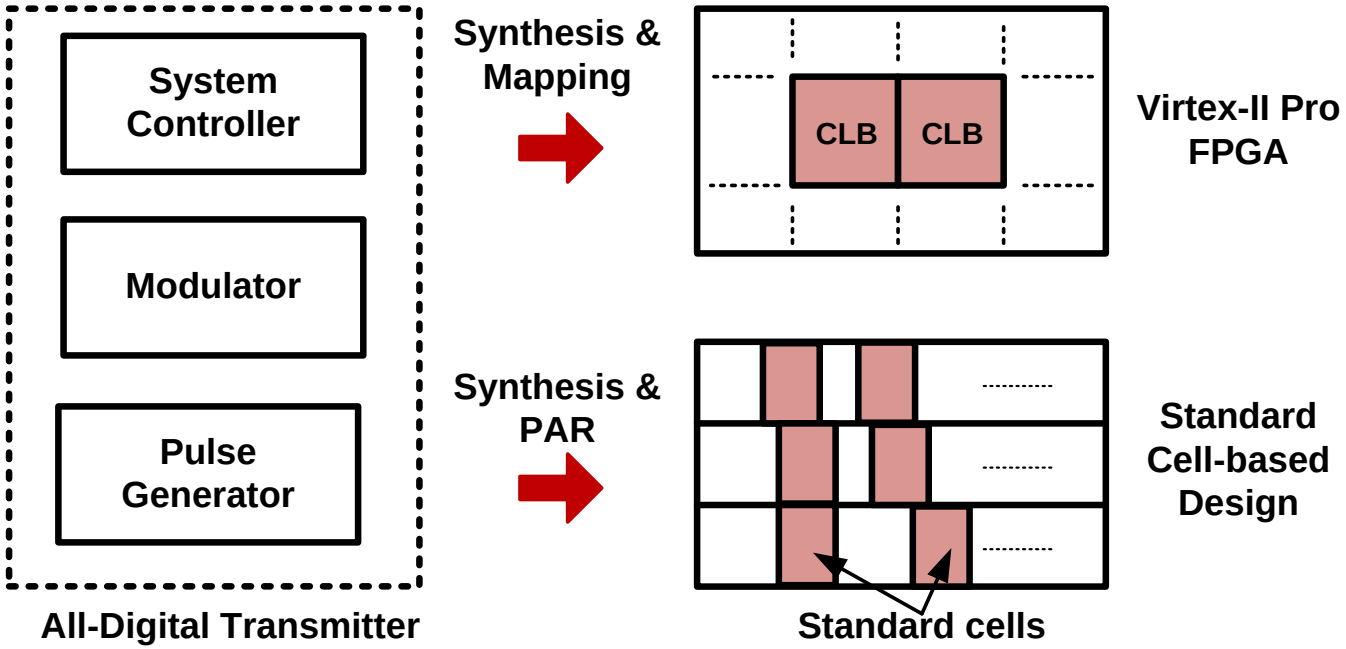
- **Build transmitters with proposed pulse generators**
  - **System controller, modulator also digital logic blocks**



Synthesizable Transmitter

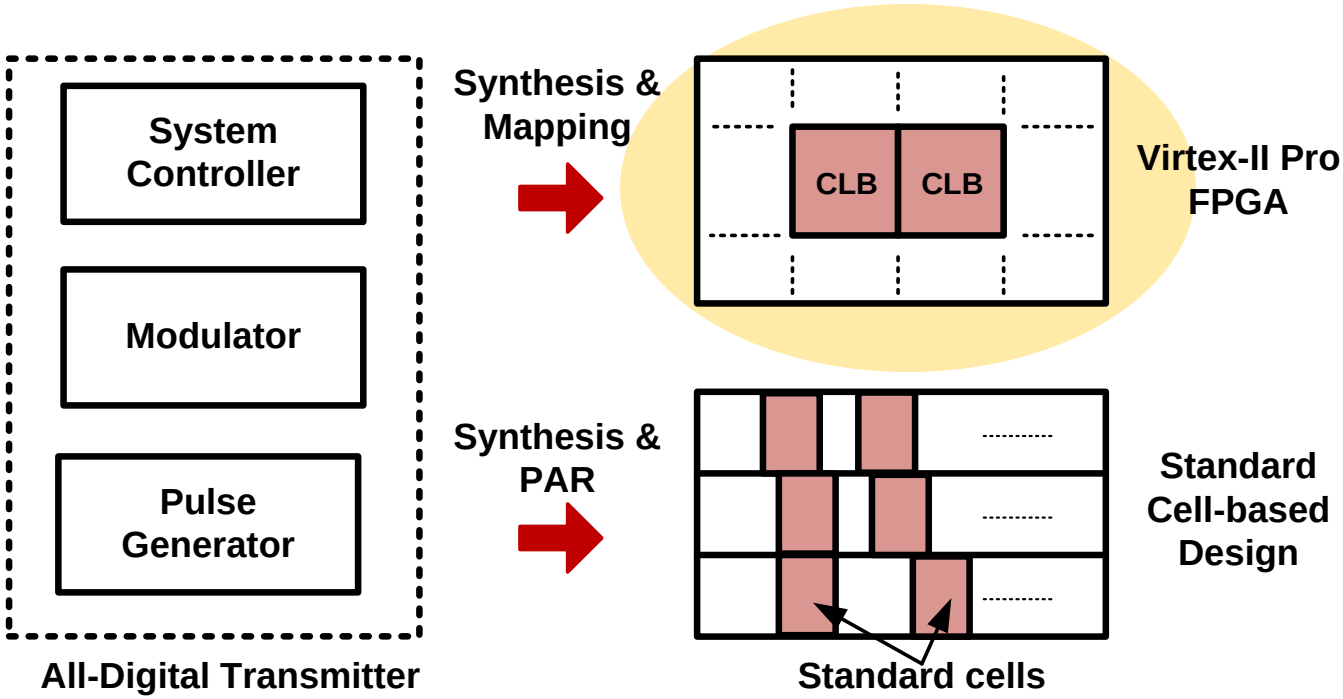
Synthesizable Transmitter

- **Take advantage of current automatic design tools**
  - **Portability and Scalability**
  - **Benefits from process scaling**



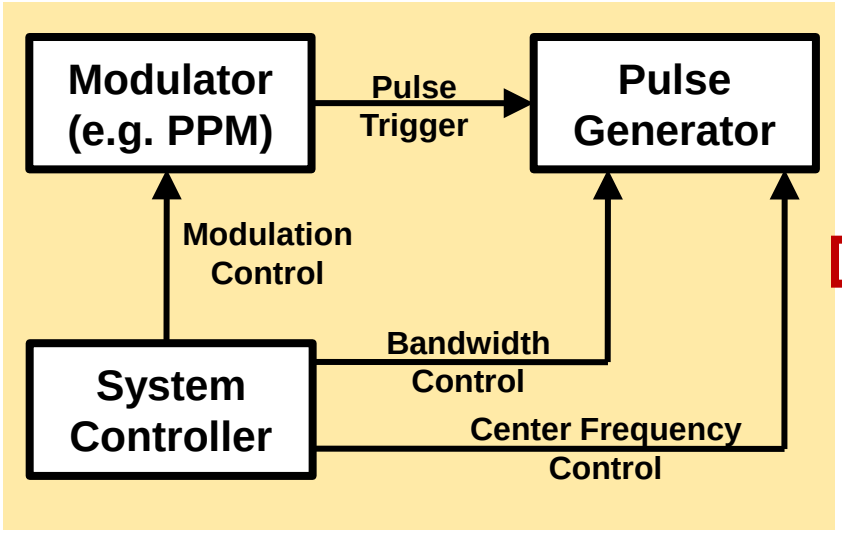
Synthesizable Transmitter

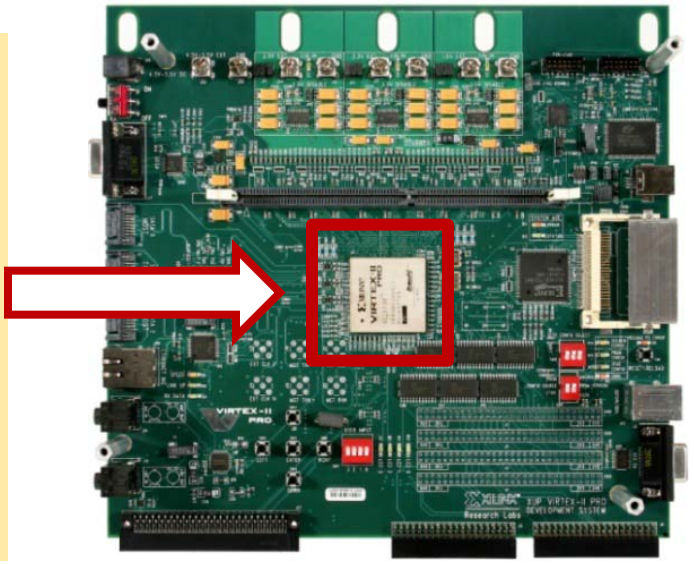
- **UWB transmitters in FPGA**



FPGA Prototype

- **Automated FPGA design flow**
  - **Mapped to configurable logic blocks and TBUF cells**



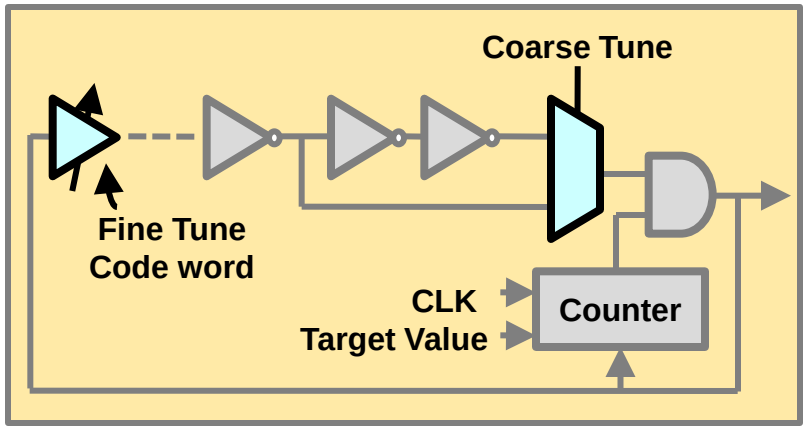


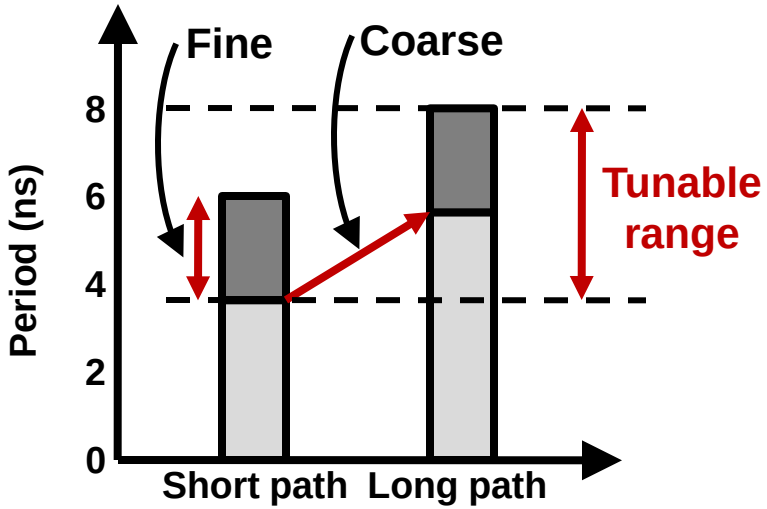
Xilinx Virtex-II Pro FPGA
Development board

Verification of synthesizable transmitter

Calibration of Pulse Generator

- **Ring pulse generator**
  - **Coarse / fine calibration to obtain large range**

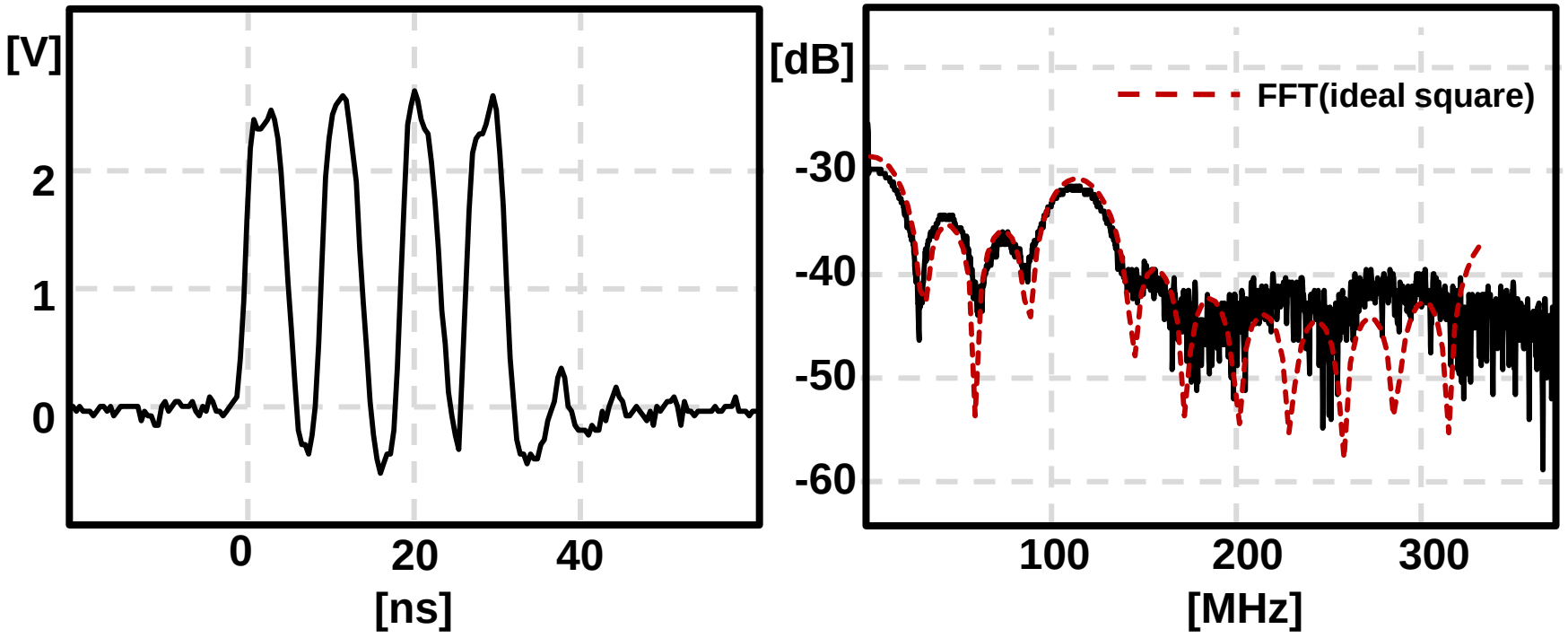




Automatic PAR requires calibration

Measured Pulse & Spectrum

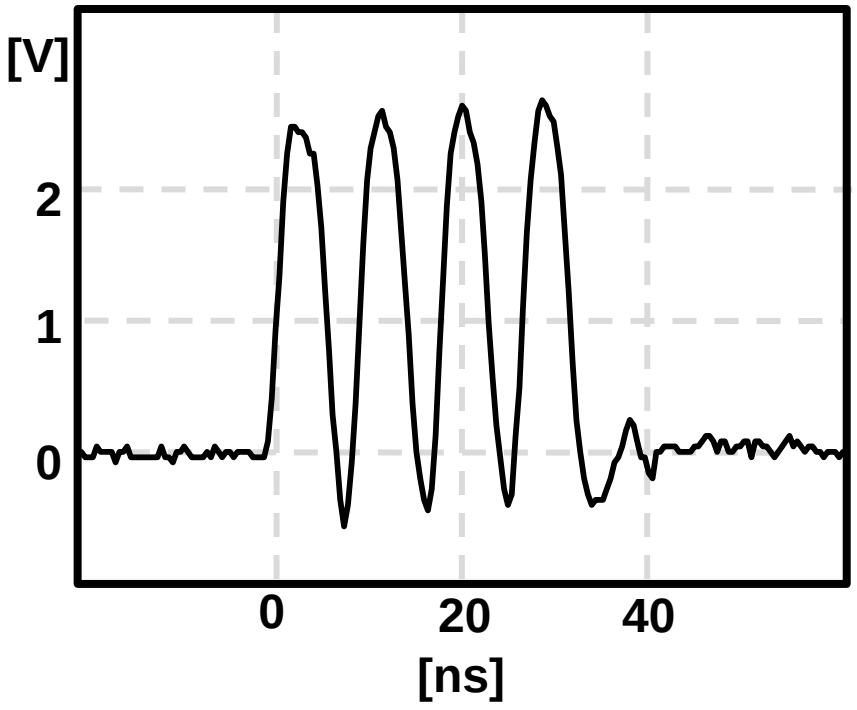
- Delay line pulse generator in FPGA prototype

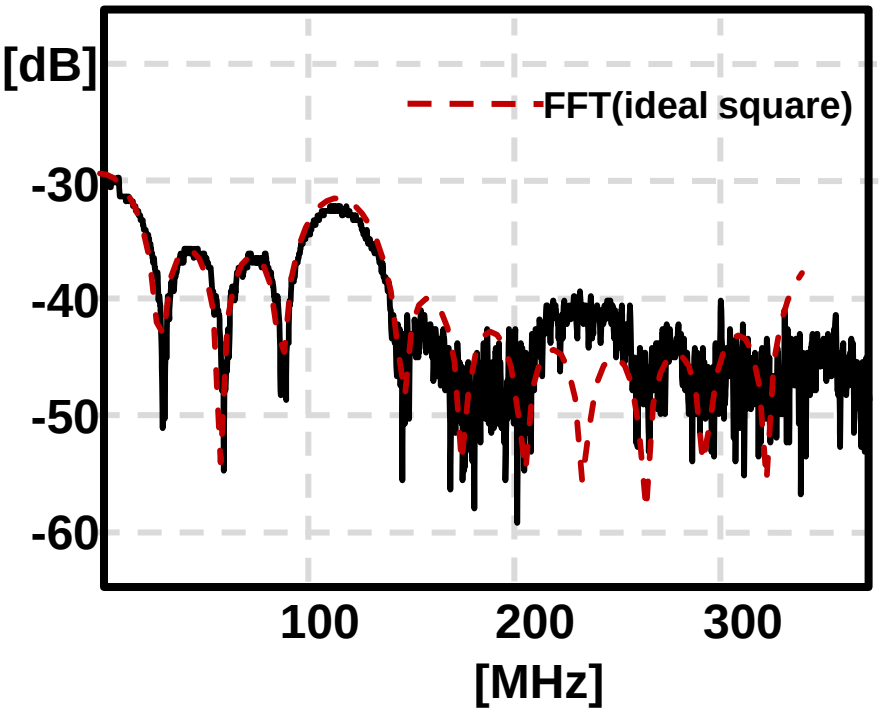


Satisfies FCC fractional requirement

Measured Pulse & Spectrum

- Ring pulse generator in FPGA prototype

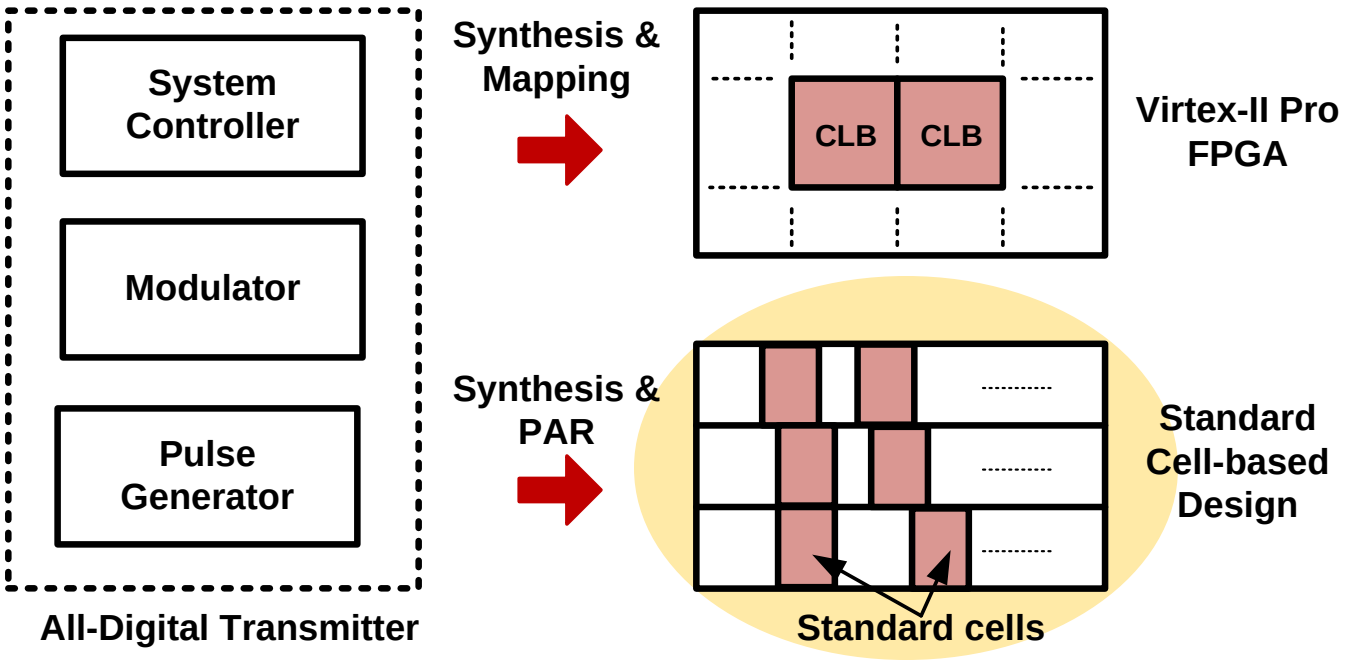




Satisfies FCC fractional requirement

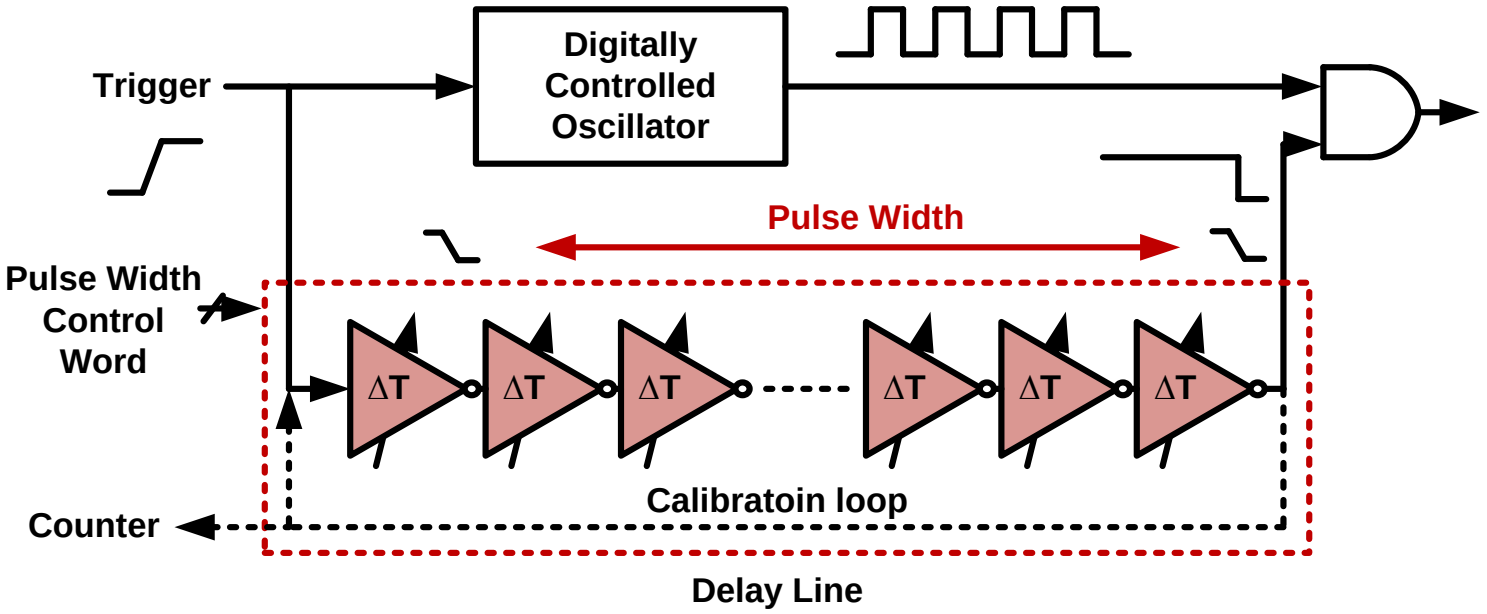
Transmitter in ASIC

- **UWB transmitter prototype in ASIC**



Pulse Generator in ASIC

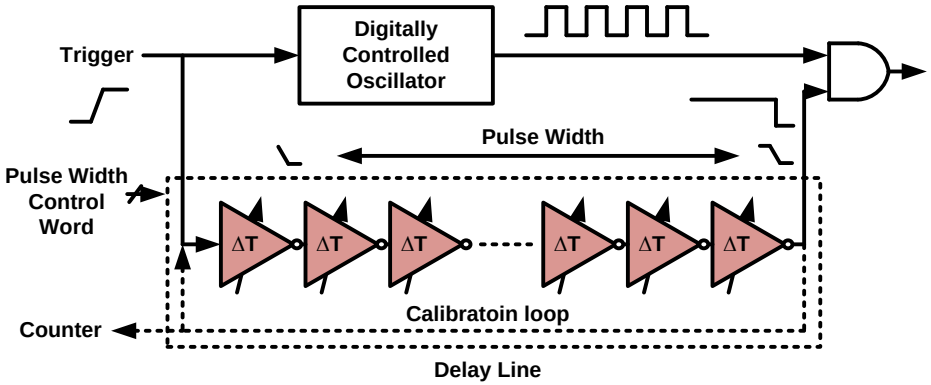
- **Tunable delay cells applied to DCO and delay line**
  - **Center frequency controlled by DCO**
  - **Pulse width controlled by delay line**



Higher resolution for center frequency and bandwidth

Pulse Generator Operation

- Gate DCO output with pulse control edge
- DCO is turned off after gating output



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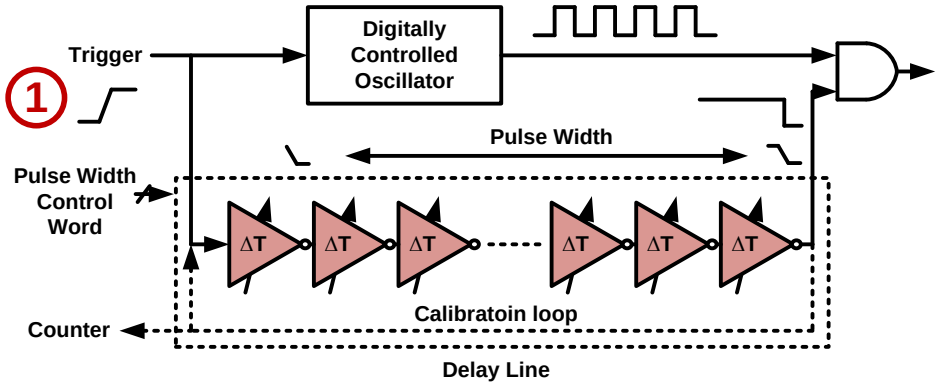

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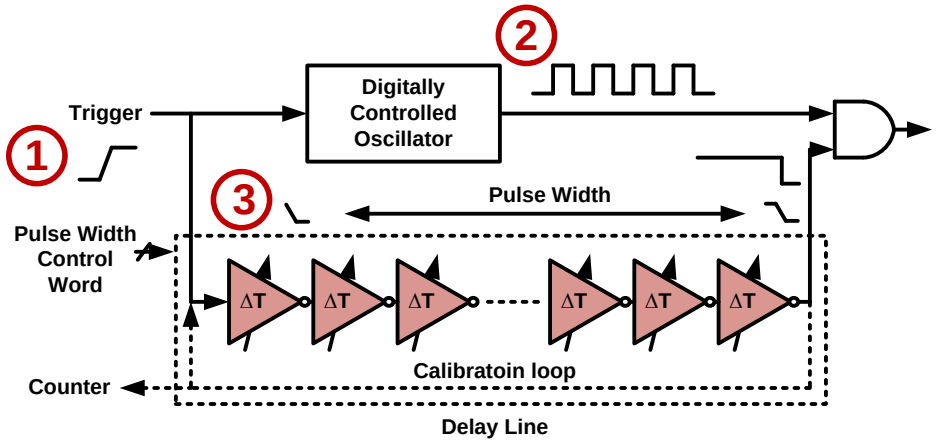

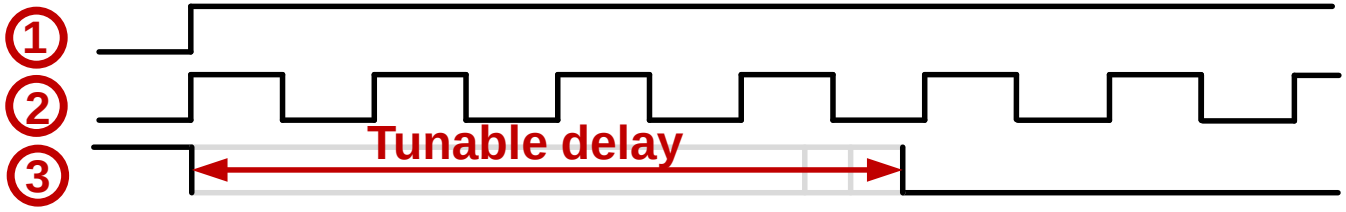

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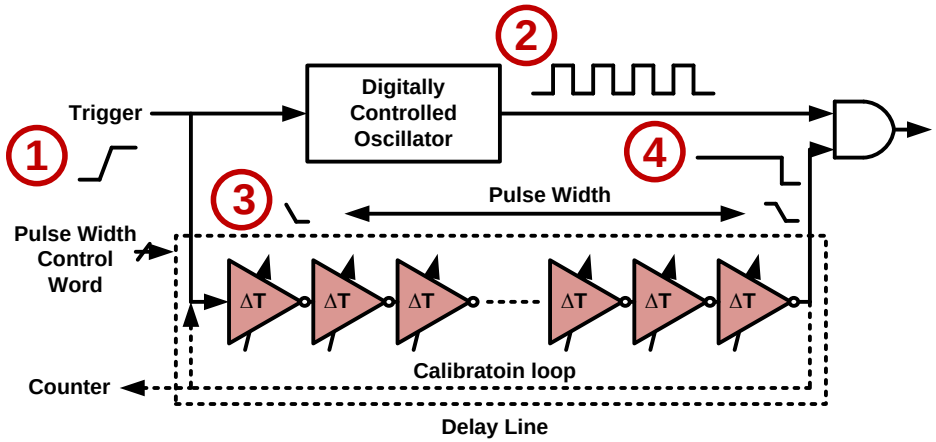

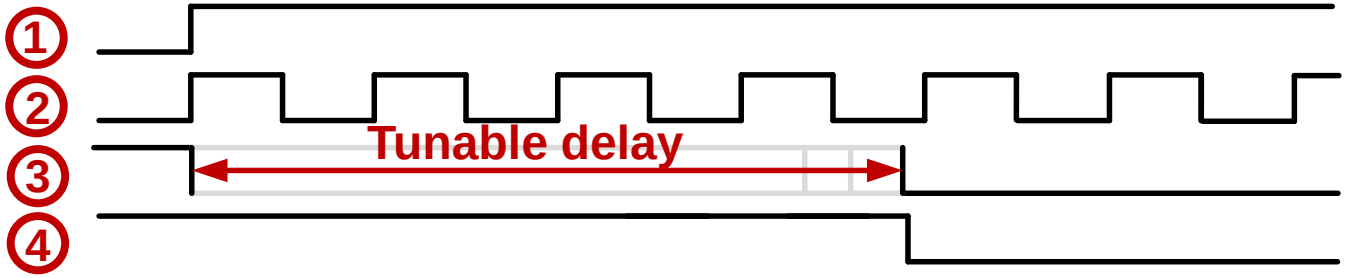

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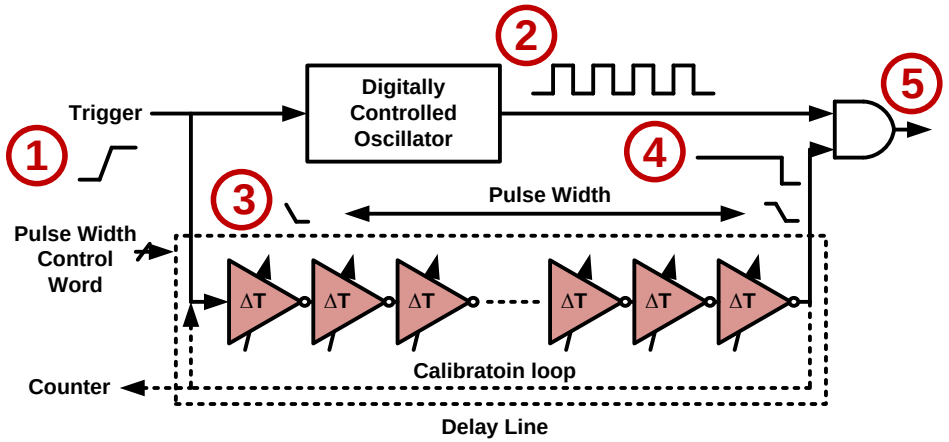

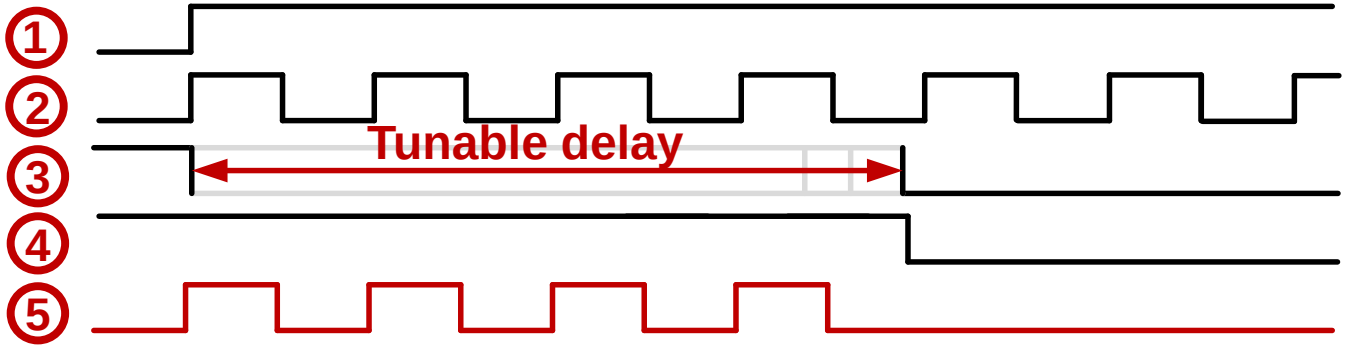

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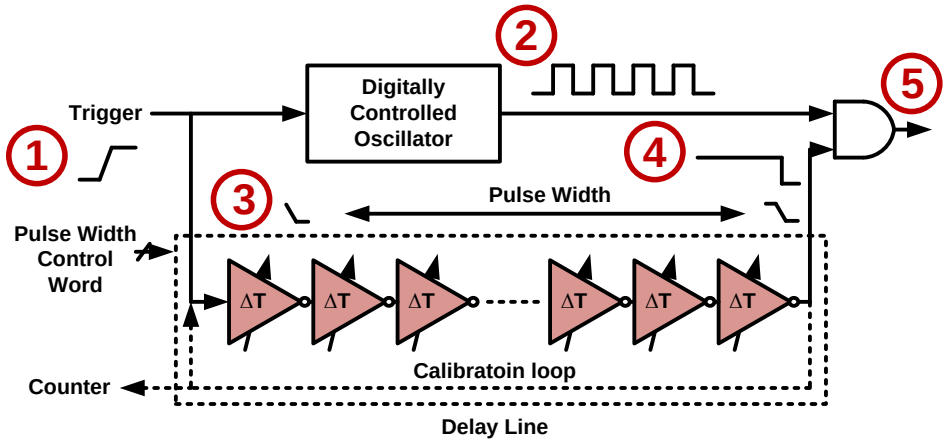
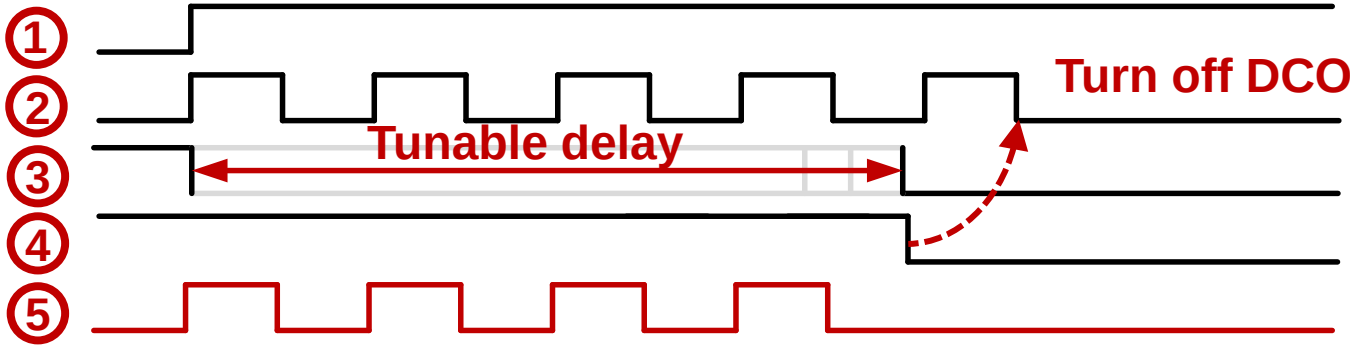
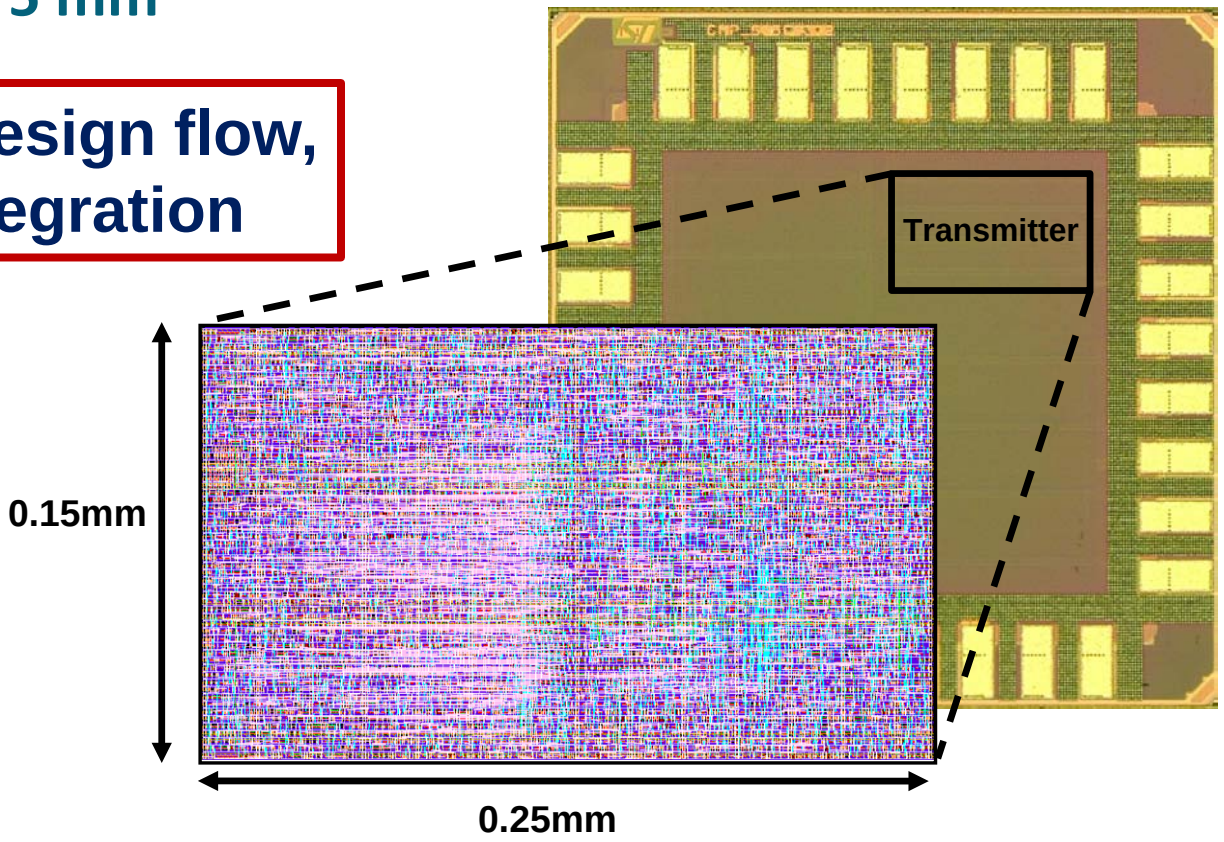




Automatic Place-and-Route

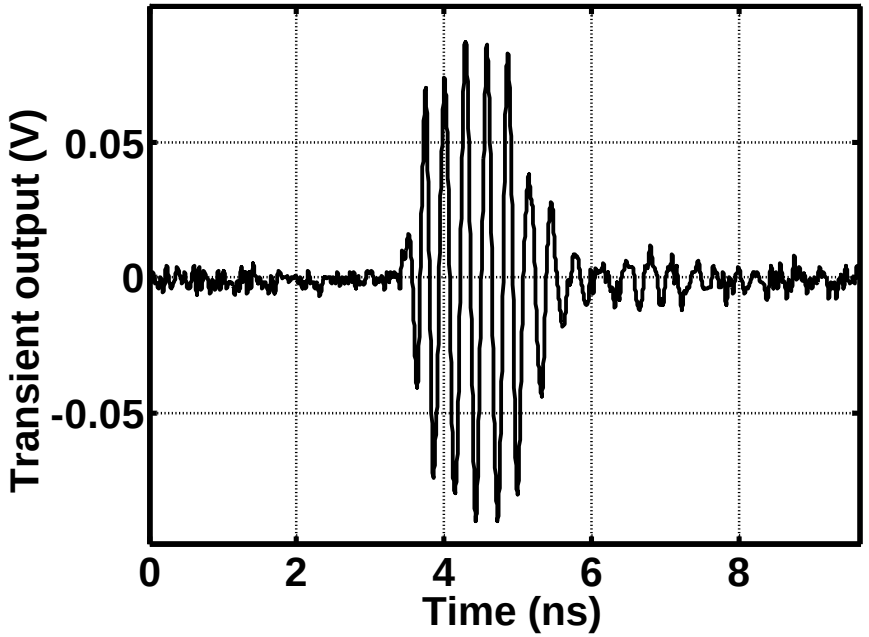
- All functional blocks implemented with standard cells
  - Area : 0.0375 mm^2

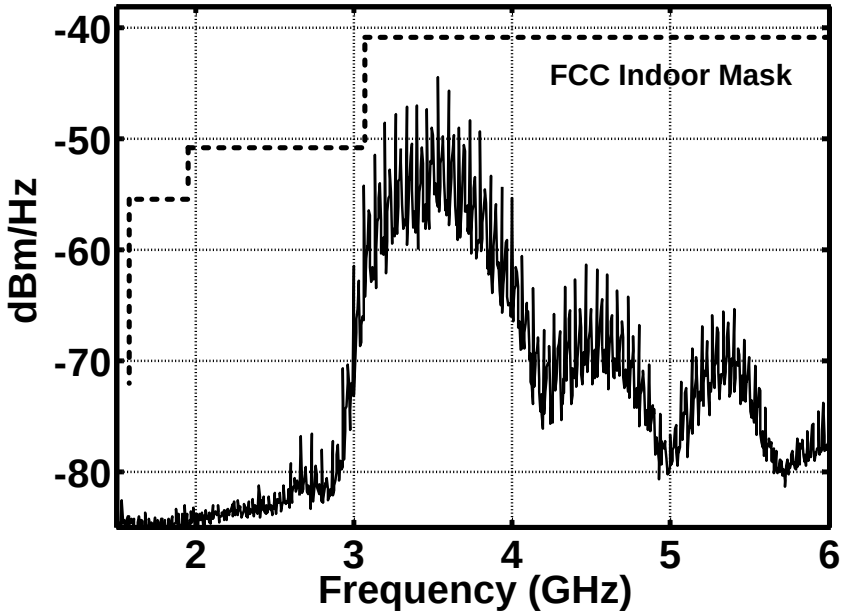
Simplified design flow, higher integration



Measured Pulse and Spectrum

- **Pulse generator in 65nm ASIC**

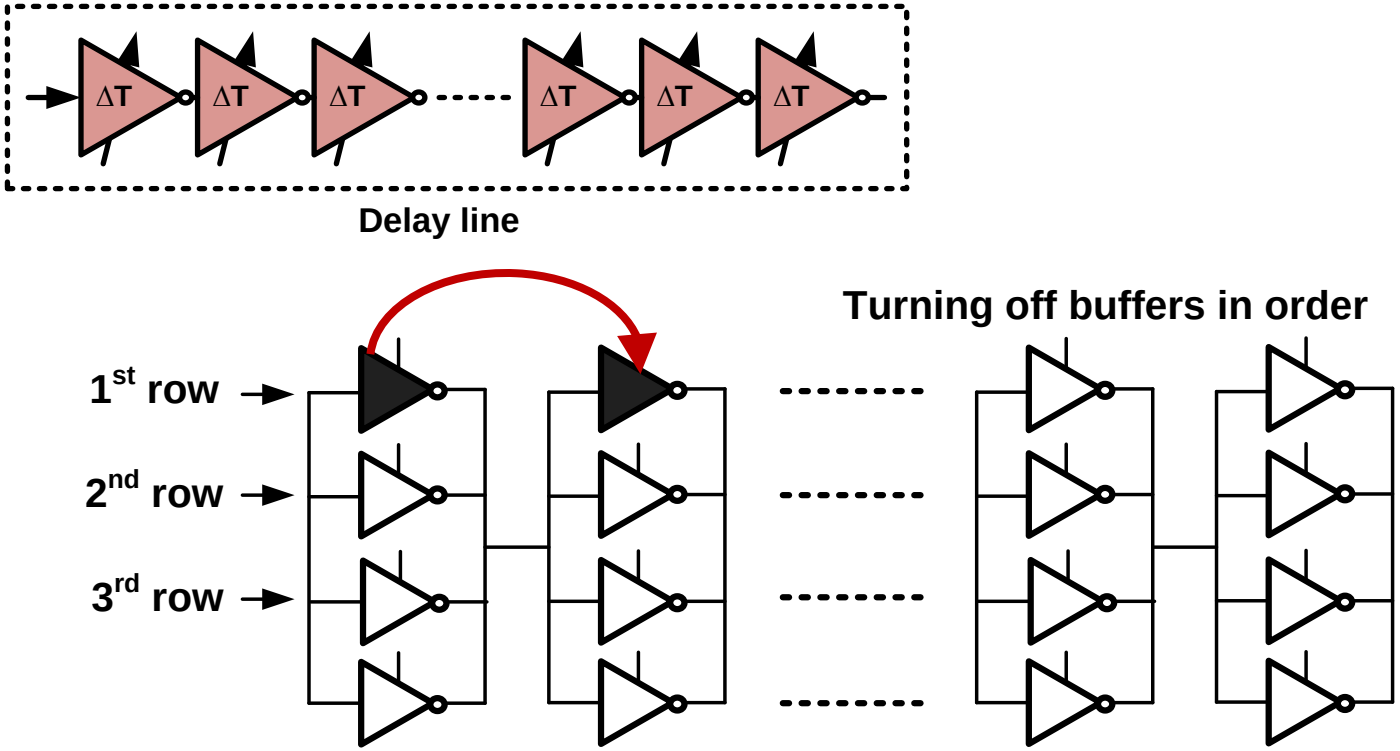




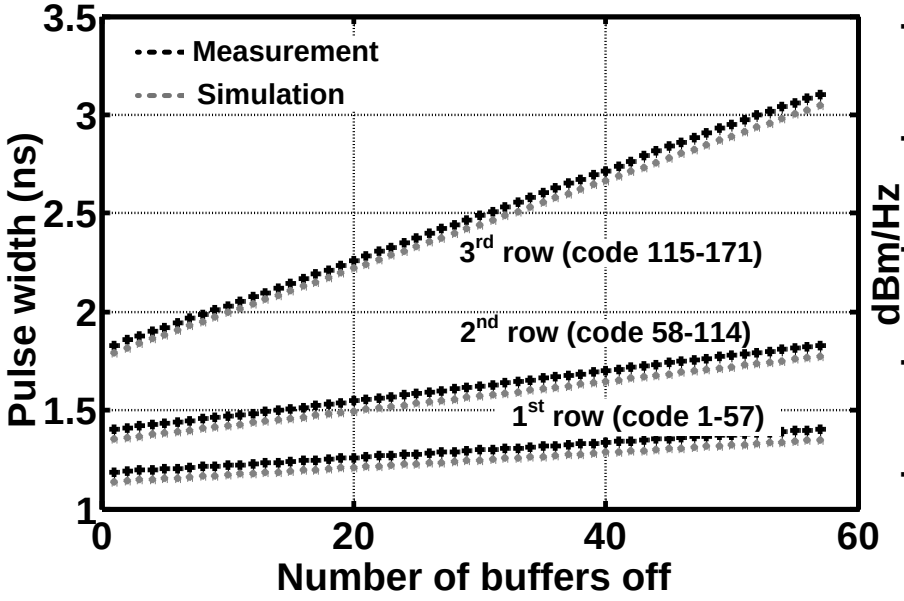
Satisfies FCC requirement
after off-chip 3.1GHz highpass filter

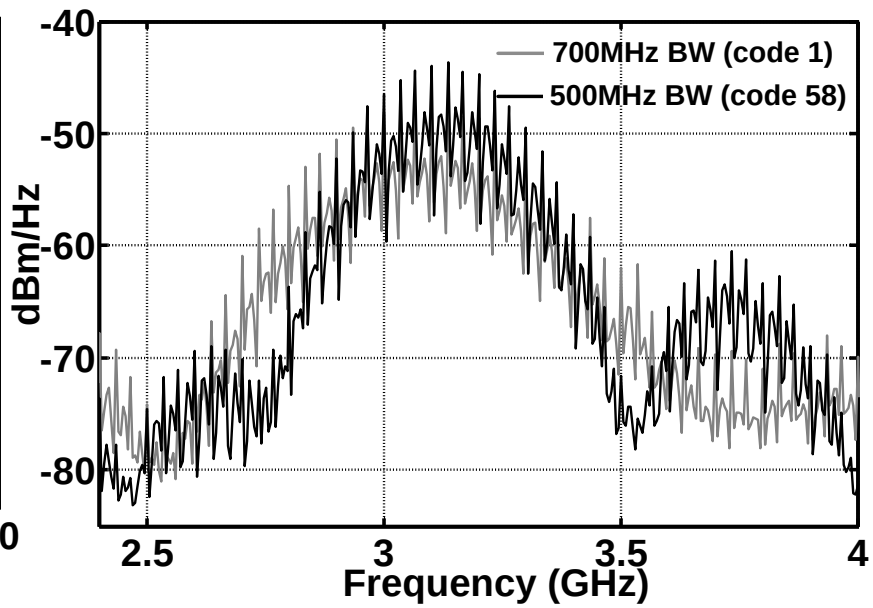
Calibration of Pulse Width

- **Calibrate bandwidth over variations or target different applications**
  - **57 tunable delay cells, 4 tri-state buffers in each cell**



Measured Pulse Width Control





- 4/ 8/ 20 ps resolution

Leverages high performance standard cells

Conclusions

- All-digital UWB Transmitters implemented with digital logic cells
- Prototypes in FPGA and ASIC verify the functionality
- ASIC UWB Transmitter performance

	This work	Wentzloff ISSCC 07
Process	65nm CMOS	90nm CMOS
Die Area	0.0375mm^2	0.08mm^2
Modulation	PPM	PPM
PRF	16.7MHz	16.7MHz
Pulse Width	1.1-3.1ns	-
Active Energy/pulse	90pJ/pulse	43pJ/pulse