# All-Digital Synthesizable UWB Transmitter Architectures

Youngmin Park and David D. Wentzloff

University of Michigan, Ann Arbor, MI, 48109, USA

***Abstract*—This paper presents two all-digital synthesizable pulsed-ultra-wideband (UWB) transmitter architectures. Both delay line-based and ring oscillator-based architectures proposed in this paper are synthesized and place-and-routed (PAR) with existing design tools. This design flow eliminates custom circuit design and layout, thus significantly enhancing design productivity. Also, the center frequency and the bandwidth of the output signals are tuned digitally to compensate for the variation induced by the PAR or to adapt to various applications. To verify the feasibility of the architectures, FPGA prototypes are implemented. The measured output signals of the prototype circuits meet the target spectrum specifications by tuning the mismatch in delay.**

***Index Terms*— ultra-wideband radio, transmitters, pulse generator, all-digital architecture, synthesizable architecture, FPGA**

## I. Introduction

ULTRA-wideband (UWB) is becoming a promising technology for short-range wireless communication applications such as sensor networks and RFIDs with improving performance and reducing cost and power consumption. Among many proposed UWB systems, pulsed-UWB presents many advantages to achieve these targets in the transmitter [1]. When used with pulse position modulation (PPM), most of the complexity is taken by the receiver to detect transmitted signals, thus the transmitter can have a simple architecture which can be integrated with CMOS technology. Also, the transmitter is turned on only when transmitting pulses, thereby significantly reducing power consumption in the transmitter. Recently, various digital UWB transmitters have been implemented in CMOS technologies showing expected performances with low power consumption [2]-[5].

Taking further the advantages of all-digital transmitters, this paper presents *synthesizable* UWB transmitter architectures. These synthesizable architectures, by definition, are described using a hardware description language such as verilog, then synthesized and place-and-routed (PAR) by existing design tools. This eliminates the time-consuming and error-prone procedure of custom circuit design and layout, and enables the UWB transmitter to be synthesized with other digital systems. Automatic PAR, however, can introduce undesirable mismatch in the timing control; hence a digital tuning capability which can compensate for the mismatch introduced by PAR is also included in these architectures.

The remainder of this paper is organized as follows. Section II describes all-digital synthesizable transmitter architectures; delay line-based architecture and ring oscillator-based architecture. The FPGA implementation of the architectures and FPGA-specific issues are discussed in the section III. Section IV then presents the experimental results of the prototype circuits. Finally, section V concludes this paper.

## II. All-Digital Transmitter Architectures

All-digital transmitter architectures are comprised of a system controller, a modulator, and a pulse generator as depicted in Fig. 1. The system controller in Fig. 1 sets all the parameters which control the modulator and the pulse generator. When the PPM modulation scheme is applied, the system controller determines the duration of each PPM symbol and the pulse repetition frequency (PRF). These parameters can be set dynamically based on the detecting resolution of the receiver and the data rate of the input signals. The system controller also sets the parameters that define the center frequency and the bandwidth of the RF output signals. With this interface between the system controller and the pulse generator, the specifications of various applications can be met.

The PPM modulator generates a triggering edge for the pulse generator. According to the control signals from the system

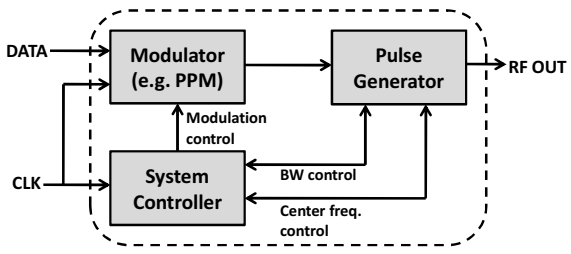



Fig. 1. All-digital pulsed UWB transmitter architecture

controller, it divides the PRF period into a number of time slots and generates one edge at a coded time slot.

The pulse generator synthesizes pulses with the desired center frequency and bandwidth. Since the pulses determine the power spectrum of the transmitted signals, this pulse generator is the most critical block in terms of power and frequency specifications. In this paper, two pulse generators; a delay line-based pulse generator and a ring oscillator-based pulse generator, are presented that are fully described in verilog.

### *A. Delay Line-Based Pulse Generator*

The delay line-based pulse generator [2] consists of a delay line (Fig. 2), a mask register, and an edge combiner (Fig. 3). When a rising edge from the modulator arrives at the delay line, it propagates through $n_{stage}$ stages of delay cells, thus generating $n_{stage}$ delayed rising edges. The delays between these edges are digitally controlled. As shown in Fig. 2, each delay cell is implemented with $n_{width}$ parallel tri-state buffers. When disabled, the output of each tri-state buffer is high-impedance and the driving strength on the shared output node is reduced. Then, the delay through that stage increases. Therefore, the delay between the edges D[n] and D[n+1] are tunable by $n_{width}$ bits of control signals CTRL[$n_{width}$ -1:0].

Fig. 3 shows the mask register and the edge combiner. The generated edges from the delay line are combined in the edge combiner. Since the edge combiner in this architecture is implemented with an XOR tree, each incoming edge toggles the output signal. In this way, two edges combine to generate one cycle and the period of that cycle is the sum of the delays of the two stages, thereby setting RF center frequency of pulse. The mask register selects the edges to be combined in the edge combiner by bitwise AND-ing the edges and corresponding masking bits. This determines the number of cycles in a pulse,

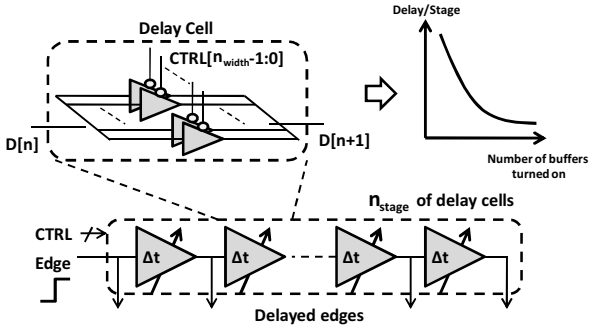



Fig. 2. Delay line and delay cell

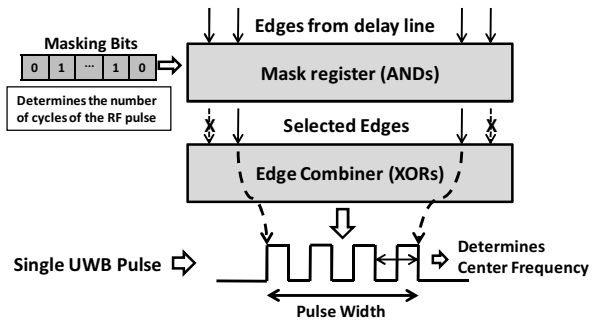



Fig. 3. Block diagram of mask register and edge combiner

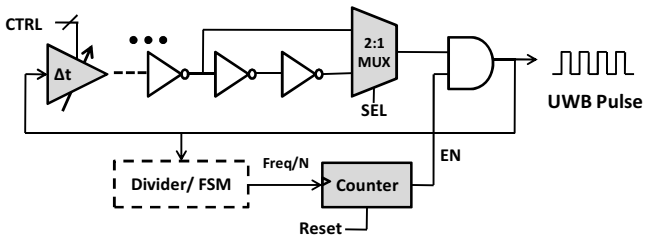



Fig. 4. Ring oscillator-based pulse generator

thereby the bandwidth of the signal in the frequency domain. This pulse generator provides flexibility in the center frequency and the bandwidth to meet the specifications of UWB systems. If the delay of each delay cell is tunable between 50ps and 150ps, and the total number of delay cells is larger than 30, the UWB frequency band (3.1-10.6GHz) can be covered.

### *B. Ring Oscillator-Based Pulse Generator*

The ring oscillator-based pulse generator (Fig. 4) is composed of an inverter chain, a delay cell, a MUX, a divider, a counter, and an AND gate. An odd number of inverters in a ring generate an oscillating signal and the center frequency of the oscillation is determined by the driving strength of each inverter and the number of the inverters. Since these parameters are fixed when the circuit is synthesized, the delay cell and the MUX are included to tune the frequency of the ring oscillation. The delay cell provides digitally tunable delay in the oscillating loop and the MUX selects the number of the inverters in the loop to implement a coarse tuning.

The counter and the AND gate are required to control the number of cycles in a pulse which determines the bandwidth of the output signals. When the counter value reaches the target number of cycles, the oscillating signal is gated and the ring oscillator is turned off. In the event that the synthesized counter is not fast enough to count the RF cycles (3.1-10.6GHz), a divider may be placed before the counter. Since this divider reduces the resolution of the counter, a simple and fast finite state machine is implemented to account for the remainder from the division.

This pulse generator also provides a range of the center frequency and the bandwidth. If the number of the inverters is determined so that the oscillating period is between 100ps and 300ps, the 3.1-10.6 GHz UWB frequency requirements can be met.

## III. PROTOTYPE IMPLEMENTATION (FPGA)

Since all the functional blocks in FPGA circuits are synthesized and place-and-routed by automatic design tools, they are good prototype demonstrations of the synthesizable architectures. Fig. 5 shows FPGA prototype implementation of the all-digital transmitter. In this implementation, the Virtex-II Pro FPGA device and the ISE Foundation design tools from Xilinx are used [6]. The clock signal and the input data are provided to the FPGA from external sources and the input data rate and the output frequency are scaled down to 1Mbps and 110MHz respectively for the purpose of the prototype.

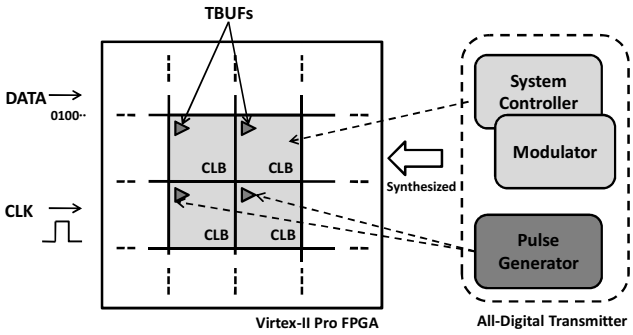



Fig. 5. FPGA prototype of all-digital pulsed-UWB transmitter

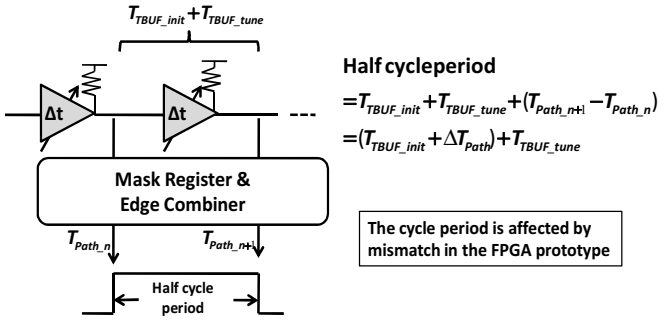



Fig. 6. FPGA prototype of the delay line-based pulse generator

The system controller and the modulator are implemented as finite state machines. Verilog code is written describing their functions, and mapped to the configurable logic blocks (CLBs) in the FPGA device.

Unlike the system controller and the modulator, the timing of the output signals is sensitive to the implementation of the pulse generator. Since the performance of the pulse generator is affected by the synthesis and routing, the detailed implementation of the pulse generator is presented in the following sections.

### *A. Delay Line-Based Pulse Generator*

The Virtex-II Pro FPGA device provides tri-state buffers named TBUF (Fig. 5). Although these buffers are not implemented exactly as the tri-state buffers in CMOS standard libraries, they have input ports controlling connectivity to shared wires. Therefore, the digital tuning described in the previous section can be achieved with TBUFs. The FPGA delay line was implemented with eight stages of delay cells, thus having four cycles per UWB pulse at the output port. The mask register and the edge combiner are implemented with logic gates, which are mapped to the CLBs in the FPGA.

As shown in Fig. 6, the half cycle period is determined by the sum of the delay of each delay cell and the mismatch in the path to the output. With all the TBUFs turned on, the delay cell generates the shortest delay ($T_{TBUF\_init}$). Then, the mismatch in the path delay ($\Delta T_{PATH}$) through the mask register and the edge combiner is added to it. These two values, however, are affected by PAR, thereby introducing variation over the stages. To obtain a unified cycle period, the tunable delay ($T_{TBUF\_tune}$) of each stage is increased by turning off the TBUFs. Fig. 7 shows the measured mismatches and the achievable range by tuning the delay cells. Though the FPGA device has an interconnect-dominant structure, thereby limiting the tuning ability of the delay cells, this pulse generator provides a range of feasible cycle period.

One of the major differences in the FPGA implementation is that pull-up resistors are tied to the output node of each tri-state buffer. When disabled, the output of TBUF is pulled up to the supply voltage, which makes the delay control of the rising edges non-monotonic. To obtain the desired tuning control, only the falling edges are used to synthesize pulses.

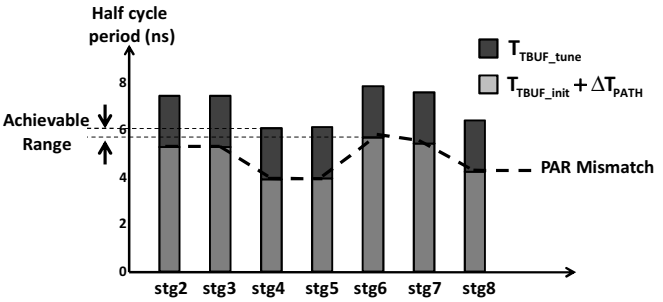



Fig. 7. Measured mismatches of the initial delays and tunable delay values (stage 1 is used as a reference).

### *B. Ring Oscillator-Based Pulse Generator*

Fig. 8 shows the FPGA prototype of the ring oscillator-based pulse generator and cycle period tuning with it. The TBUFs and the MUX are used to tune the center frequency of the oscillating signal. With 16 parallel TBUFs, there are 16 steps of fine tuning. The MUX selects the number of inverters in the loop to provide coarse tuning of the center frequency. As shown in Fig. 8, this pulse generator can have a broad range of center frequency with this coarse-fine tuning approach. Unlike the delay line-based pulse generator, all the RF cycles in a pulse have the same period since they share the same path to the output port.

All blocks including the inverters, the switching gate and the counter are synthesized and mapped to the CLBs in the FPGA device.

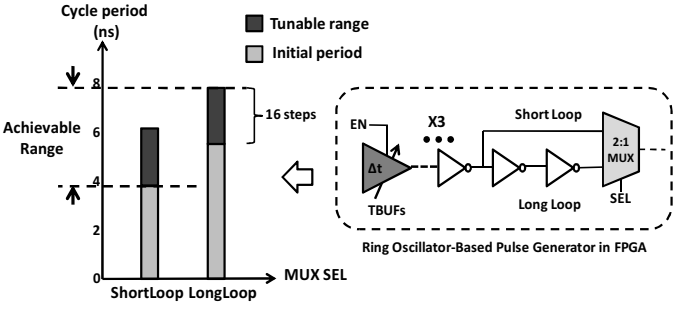


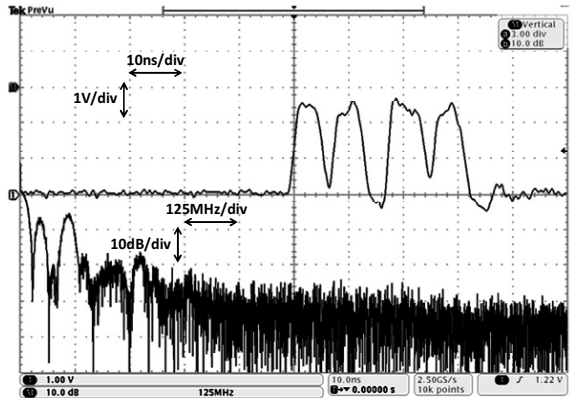

Fig. 8. Period tuning with TBUFs and MUX in the ring oscillator-based pulse generator

## IV. EXPERIMENTAL RESULTS (FPGA)

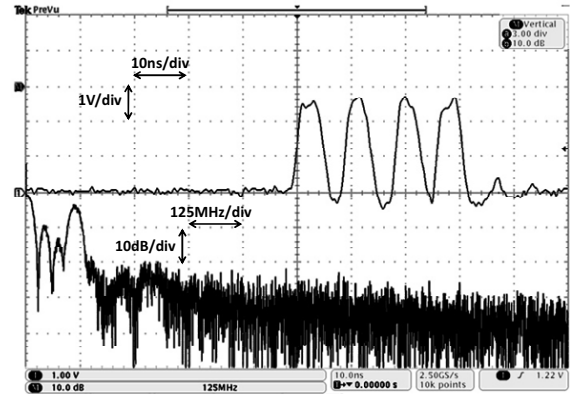
As mentioned in the previous section, the target center frequency is scaled down to 110MHz and the fractional bandwidth requirement (bandwidth > 20% of the center frequency) is achieved in the prototype circuits.

Fig. 9 shows the pulse waveform and the spectrum of the delay line-based pulse generator (a) before and (b) after the delay has been digitally tuned to equalize delays. As explained in Fig. 6 and Fig. 7, the mismatch of the path delay is significant, which prevents the cycles from having unified periods. Thus, the side lobe of the spectrum is not reduced and harmonics are present (Fig. 9a). After tuning each delay cell, the mismatches are compensated and the desired spectrum is obtained (Fig. 9b). The measured center frequency is 110.25MHz and the bandwidth is 41.5MHz (37.6% of the center frequency), which meets the FCC fractional bandwidth requirement.

Fig. 10 shows the pulse waveform and the spectrum of the ring oscillator-based pulse generator. Since the period of each cycle is the same without tuning, only the center frequency is tuned to have the target frequency. The measured center frequency is 111.25MHz and the bandwidth is 41.9MHz (37.6% of the center frequency), which also meets the FCC fractional bandwidth requirement.




a. Without tuning




b. With tuning

Fig. 9. Comparison of measured pulse waveform and spectrum of the delay line-based pulse generator with and without tuning

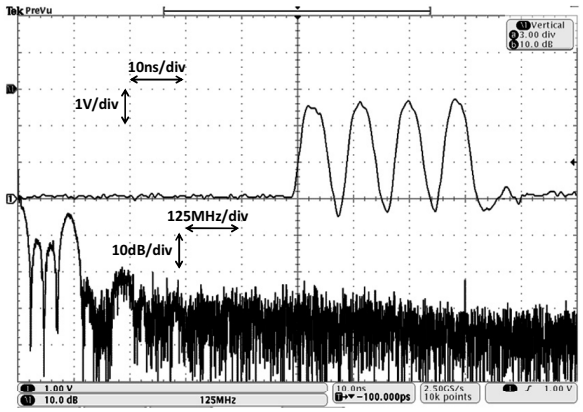



Fig. 10. Measured pulse waveform and spectrum of the ring oscillator-based pulse generator

## V. CONCLUSION

We have presented two all-digital, synthesizable transmitter architectures. Whereas both architectures have digitally tunable center frequency and bandwidth, the delay line–based architecture shows more flexibility in tuning the pulse width. That is, it can have variable duty cycle of the pulses for specific applications and can adopt other modulation schemes such as DB-BPSK [7]. The ring oscillator-based architecture, on the other hand, requires a much smaller number of transistors, thus reducing the area and power consumption. Also, the unified cycle periods simplifies the tuning of the center frequency. However, if the synthesized circuit does not have the desired duty cycle (e.g. 50%), the spectrum has undesirable side lobes.

The FPGA prototype circuits verified the feasibility and the functionality of both architectures. Since these architectures are comprised of functional blocks which can be implemented with standard library cells in CMOS technologies, the desired design productivity and performance from these architectures are achievable with technology scaling.

## ACKNOWLEDGMENT

Youngmin Park is partially funded by the Kwanjeong Educational Foundation Scholarship.

## REFERENCES

[1] M. Z. Win and R. A. Scholtz, "Impulse radio: How it works," *IEEE Commun. Lett.,* no. 2, Aug. 1998, pp. 36-38.

[2] D. D. Wentzloff, A. P. Chandrakasan, "A 47pJ/pulse 3.1 to 5 GHz all-digital UWB transmitter in 90 nm CMOS," *IEEE Int. Solid State Circuits Conf.,* 2007.

[3] J. Ryckaert, *et al*, "Ultra-wide-band transmitter for low-power wireless body area networks: Design and evaluation," *IEEE Trans. Circuits and Systems*, vol. 52, no. 12, Dec. 2005.

[4] T. Norimatsu, *et al*, "A novel UWB impulse-radio transmitter with all-digitally-controlled pulse generator," in *European Solid-State Circuits Conference*, Sep. 2005, pp. 267-270.

[5] C.-F. Liang, S.-T. Liu, S.-I. Liu, "A calibrated pulse generator for impulse-radio UWB applications," *IEEE Journal of Solid-State Circuits,* vol. 41, NO. 11, Nov. 2006.

[6] Xilinx, Virtex-II Pro User Guide, 2007.

[7] D. D. Wentzloff, A. P. Chandrakasan, "Delay-based BPSK for pulsed-UWB communication," *IEEE Int. Conf. on Speech, Acoustics, and Signal Processing,* 2007.