A Step Recovery Diode Based UWB Transmitter for Low-Cost Impulse Generation

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Abstract - **In this paper, we present a step recovery diode (SRD) based ultra-wideband (UWB) transmitter. No custom integrated circuits (ICs) are used, and all of the components are commercially available off-the-shelf products, targeting low-cost and fast turn-around. UWB pulses are generated using SRDs, and pulse position modulation (PPM) is implemented by a microcontroller. Detailed analysis and equations for the SRD-based impulse generation are provided and verified with experimental results. This UWB transmitter has a measured full width half maximum (FWHM) pulse width of 213ps, pulse amplitude of 1.6V, and peak power of 17dBm. The data rate is 2.5MHz, which is limited by the maximum clock frequency of the microcontroller. The supply voltage for the entire circuit is 3V, which is compatible with coin batteries. The power consumption of the SRD pulse generator is 57mW, and the total power consumption of the complete transmitter is 70mW.**

I. INTRODUCTION

The implementation of a simple, low-power and low-cost ultra-wideband (UWB) transmitter is challenging in many UWB communication systems. In many cases, impulse radio-based UWB (IR-UWB) transmitters are fabricated as custom ICs in CMOS processes [1, 2]. They have the advantage of system integration with processing and receiver electronics, etc., in a single-die. However, in some cases, full system integration is not required, and furthermore, some applications require only a UWB transmitter (e.g. channel sounding). In this case, it may be desirable to build a custom, high-performance impulse generator without the cost or complexity of fabricating a custom IC [3]. Moreover, if a pulse with high peak power is necessary, an IC may not be a good option. In particular for portable channel sounding in body area networks, we desire a UWB transmitter that is battery operated, is small enough to be worn on the body, and generates high power impulses to estimate the RF communication channel. In this application, the impulse generator only needs to excite the impulse response of a wireless channel so that it can be recorded by a higher-power receiver. Furthermore, the transmitter has low complexity and does not require compliance with a wireless standard. Therefore, a simple impulse generator is sufficient (no system integration with digital baseband processing is required). Designing a UWB transmitter on a printed circuit board (PCB) with discrete components is advantageous for these UWB applications.
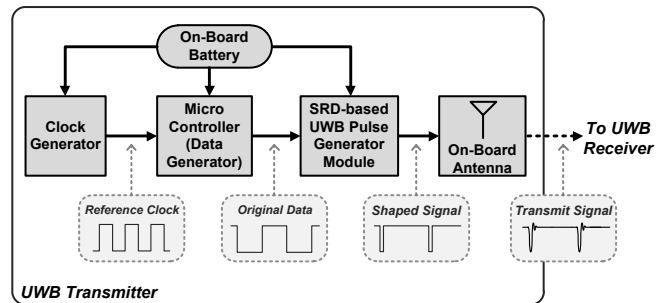

Figure 1. The architecture of the UWB transmitter.

There are several techniques to produce UWB pulses at the PCB design level [4-13]. These include avalanche transistors, tunnel diodes [4], nonlinear transmission lines (NLTLs) [5], photoconductive switches [6], bipolar transistors [7], FETs [8], and step recovery diodes (SRDs) [9-13]. Avalanche transistors have high-power edge sharpeners, but the maximum pulse repetition frequency is limited, and the transistor lifetime is short. Tunnel diodes have short transition times, but their output amplitude is relatively small. NLTLs and photoconductive switches usually require monolithic microwave integrated circuits (MMICs). SRD based circuits are relatively easy to fabricate, cost effective and capable of generating pulses with less than 100ps of transition time. For this reason, SRD based circuits are suitable for low-cost, low-volume, and high performance UWB applications.

There are many papers which use SRDs to implement a UWB transmitter [9-13]. In most of these circuits, the power consumption is high (>300mW), and the supply voltage of the circuit is more than 7V, which is not compatible with a portable battery. This paper presents a simple UWB transmitter with a supply voltage of 3V and also provides equations for estimating the pulse width and amplitude of the SRD pulse generator which are verified by experimental results.

The remainder of this paper is organized as follows. In section II, the architecture of the UWB transmitter is described. A detailed explanation of the UWB pulse generator and the microcontroller, which uses pulse position modulation (PPM), is included. Experimental results are provided in section III. Finally, section IV concludes this paper.
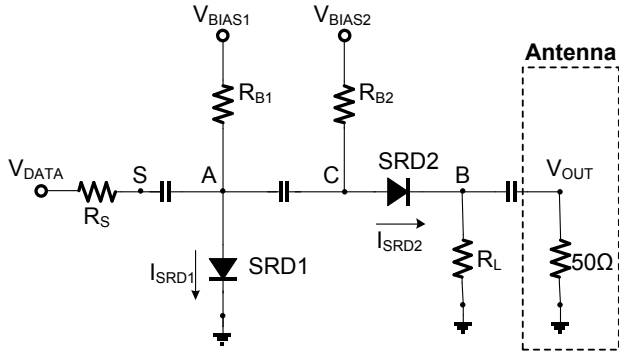
Figure 2. The schematic of the UWB pulse generator.

II. ARCHITECTURE

The architecture of the UWB transmitter is depicted in Figure 1. A microcontroller generates V_{DATA} which contains PPM information to be transmitted, and the UWB pulse generator produces the UWB pulses with SRDs according to the falling edges of V_{DATA}. A single 3V power supply is used for the entire circuit, and a 10MHz reference clock is used to produce the pulse repetition frequency.

A. UWB Pulse Generator

Figure 2 shows the schematic of the UWB pulse generator [13]. The core part of the pulse generator consists of two SRDs. To briefly explain its operation: SRD1 sharpens the falling edge of a negative pulse and SRD2 determines the width of the pulse and sharpens the rising edge of the pulse. Next we will examine the UWB pulse generator circuit in more detail.

The most important characteristic of an SRD is that it stores charge when forward biased. Once the SRD stores enough charge, it can use this stored charge at the beginning of reverse bias to temporarily maintain conduction and a forward bias voltage. Therefore, the SRD still functions like a short circuit with negative current during the initial time in reverse bias. However, when all stored charge is depleted, the SRD suddenly open circuits. At this time, the voltage across the SRD changes dramatically fast so that a sharp voltage edge can be generated. The pulse sharpening operation of the SRD is explained in [13].

Figure 3 shows the voltage and current of each node in the UWB pulse generator. We will divide the entire period into 4 stages, (I) V_{DATA} is high, (II) V_{DATA} is low and the stored charge of SRD1 is being used, (III) the stored charge of SRD1 is depleted and the stored charge of SRD2 is being used, and (IV) all the stored charge of SRD1 and SRD2 is depleted.

During stage (I), V_{DATA} is V_{DD}. SRD1 and SRD2 are forward biased since V_{BIAS1} and V_{BIAS2} are set to be greater than V_{ON1} and V_{ON2}, where V_{ON} is the on-voltage of the SRD. Therefore the voltage at node A, V_A, is V_{ON1} and the voltage of node B, V_B is $I_{F2} \cdot R_L$, where I_{F2} is the forward bias current of SRD2. The forward bias current of SRD1, I_{F1} is $(V_{BIAS1} - V_{ON1})/R_{B1}$ and I_{F2} is $(V_{BIAS2} - V_{ON2})/(R_{B2} + R_L)$. If the forward bias duration is much longer than τ, where τ is the minority carrier
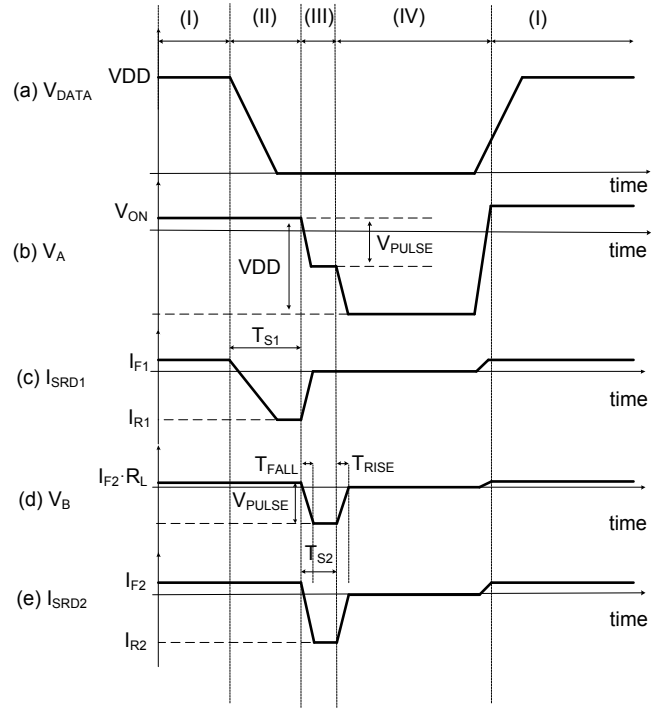

Figure 3. Voltage and current of each node (a) Input Voltage (b) Voltage of A (c) Current of SRD1 (d) Voltage of B (e) Current of SRD2.

lifetime of the SRD ($\tau = 1.7ns$ in our case), the final stored charge of the SRD during forward bias is $I_F \cdot \tau$.

During stage (II), V_{DATA} changes from V_{DD} to zero, and SRD1 is reversed biased. However, due to the characteristics of the SRD that it uses the stored charge at the beginning of reverse bias, V_A is still V_{ON1} and the voltage of node S is still V_{DD}. Therefore the current of SRD1, I_{SRD1}, is negative and the peak reverse current, I_{R1} is $V_{DD}/R_S - I_{F1}$. If the forward bias duration time is much longer than τ, the duration time of stage (II), T_{S1} is $\ln(1 + I_{F1}/I_{R1}) \cdot \tau$.

The transition from stage (II) to (III) occurs when SRD1 becomes fully depleted of the stored charge and transitions to an open circuit. During stage (III), the stored charge in SRD1 is depleted and the stored charge in SRD2 is being used. At this point, SRD1 is an open circuit. SRD2 is conducting reverse current, but similar to stage (II), the voltage between SRD2 is still V_{ON2} because of the stored charge in the SRD. The falling time of V_B, T_{FALL} is $\sqrt{T_T^2 + ((R_S \parallel R_L \parallel 50) \cdot C_T)^2}$, where C_T is the reverse capacitance of the SRD and T_T is the intrinsic transition time of the SRD (specified by the manufacturer). The pulse amplitude is the product of the transient current and the impedance shown at node V_{OUT} to AC ground, $(V_{DD}/R_S - I_{F1}) \cdot (R_S \parallel R_{B1} \parallel R_{B2} \parallel R_L \parallel 50)$. The current of SRD2 is negative, and $I_{R2} = (V_{DD}/R_S - I_{F1}) \cdot (R_S \parallel R_{B1} \parallel R_{B2} \parallel R_L \parallel 50)/(R_L \parallel 50) + I_{F2}$, where I_{R2} is the peak reverse current. The duration time of stage (III), T_{S2}, is $\ln(1 + I_{F2}/I_{R2}) \cdot \tau$.

The transition from stage (III) to (IV) occurs when SRD2 becomes fully depleted. During stage (IV), the stored charge of
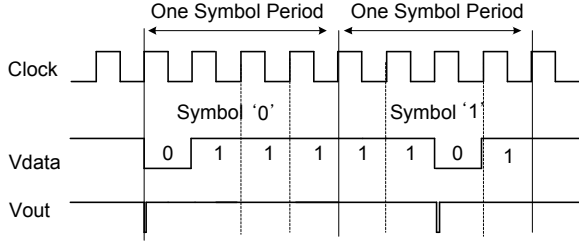
Figure 4. Pulse position modulation.

SRD1 and SRD2 is fully depleted and both SRD1 and SRD2 are open circuits. Therefore V_B will be zero. The Rise time of V_B, T_{RISE}, is $\sqrt{T_T^2 + ((R_S + (R_L \parallel 50)) \cdot C_T)^2}$. Note that the impedance into SRD2 is $(R_S + (R_L \parallel 50))$ which is not the same as SRD1, $(R_S \parallel R_L \parallel 50)$. After stage (IV), stage (I) will repeat on the next rising edge of V_{DATA}.

The following equations summarize the output pulse.

$$T_{FALL} = \sqrt{T_T^2 + ((R_S \parallel R_L \parallel 50) \cdot C_T)^2} \qquad (1)$$

$$T_{RISE} = \sqrt{T_T^2 + ((R_S + R_L \parallel 50) \cdot C_T)^2} \qquad (2)$$

$$pulse\ width = T_{FALL} + T_{RISE} + \ln(1 + \frac{I_{F2}}{I_{R2}}) \cdot \tau \qquad (3)$$

$$amplitude = (\frac{V_{DD}}{R_S} - I_{F1}) \cdot (R_S \parallel R_{B1} \parallel R_{B2} \parallel R_L \parallel 50) \qquad (4)$$

Several design guidelines may be followed for selecting the values of the components. For faster rising and falling edges, and large pulse amplitude, small R_S and R_L are preferred. However, if R_L becomes too small, there is a ringing in the output pulse, and the output amplitude decreases. On the other hand, if R_L is larger than the 50Ω antenna impedance, it has a minimal effect on the pulse width and amplitude. Therefore, large R_L is desirable. Small I_{F1} and I_{F2} are better for lower power consumption, but I_{F1} and I_{F2} should be large enough to store sufficient charge in the SRDs during stages (II) and (III). R_{B1} and R_{B2} should be much larger than R_S and $R_L \parallel 50$Ω for high pulse amplitude.

B. Microcontroller

An ATtiny13A microcontroller is used to generate the data to be transmitted which is PPM modulated. A 10MHz oscillator is used for maximum data rate, which is the maximum frequency of the external clock for this

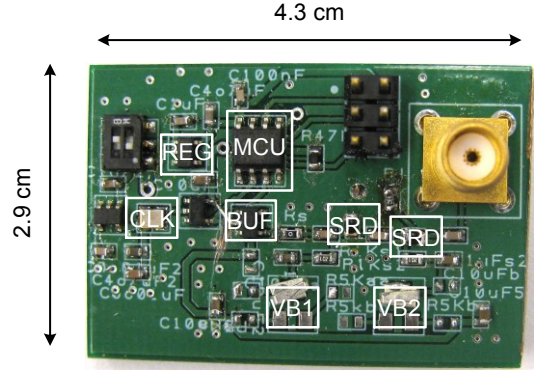|	Manufacturer	Part number
SRD	Aeroflex/metalix	MMDB30
Microcontroller	Atmel	ATtiny13A
Clock	ECS Inc.	ECS-2018-100
Capacitor	Panasonic-ECG	ECJ-1VB1A
Resister	Panasonic-ECG	ERJ-3GEYJ

Table 1. Manufacturer and part number of components.
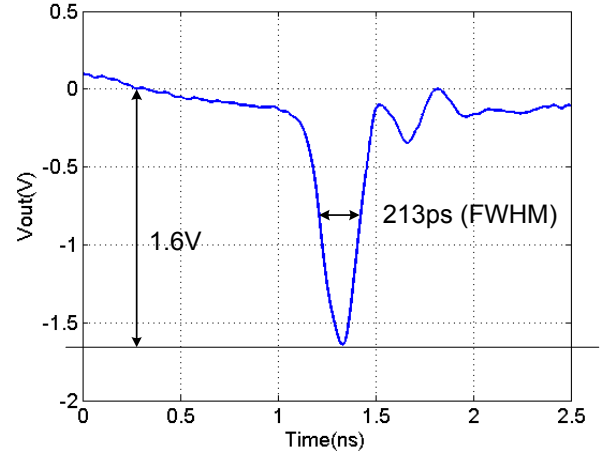

Figure 5. PCB of the UWB transmitter.

Figure 6. Measured UWB pulse at V_{OUT} (R_S:20 Ω, R_L:300 Ω, I_{F1}:9.5mA, I_{F2}:2.5mA).

microcontroller.

Figure 4 shows the pulse position modulation which is used in this system. V_{DATA} is the output of the microcontroller and V_{OUT} is the output of the UWB pulse generator. One symbol period consists of four processor clock cycles. For the symbol '0', the value of V_{DATA} is '0111' and a UWB pulse of V_{OUT} exists at first clock edge. For the symbol '1', the value of V_{DATA} is '1101' and there is a UWB pulse at the third clock edge.

III. EXPERIMENTAL RESULTS

The names of manufacturers and part numbers for the components are listed in Table 1. All of the components are commercially available products. Figure 5 is a photo of the UWB transmitter PCB with all the components. A single 3V supply is used for the entire circuit. A 2.7V regulator is used for the UWB pulse generator, the microcontroller and the buffer, and a 1.8V regulator for the 10MHz clock. For convenience, V_{BIAS1} and V_{BIAS2} were provided from an external power supply during the measurement. However, it could be replaced with voltage dividers using a potentiometer, since V_{BIAS1} and V_{BIAS2} are below 3V. The total size of the PCB is 4.3 cm x 2.9 cm.
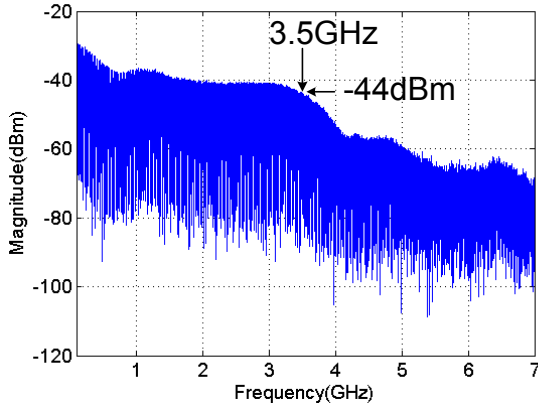
Figure 7. Measured UWB pulse power spectrum (R_S:20 Ω, R_L:300 Ω, I_{F1}:9.5mA, I_{F2}:2.5mA).
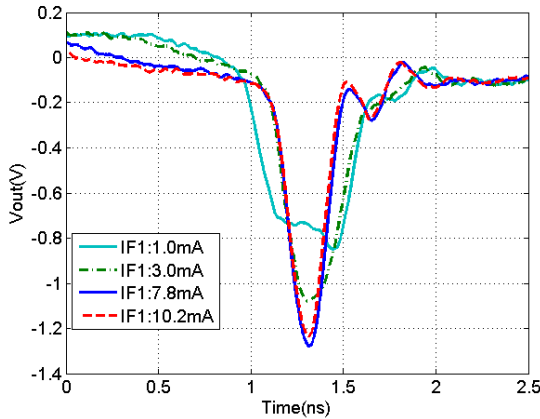
Figure 9. V_{out} vs. I_{F2} (R_S:30 Ω, R_L:300 Ω, I_{F1}:7.8mA).

Figure 8. V_{out} vs. I_{F1} (R_S:30 Ω, R_L:300 Ω, I_{F2}:2.1mA).
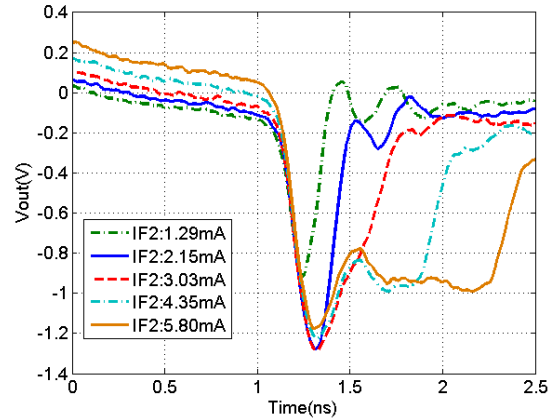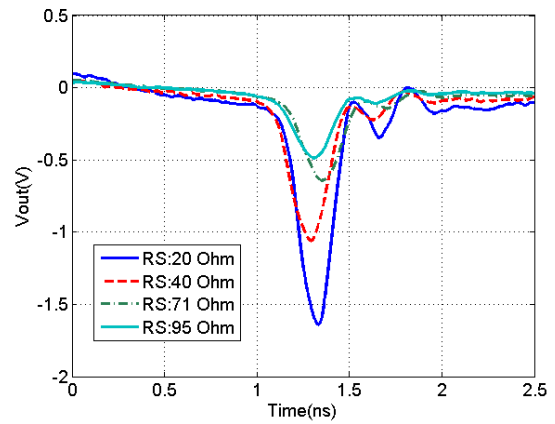

Figure 10. V_{out} vs. R_S (R_L:300 Ω).

Figure 6 shows the output UWB pulse measured with a Tektronix TDS6000C digital oscilloscope. The FWHM pulse width is 213ps and the pulse amplitude is 1.6V, which agrees with 227ps and 1.87V calculated from equations (3) and (4). When calculating equations (3) and (4), output resistance of the buffer should be considered as R_S, which was 20Ω in our case. Figure 7 shows the power spectrum of the UWB pulse measured with an Agilent N9020A spectrum analyzer. The 3dB bandwidth of the UWB pulse is 3.5GHz. The power consumption for the UWB pulse generator is 57mW and the total power of UWB transmitter is 70mW.

Figures 8 and 9 show how the pulse shape changes with various I_{F1} and I_{F2}. In Figure 8, pulse amplitude decreases as I_{F1} decreases, since small I_{F1} cannot store enough charge during stage (II). Once I_{F1} is large enough to store sufficient charge, it no longer affects the pulse shape. It can be seen in Figure 9 that as I_{F2} increases, the pulse width increases and, therefore, delays the rising edge of the pulse, while a smaller I_{F2} reduces the pulse amplitude due to the fact that the SRD cannot hold enough charge during stage (III). Therefore, there is an optimum value of I_{F2} which results in a maximum signal-amplitude to pulse-width ratio, which happened to be I_{F2} = 2.15 mA for our case. .

Figure 10, 11, and 12 show UWB output pulses according to different values of R_S. In Figure 10, the pulse amplitude decreases as R_S increases, and this is predicted by equation (4). In Figure 11, the pulse width increases as R_S increases, but it is not monotonic since the pulse width depends not only on R_S but also on I_{F2}. For each R_S, optimal values of I_{F1} and I_{F2} are applied. Measured results of the pulse width match well with equation (3). In Figure 12, measured results for the pulse amplitude and equation (4) have the same trend and are well matched. Pulse position modulation is verified in Figure 13.

Table 2 shows the performance summary of the UWB pulse generator. The performances from other papers with different components are also provided. The power consumption of the IC based transmitter is the smallest, but the pulse amplitude is also relatively small. The pulse amplitudes of BJT and other SRD based transmitters are high. However, their supply voltage is greater than 7V, which precludes their use with single coin batteries. By comparison, this work demonstrates an SRD based transmitter that operates from a 3V supply, while generating pulse amplitude of 1.6V.
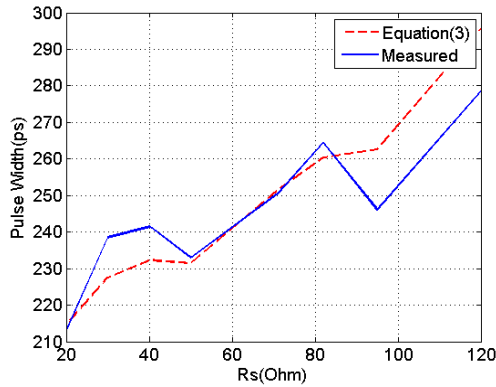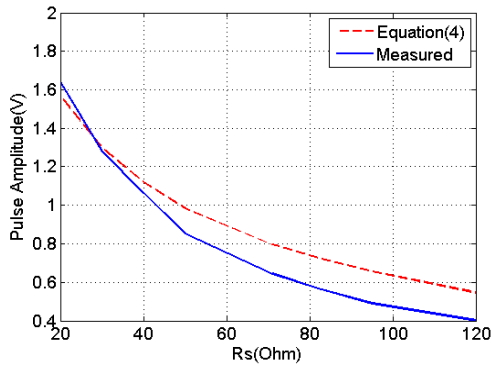
Figure 11. Pulse Width vs. R_S.
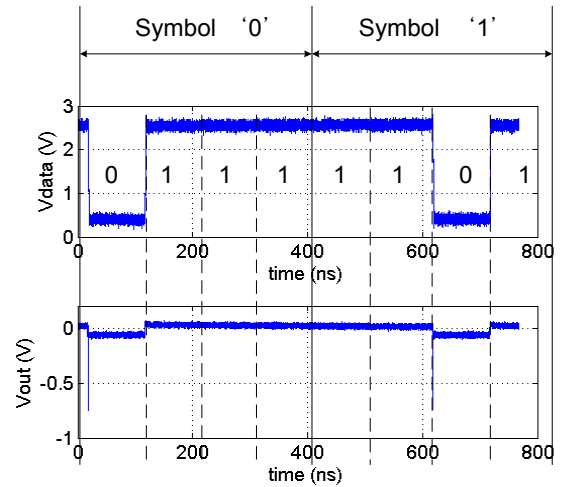

Figure 12. Pulse Amplitude vs. R_S.

Figure 13. Measured PPM output.

consumption of the UWB transmitter is 70mW, which allows continuous operation for 43 hours with a 24.5mm coin battery.

IV. CONCLUSION

This paper has presented details of an SRD based UWB transmitter. The working mechanism of the impulse generator is precisely analyzed and equations for the pulse width and amplitude are provided, which agrees well with experimental results. The measured UWB pulse width (FWHM) is 213ps and the pulse amplitude is 1.6V. PPM is implemented with a microcontroller. All of the components are off-the-shelf commercial products whose manufacturers and part numbers are listed in Table 1. No custom ICs and transmission lines were employed, which makes it possible to fabricate a simple, small size and low-cost UWB transmitter. The total power

	Tech	Pulse Width	Pulse Amplitude	VDD	Power
Hu [1]	90nm CMOS	1ns	160mV	1.2V	225uW
Salameh [5]	NLTL	19ps	1.8V	-	>100mW
Gerding [7]	BJT	90-800ps	7V	-	-
Protiva [9]	SRD	110ps	7.5V	12V	>360mW*
Rueng. [10]	SRD	140ps, 100ps	2.5V, 1.1V	>7V	-
Han [11]	SRD	400-850ps	200-500mV	>7V	-
This work	SRD	213ps	1.6V	3V	70mW

*we calculate power consumption based on forward bias current

Table 2. Performance summary of the UWB pulse generator.

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