A 116nW Multi-Band Wake-Up Receiver with 31-bit Correlator and Interference Rejection

Seunghyun Oh, Nathan E. Roberts, and David D. Wentzloff

University of Michigan, Ann Arbor, MI, 48109, USA

***Abstract* — This paper presents a 116nW wake-up radio complete with crystal reference, interference compensation, and baseband processing, such that a selectable 31-bit code is required to toggle a wake-up signal. The front-end operates over a broad frequency range, tuned by an off-chip band-select filter and matching network, and is demonstrated in the 402-405MHz MICS band and the 915MHz and 2.4GHz ISM bands with sensitivities of -45.5dBm, -43.4dBm, and -43.2dBm, respectively. Additionally, the baseband processor implements automatic threshold feedback to detect the presence of interferers and dynamically adjust the receiver's sensitivity, mitigating the jamming problem inherent to previous energy-detection wake-up radios. The wake-up radio has a raw OOK chip-rate of 12.5kbps, an active area of 0.35mm^2 and operates using a 1.2V supply for the crystal reference and RF demodulation, and a 0.5V supply for subthreshold baseband processing.**

I. Introduction

Wireless sensor nodes spend most of the time in an ultra-low-power sleep state with their radios off to conserve energy. This presents a problem when remotely waking up and synchronizing to these nodes. Wake-up radios (WRX) are a viable solution [1-4], but only if their active power is below the sleep power of the node, otherwise the WRX power dominates and dictates the lifetime of the node. With digital sleep power being reported in the nW range, this presents a significant challenge to WRX design. A simple method for reducing the power of a WRX is to reduce sensitivity, which is tolerable for short-range communication and when the primary goal is a lifetime of multiple years [3]. For example, with a receiver sensitivity of -40dBm, 6m communication at 400MHz is theoretically possible with only 0dBm transmit power. This range and power level is suitable for a broad set of personal and internet of things (IoT) applications.

WRXs use energy detection architectures to keep power low; however, any signal at the proper frequency can trigger a false wake-up of these radios, and false wake-ups result in significant amounts of wasted energy on the node. In order to prevent this, a WRX must have enough local processing to differentiate a wake-up event from interference without use of the node's main processor. The proposed WRX addresses these issues.

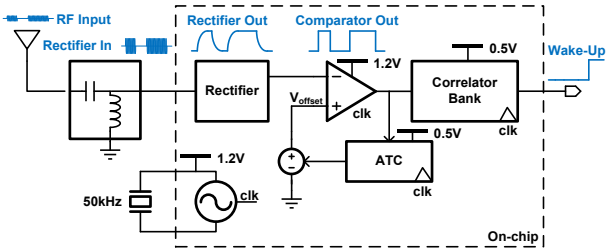

Fig. 1. Architecture of the WRX with rectifier, baseband processor, and crystal oscillator on-chip

A 116nW WRX complete with crystal reference, interference compensation, and all the necessary baseband processing is presented. To operate in the nW power range, the power hungry LNA is replaced with a high-sensitivity, passive RF rectifier, tuned by an off-chip band select filter and matching network. To prevent false wake-ups the WRX does two things: first, it must receive a selectable 31-bit OOK-modulated CDMA code, and second, the baseband processor implements automatic threshold feedback to detect the presence of interferers and dynamically adjusts the receiver's sensitivity, which mitigates the jamming problem found in previous energy-detection radios [1-4]. Operation of the WRX has been demonstrated in the 402-405MHz MICS band and the 915MHz and 2.4GHz ISM bands. Section II will introduce the architecture of the WRX. Section III will explain the major circuit blocks of the WRX in detail, and Section IV will present measurement results. Finally, Section V will conclude the paper.

II. System Architecture

Fig. 1 shows a block diagram of the WRX. From the antenna and band-select filter, the RF signal passes through an input matching network that filters and boosts the signal before going on-chip. A 30-stage rectifier down-converts the RF signal to baseband, which is then sensed by a comparator clocked at 4X the chip-rate. The input offset voltage of the comparator is controlled by the ATC (Automatic Threshold Controller) which is used to overcome interferers. A bank of 124 correlators (31 shifts of the code, 4x oversampled) continuously compare the

978-1-4673-6146-0/13/$31.00 ©2013 IEEE

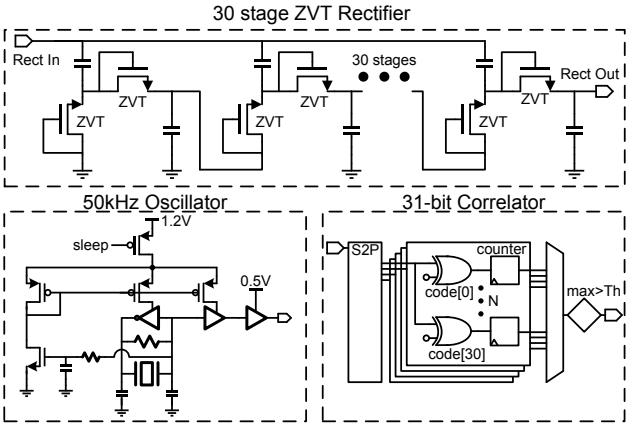

Fig. 2. Schematic of the rectifier, crystal oscillator, and parallel correlators

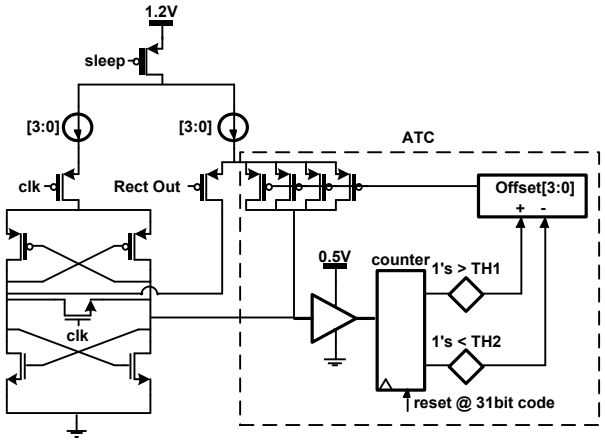

Fig. 3. Schematic of the clocked comparator and automatic threshold control (ATC)

received chip sequence with a programmable wake-up code, and toggles the wake-up signal only when a correlation result exceeds a user-programmable threshold. The reference clock for the receiver is generated using an off-chip 50kHz crystal with an integrated oscillator. The oscillator and comparator operate from a 1.2V supply while all the digital logic operates in subthreshold at 0.5V.

III. Circuit Description

In this section, the major circuit blocks of the WRX are explained in detail. All circuits include a thick-oxide PMOS header to reduce sleep-mode power at the expense of slightly higher active power.

A. Off-chip matching network

For the WRX, a 2-element off-chip matching network was used and provided a passive 5dB voltage boost. For example, at 400MHz the input impedance of the chip was measured on a network analyzer to be 23-j35Ω, and a 12pF series capacitor and a 15.7nH shunt inductor were used in this case. The Q factor of the input impedance is low, due to a voltage limiter that prevents the rectified voltage from exceeding the breakdown voltage of the FETs, so a broadband matching network could be implemented. Devices like BAW or FBAR resonators can also be used to tune to the desired frequency of operation

B. RF rectifier

An RF rectifier, shown in Fig. 2, replaces a traditional LNA to save significant power. The rectifier's structure is the same as the Dickson Multiplier, with the exception that all transistors operate in the sub-threshold regime (at low Rx power levels). The output voltage calculation is therefore different [5]. This subthreshold rectifier uses zero-threshold transistors and 30 stages to achieve sufficient RF gain with fast charging time.

C. Crystal oscillator

A 50kHz crystal oscillator in Fig. 2 [6] serves as the reference clock of the WRX. An off-chip crystal is used, and the oscillator's primary amplifier is an inverter with resistive feedback. When the oscillator circuit first turns on, the transconductance of the primary amplifier is much greater than the critical transconductance of the crystal in order to start oscillation and increase amplitude. As the amplitude increases the DC level of the oscillation drops, which is used in feedback to starve the primary amplifier until it settles to 38nW while sustaining oscillations.

D. Comparator with ATC

The clocked comparator, shown in Fig. 3, applies regenerative feedback clocked by the 50kHz oscillator [7]. Two separate current biases are each controlled by 4-bit binary-weighted current DACs. The programmable 4-bit binary-weighted input threshold of the comparator is controlled by the ATC which dynamically adjusts the offset voltage to overcome interference signals. The ATC monitors the samples coming from the comparator output for one 31-bit code period. If the number of 1's is greater than a programmable value (indicating an interferer is present), then the ATC will increase the comparator's threshold to bring the sensitivity of the receiver above that of the interfering signal. When the number of 0's at the output of the comparator reaches a separate programmable value (indicating the interferer is gone), the ATC then reduces the threshold to increase the sensitivity of the receiver. Hysteresis is added between these values to eliminate limit-cycles.

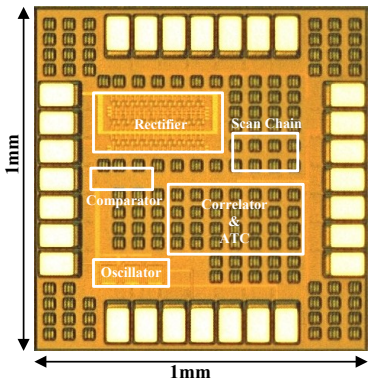

Fig. 4. Die photo

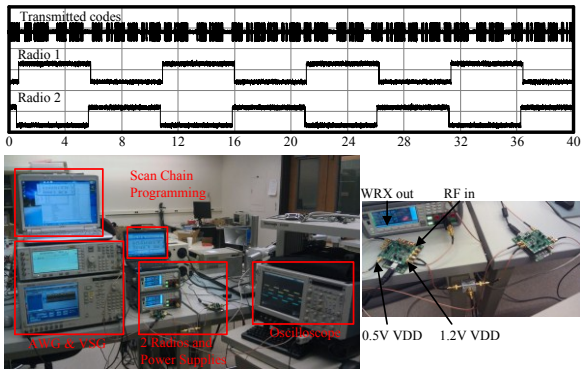

Fig. 5. Measurement with 2 codes and 2 receivers.

E. Correlators

Four banks of 31 correlators, each shifted by one sample, work simultaneously to account for any phase shift between the transmitter and WRX. Each correlator takes two samples per chip from the 4X sampled comparator output when correlating with the wake-up code. Therefore, each 31-bit code has 62 total comparisons. This is used to synchronize the WRX to the chip boundary. In addition, each correlator simultaneously compares with every possible shift of the code, in order to align to the code boundary. A programmable correlator threshold determines the number of correct sample points needed before the wake-up code is toggled. A lower correlator threshold means fewer bits have to match the code, improving sensitivity, but leads to more false wake-ups. A higher correlator threshold prevents false wake-ups, but also reduces the sensitivity of the receiver.

IV. Measurements

The IC is fabricated in an IBM 130nm CMOS process. Fig. 4 shows the die photo of the fabricated chip. The total size is 1mm x 1mm, and the wake-up receiver occupies 0.35mm^2 without pads.

Fig. 5 shows the measurement setup. It also demonstrates the WRX's ability to accept only the programmed code and reject others. In this setup an arbitrary waveform generator (AWG) and vector signal generator (VSG) were transmitting two different codes back to back. The signal was then split and sent to two different WRXs that were each programmed with two different codes. The top trace shows the transmitted OOK signal and the bottom traces show that each WRX toggles its wake-up signal when receiving its own code, but not when receiving the other code.

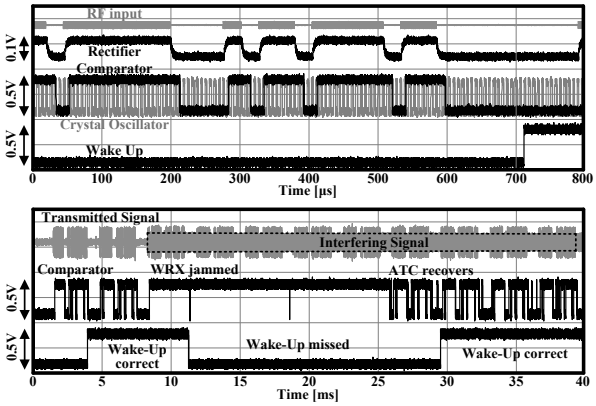

Fig. 6. Transient response of the WRX in normal operation, and in the presence of an interferer

Detailed transient operation of the WRX receiving a 31-bit code is shown in Fig. 6. The WRX automatically synchronizes to the incoming bit stream. The top two traces show the RF input signal and the RF rectifier converting the signal to baseband. The third trace shows the output of the comparator being clocked at 4X the data-rate by the local oscillator and the final trace is the wake-up signal being toggled by the correlator. The WRX is capable of CDMA by selecting different codes used by the correlator block.

If an interfering signal is strong enough to exceed the comparator threshold (saturating the bit-slicer), then the ATC increases the comparator's threshold until it is above the interfering signal. A transient of this operation can be seen in Fig. 6. The top signal is the received RF signal, which is jammed by a 2.4GHz tone at 8ms. With the interferer present, the comparator initially outputs 1's so that the receiver cannot receive the code. After 15ms, the ATC has raised the threshold of the comparator above that of the interferer, and the WRX regains synchronization.

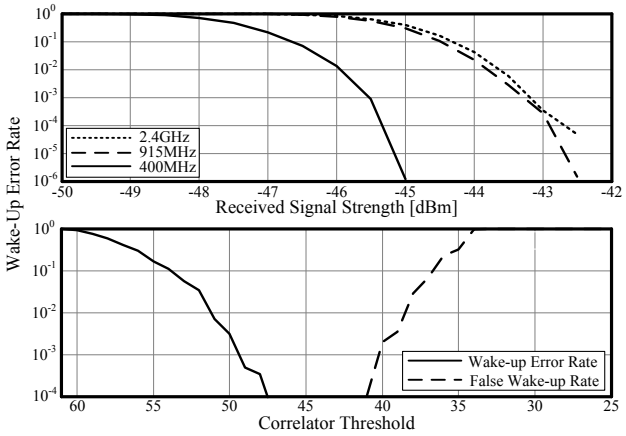

Fig. 7. Wake-up error rate vs. signal strength and correlator threshold

The top of Fig. 7 shows the chip error rate (BER) curves for the 403MHz, 915MHz, and 2.4GHz bands. Sensitivity is best in the 403MHz range. The bottom of Fig. 7 shows BER as the correlator threshold is varied. The measurements were taken using a -40dBm signal in the 2.4GHz band. The figure also shows the impact this threshold has on false wake-ups. From these two data sets, the correlator threshold can be set to maximize sensitivity while minimizing the possibility of a false wake-up.

The WRX has an active power of 116nW with a sleep power of 18pW, afforded by thick-oxide headers. A full power breakdown can be found in Table I. The digital baseband processing consumes the majority of the power in the WRX. The measured performance is summarized and compared with other WRXs in Table II.

V. Conclusion

This paper introduced a 116nW WRX that uses CDMA codes to provide interference rejection from both in-band and out-of-band interferers. In addition, with programmable wake-up codes, the WRX can be used in a network with similar WRXs and be able to uniquely wake up. With reduced sensitivity specifications, the use of a zero-power RF energy harvester was used as the RF front end of the receiver and subthreshold design was implemented to keep entire radio in the nanowatt power region. With power that is less than a typical sensor node's sleep power, the WRX is not the energy dominant circuit when the node is asleep and can provide false wake up rejection, making it a very suitable synchronization technique for sensor nodes.

Table I
Power breakdown and receiver specs

Power Breakdown [nW]		Receiver Specs	
RF Rectifier	0	Energy/bit	9.28pJ
Comparator	8.4	Energy/wakeup	287.7pJ
Digital Logic	69.5	Max signal level	-15dBm
Crystal Oscillator	38.4	Max interferer level	-20dBm
TOTAL	116.3	Code length	31
Sleep [pW]	20	# of pre-defined codes	8

Table II
Comparison with other state of the art work

	This Work			**[1]**	**[2]**	**[3]**
Power [µW]	0.116			52	45	0.098
Sleep [pW]	20			N/A	N/A	11
Frequency [MHz]	403	915	2400	2000	5800	915
Data-rate [kbps]	12.5/31			100	14	100
Sensitivity [dBm]	-45	-43	-41	-72	-45	-41
SIR [dB]	3.3	1.7	1.7	N/A	N/A	N/A
Die Area [mm^2]	0.35			0.1	N/A	0.03
VDD [V]	1.2|0.5			0.5	3.0 ~ 3.6	1.2
Process [nm]	130			90	130	130

Acknowledgement

This material is based upon work supported by the National Science Foundation under Grant No. CNS-1035303.

References

[1] N.M. Pletcher, et. al, "A 2GHz 52µW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture, " ISSCC Dig. Tech. Papers, pp. 524-525, Feb. 2008

[2] Jeongki Choi, et. al, "An interference-aware 5.8GHz wake-up radio for ETCS, " ISSCC Dig. Tech. Papers, pp. 446-448, Feb. 2012

[3] N.E. Roberts, and D.D. Wentzloff, "A 98nW Wake-Up Radio for Wireless Body Area Networks," Radio Frequency Integrated Circuits Symposium, pp.373-376, June 2012

[4] X. Huang, et. al, "A 2.4GHz/915MHz 51µW Wake-up Receiver with Offset and Noise Suppression, " ISSCC Dig. Tech. Papers, pp. 222-223, Feb. 2010

[5] Seunghyun Oh, and D.D.Wentzloff, "A −32dBm Sensitivity RF Power Harvester in 130nm CMOS," Radio Frequency Integrated Circuits Symposium, pp.483-486, June 2012

[6] Hector Ivan Oporta, "An Ultra-low Power Frequency Reference for Timekeeping Applications," Master's Thesis, Oregon State University, December, 2008

[7] B. Razavi, and B.A. Wooley, "Design techniques for high-speed, high-resolution comparators," Solid-State Circuits, IEEE Journal of, vol.27, no.12, pp.1916-1926, Dec. 1992