A 217µW -82dBm IEEE 802.11 Wi-Fi LP-WUR using a 3rd-Harmonic Passive Mixer

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***Abstract*— A 40nm CMOS IEEE 802.11 Wi-Fi LP-WUR receiver is presented. The receiver demodulates OOK messages generated by an 802.11 OFDM Wi-Fi transmitter operating at 5.8GHz. The receiver improves sensitivity by allocating the image-less single sideband signal above the flicker noise floor. The 3rd harmonic down-conversion receiver reduces active power consumption, while rejecting unwanted harmonic components. The receiver achieves a sensitivity of -82dBm while consuming 217µW at a BER of 10^{-3} and data-rate of 62.5kb/s.**

***Index Terms*— sub-harmonics N-path passive mixer (SH-NPPM), 3rd harmonics down-conversion, 802.11 LP-WUR, Wi-Fi wake-up.**

I. Introduction

Wi-Fi is the most ubiquitous wireless protocol. However, the excessive power consumption of legacy 802.11 radios limits the widespread adoption of Wi-Fi in ultra-low power (ULP) IoT applications. Even with heavy duty cycling, the average power is still too high for most ULP IoT applications. According to the 802.11 LP-WUR study group, the power budget of an active Wi-Fi network can be significantly reduced by leveraging a wake-up radio when the regular Wi-Fi radio remains asleep [1]. ULP Wi-Fi wake-up radios have recently been published supporting this network control scheme [2-3]. These prior works, however, do not meet the sensitivity specification of existing 802.11 OFDM receivers, therefore limiting the range of an ULP Wi-Fi network utilizing these wake-up receivers.

In this paper, an ULP 5.8GHz 802.11 wake-up receiver is presented with a sensitivity of -82dBm at a BER of 10^{-3} and data-rate of 62.5kbps, while consuming 217µW. The receiver uses a 3-path, 3rd harmonic mixer-first RF front-end that requires a ring oscillator operating at only 1/3 the RF frequency. The 3 RF paths cancel the fundamental component, while enhancing the desired 3rd harmonic component. This saves significant power while still achieving a NF of 17dB, resulting in the best sensitivity-power trade-off for receivers operating above 3GHz.

The paper is organized as follows. The 802.11 LP-WUR OOK frequency planning, and its (de)modulation is covered in Section II. Detailed circuit architectures of 3rd harmonic down-conversion and LO design are in Section III. Measured results of the receiver, and a comparison with past ULP down-conversion receivers are discussed in Section IV. Finally, Section V concludes the paper.

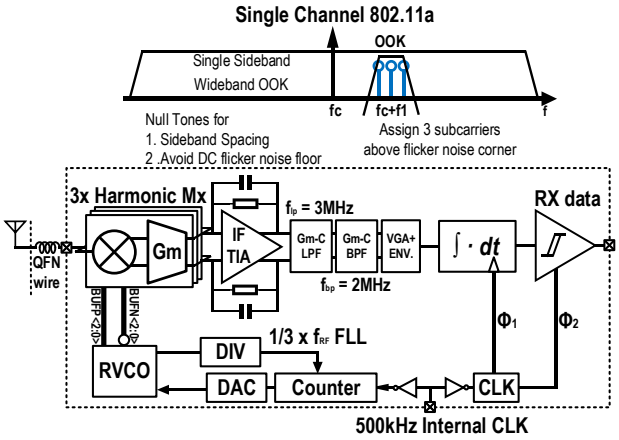

Fig. 1. Frequency plan of 802.11 LP-WUR OOK (top), and block diagram of the receiver (bottom).

II. Frequency Plan & System Architecture

The frequency planning of the 802.11 LP-WUR is shown in Figure 1. Legacy Wi-Fi OFDM signals are generated by modulating sub-carriers in the frequency domain, converting sub-carrier symbols to the time domain signal, outputting them through a DAC, and finally up-converting the signal to RF. This OFDM architecture allows for a wide set of modulations such as OOK or M-ary FSK, although it is not specifically designed for this type of signal generation. By only updating the firmware of an 802.11 OFDM radio [1-2], it is possible to map narrowband OOK or FSK symbols onto OFDM subcarriers, and disable un-used sub-carriers. As shown in Figure 1, the 802.11 LP-WUR signal can be generated by selectively allocating power to a subset of sub-carriers, which are OOK modulated. The maximum symbol rate of the Wi-Fi wake-up data is 250kS/s, the same as the OFDM symbol rate. As subcarriers are 312.5kHz apart, the resulting OOK WUR signal has wider bandwidth compared to conventional ULP transceivers [1-2]. The proposed frequency plan has asymmetric power allocation to enable single sideband modulation (SSB) without the image on the other side of the spectrum. It removes the requirement for quadrature mixing at the receiver, and the

multi-carriers are shifted slightly above the center frequency to avoid DC flicker noise floor when demodulating the wake-up signal.

The system architecture is shown in bottom of Figure 1, which performs direct down-conversion. Although the WUR signal is generated from an 802.11 OFDM transmitter, the receiver does not require a highly linear RF front-end, high-resolution ADC, or significant digital baseband processing due to its relatively simple wideband (de)modulation scheme.

III. 3RD-HARMONIC MIXER-FIRST RF FRONT-END

The key novelty in the architecture is the sub-harmonic 3-path passive mixer which down-converts RF signal at the 3rd-harmonic of the LO, while cancelling undesired signals at the fundamental. We propose a sub-harmonic, N-path passive mixer (SH-NPPM) for low-power, direct-conversion receiver implementation. Recently, sub-harmonics frequency generation, and transceivers have been proposed [4-5] for low power applications, which uses frequency multiplication by edge combining before or in the mixing stages. This requires more power than conventional RF down-conversion, because edge-combining ultimately generates an LO frequency at RF. This results in equal or higher power in the LO buffers and mixers, except for the oscillator. In contrast, in this work the highest frequency generated is RF/3, thus all LO and buffer components operate at lower power.

As shown in Figure 2, combination of phases happens at the baseband amplifier output after down-conversion, which is node C. A commutating passive mixer has a non-linear response, so that at node B, when feeding an LO operating at f_{LO} to the mixer, it produces harmonic

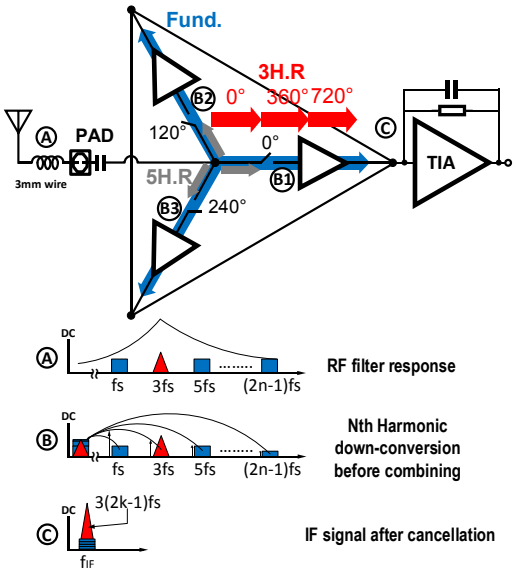

Fig. 2. RF front-end of the receiver using 3rd-harmonics down-conversion.

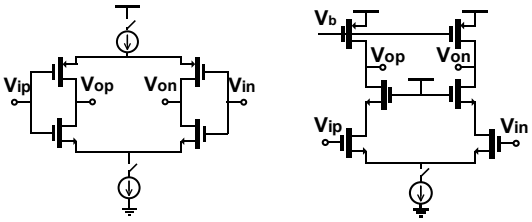

Fig. 3. IF circuits. Left figure is a single cell of IF-LNA, and right figure is a trans-impedance amplifier (TIA).

components at $(2n-1) \times f_{LO}$ (n is an integer). Allocating N-paths with mixers operating at 360°/N phase difference each, Nth harmonic signals will be in-phase at baseband, while the other harmonic components are out-of-phase and cancel. The differential SH-NPPM requires 2N mixers operating at f_{RF}/N. The number of LO buffers and RF switches used for RF front-end is 2X fewer than in [5], which is a dominant factor of the overall ULP receiver power consumption. The architecture doesn't inevitably require a high-Q-enhanced RF gain stage in front of the mixing stage due to undesired harmonic spurs generated from the sub-sampling mixer [4]. As shown in Figure 2, the SH-NPPM architecture only requires N narrowband baseband amps, which is a good trade-off for ULP radio designs because these operate at significantly lower power than RF stages. Considering FLL offset control and noise analysis, this architecture shows optimal trade-off between performance and power with an LO at 1/3 of the RF frequency, so that 3rd-harmonics 3-path passive mixer is implemented.

Ideally, the front-end can reject fundamental RF component perfectly while down-converting signals at the 3rd-harmonic. However, two mismatch factors affect the rejection ratio (3rd harmonic / fundamental). Mismatch in delay cells generate phase deviation which reduces the rejection ratio as the deviation increases. However, the dominant factor is gain mismatch in the first IF stages which impacts the rejection ratio. According to simulation, a phase error less than 5% results in a rejection ratio up to 40dB. To minimize the gain mismatch, self-biased current steering differential IF amplifiers are used with fine resolution gain tuning. The worst rejection ratio measured was 37dB, which is the value with passive RF matching before RF front-end.

IV. LO GENERATION AND IF CIRCUITS

In this design, we the LO had a targeted PN of -75dBc/Hz for wideband OOK and low active power. The PN specification is derived by a BER performance analysis which defines the border where sensitivity is limited by phase noise at a fixed signal bandwidth.

According to [7], it is shown that for a target PN specification at a certain offset frequency for narrowband applications, time-interleaved RVCOs (TI-RVCOs) have

better power efficiency when compared to conventional RVCOs. Using a harmonic component from a lower-operating-frequency TI-RVCO results in a lower $1/f^3$ frequency corner at the target RF frequency when compared to an RVCO that operates directly at the target RF frequency. This results in better phase noise vs. power efficiency for harmonic TI-RVCOs. Furthermore, the power dissipated from the divider in a TI-RVCO based FLL operates at a lower frequency, further reducing power. In [7], logic cells are used to multiple the frequency of a TI-RVCO. However, in this design the low-frequency LO signals are directly applied to the mixer which performs harmonic mixing, saving power of high-speed logic.

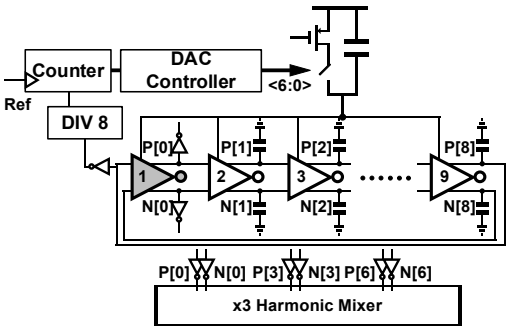

Fig. 4. Frequency locked loop of the receiver.

To aggregate 3 phase offsets from the RVCO that runs at $f_{RF}/3$, a 9-stage differential RVCO was chosen. The LO is composed of a 9-stage differential TI-RVCO, and counter-based programmable FLL with a low frequency reference for frequency calibration. The DAC counter decides to in/decrease the RVCO current based on a duty-cycled counter value. When the counted value exceeds the target reference value, the IDAC current is reduced, and vice versa when the value is lower than the reference value. For fast settling, the IDAC changes with larger steps when the absolute value difference between the counter and reference is over the programmable threshold.

After 3rd harmonic down-conversion, the OOK data is retrieved after IF gain stages and energy collection stages. The IF signal is low pass filtered, and then band pass filtered which has an IF center frequency below 3MHz. 2nd-order Gm-C filters were used for each filter design.

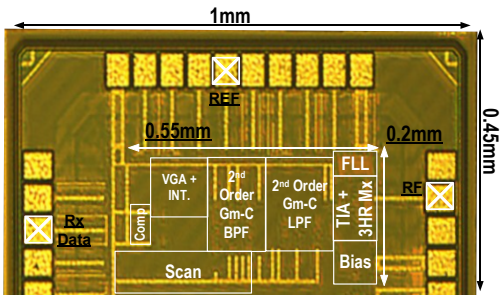

Fig. 5. A CMOS 40nm chip photograph.

The filtered signals are envelop-detected and then integrated, then finally compared with an on-chip voltage reference with a 1-bit comparator. The integrator is oversampled by an external clock to determine the symbol boundaries. The measured gain provided from baseband was 20dB.

V. Measured Results & Comparisons

The proposed receiver was fabricated in a CMOS 40nm technology. The active area is 0.151mm^2. Figure 5 shows a measured BER waterfall curve, and SIR. The receiver is operating at 5.8GHz, with a single sideband signal bandwidth of 2MHz. Due to the non-zero IF demodulation, the spectrum is spread from -3MHz to 3MHz. The Wi-Fi wake-up signal has a bandwidth of 3×312.5kHz, which uses only part of the full 20MHz spectrum bandwidth of the IEEE 802.11a standard.

The measured noise figure is 17dB around 1-3MHz, which matches simulations very well. However, the measured flicker noise corner was 2X higher than predicted by simulations.

The measured SIR is -20dB, and -24dBm from adjacent channels 1 and 2 respectively. The interference performance can be limited by the phase noise of the RVCO, thus, for narrow band receivers, SIR performance is dominated by phase noise rather than the order of band pass filter when the order is reasonably high (≥4). According to our analysis, 4th order filter is the optimal number.

The measured LO leakage power at the RF input node was -92dBm at the frequency of interest. The sensitivity of receiver was -82dBm at a BER of 10^{-3} at a data-rate of 62.5kbps, while consuming 217μW (the 500kHz reference

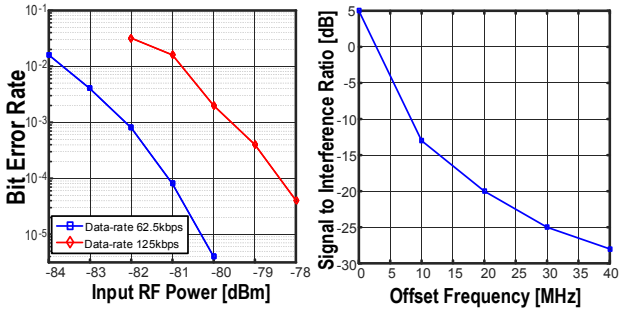

Fig. 6. BER waterfall curve, and SIR of the receiver.

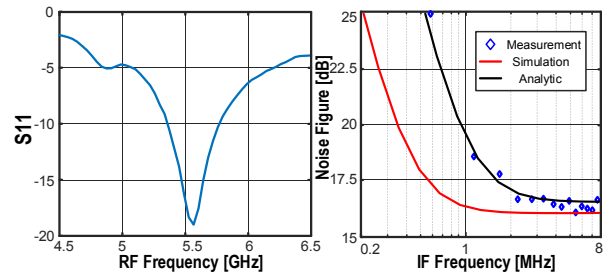

Fig. 7. S11, and Noise Figure of the receiver.

clock generation which can be realized to crystal osc. within 3µW is excluded in the total power consumption). Table I summarizes the performance of the receiver with state of art Wi-Fi wake-up radio, and high operating frequency ULP receivers which have the best performance in terms of sensitivity vs. active power.

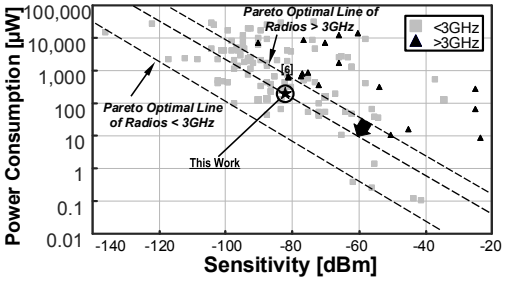

Fig. 8. ULP radio survey from 2005 to present. The data of the radio survey is from top conferences (ISSCC, VLSI, RFIC, CICC) and commercial TRx chips [8].

Table I summarizes the performance of the receiver with state of art wake-up radios. According to ULP survey shown in Figure 8, the receiver advances the Pareto optimal line of >3GHz receivers in terms of active power vs. sensitivity trade-off.

VI. Conclusion

An IEEE 802.11 Wi-Fi LP-WUR receiver is presented. The receiver demodulates OOK modulated messages generated by an 802.11 OFDM Wi-Fi transmitter operating at 5.8GHz. The 3rd harmonic down-conversion receiver reduces active power consumption, while rejecting unwanted harmonic components. The receiver achieves a sensitivity of -82dBm while consuming 217µW at a BER of 10^{-3} and data-rate of 62.5kb/s.

Acknowledgment

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TABLE I
COMPARISON WITH STATE-OF-ART ULP RADIOS

	JSSC 2015 [6]	JSSC 2016 [9]	RFIC 2017 [2]	RFIC 2017 [3]	This Work
CMOS Tech. [nm]	90	65	14 FinFET	65	40
External Component	1MHz External Clock	High-Q inductors External Clock	32kHz RTC	250kHz External Clock Off-chip RF Filter	500kHz External Clock
Carrier Frequency [GHz]	3-5	2.4	2.4	5.8	5.5-5.8
Voltage [V]	1	0.5	0.95	1	0.95/0.55**
Modulation	FM-UWB	OOK	OOK	FSK	OOK
Sensitivity [dBm] @ 10^{-3}	-80.5	-97/-92	-72	-72	-82
Active Power [µW]	580	99	95	335	217
Noise Figure [dB]	6.6	20***	NA.	25***	17
Data Rate [kb/s]	200	10/50	62.5	31.25	62.5
LO Generation	No LO, RF Env.	Unlocked LC-VCO	Ring with FLL	Ring with FLL	TI-RVCO with FLL
SIR*[dB]	-28	-25/-22	-20****	-13	-20

* Adjacent Channel **0.5V for LC-VCO, 0.95V for Analog Blocks
*** Back calculated from Sensitivity [dB] = -174 + signal BW. + NF + SNRout. **** ACI rejection measurement

TABLE II
RECEIVER POWER BREAK-DOWN

	RVCO+FLL	IF-LNA	TIA	Gm-C Filter	Env.	Int.	Bias Circ.
Power [µW]	137	30	15	15	5	5	10