60 GHz On-Chip Patch Antenna Integrated in a 0.13-µm CMOS Technology

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Abstract - **This paper presents a design method of on-chip patch antenna integration in a standard CMOS technology without post processing. A 60 GHz on-chip patch antenna is designed utilizing the top metal layer and an intermediate metal layer as the patch and ground plane, respectively. Interference between the patch and digital baseband circuits located beneath the ground plane is analyzed. The 60 GHz on-chip antenna occupies an area of 1220 µm by 1580 µm with carefully placed fillers and slots to meet the design rules of the CMOS process. The antenna is centered at 60.51 GHz with 810 MHz bandwidth. The peak gain and radiation efficiency are -3.32 dBi and 15.87%, respectively. Analysis for mutual signal coupling between the antenna and the clock H-tree beneath the ground plane is reported, showing a -61 dB coupling from the antenna to the H-tree and a -95 dB coupling of 2 GHz clock signal from the H-tree to the antenna.**

I. INTRODUCTION

IC technology is advancing towards ubiquitous wireless communication. It is desirable to have compact integrated systems for applications such as wireless sensor networks and undetectable surveillance [1]. System-on-a-chip (SoC) is one solution for small form factor system integration of the radio RF front-end, digital baseband circuitry, sensors and energy processing. Among the building blocks in a wireless system, the antenna plays a critical role because it is traditionally off-chip, and dominating the overall size of the system. Recently, several highly-integrated CMOS radio systems with on-chip antennas operating at the mm-wave range have been reported [2]-[5], showing promising opportunities for complete SoC integration. At the 57-64 GHz band approved by Federal Communications Commission (FCC) [6], the guided wave length λ in silicon is about 2.5 mm; which is a comparable scale with the active circuit blocks (e.g. processor, memory, and radio). Furthermore, elimination of expensive off-chip antenna packing, path loss, and the total size makes it more appealing for wireless system integration.

Nevertheless, there are several challenges for on-chip antenna integration. First, the area occupied by the antenna and the space for isolating the crosstalk between antenna and active circuits should be considered. Additionally, the lossy silicon substrate in a CMOS process degrades the antenna performance significantly. Moreover, the design rules in CMOS technology such as metal slotting and density requirement also impact the antenna design. In this paper, an area efficient 60 GHz patch antenna is presented, without any post processing in a standard CMOS 0.13 µm technology. Section II compares different topologies of on-chip antenna at 60 GHz. The tradeoffs between antenna gain and fabrication issues are investigated in Section III, providing a practical design aspect. Furthermore, the mutual coupling effect between the antenna and the circuit routing beneath is discussed in Section IV. Finally, Section V concludes the paper.

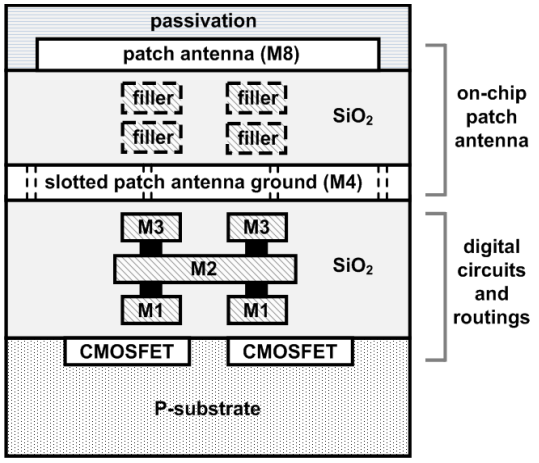

Figure 1. Layout cross section of the proposed integration scheme in a standard 0.13µm CMOS process.

II. CMOS ON-CHIP ANTENNAS AT 60 GHZ

In a standard CMOS process, the resistivity of the silicon substrate is approximately 10 Ω-cm, and the dielectric constant is 11.7. On-chip antennas suffer from the low resistivity and the high dielectric constant, causing energy dissipated in the substrate instead of radiated into the air. Therefore, most of the antenna topologies without shielding from the lossy substrate have low radiation efficiency numbers, thus low antenna gains. Different types of on-chip antenna have been reported at 60 GHz and 77 GHz bands [2]-[4]. Table I compares four common topologies of CMOS on-chip antenna. The patch antenna has the highest radiation efficiency and antenna gain due to the ground shielding the antenna from the substrate, as shown in Fig. 1.

TABLE I
COMPARISON OF CMOS ON-CHIP ANTENNA TOPOLOGIES AT 60 GHZ

Type	Area	Gain	Efficiency	Directivity
Dipole	Δ	Δ	Δ	X
Monopole	O	X	X	X
Loop	X	Δ	Δ	X
Patch	X	O	O	Δ

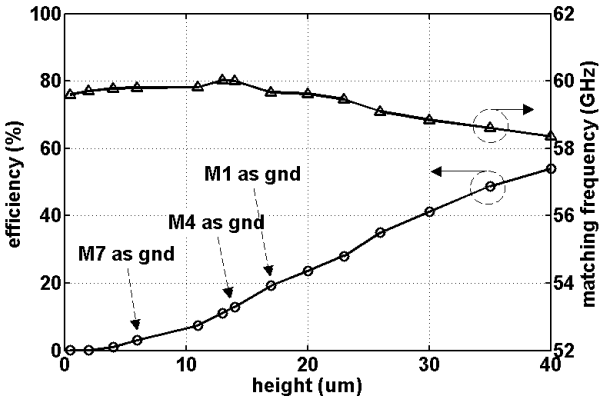

Figure 2. Efficiency and center frequency of the antenna versus the height of the antenna.

Space below the patch antenna is required for integrating custom circuits (e.g. DSP and memory) in a SoC application. Conventional digital circuits typically use 4 to 6 metal layers for wire routing; fewer metal layers of routing is feasible, but at the cost of lower circuit density. Consequently, the patch antenna is a good candidate for system integration due to the better performance and reusable area beneath the patch. The tradeoff between the performances of the antenna and room for digital circuitry beneath will be discussed in the following section.

III. ON-CHIP PATCH ANTENNA INTEGRATION

A. Patch Antenna Design

Microstrip patch antenna theory is well developed. The width and the length of the patch for the frequency of interest can be determined by the transmission line model [3]. From this model, we calculate the length and the width of the patch as 1.22 mm and 1.58 mm, respectively. The patch needs a ground plane to shield the substrate, which can be drawn in a lower metal layer in the CMOS process. The distance between the patch (top-metal) and the ground metal layer determines the height of the patch antenna. Fig. 2 shows the simulated radiation efficiency and the center frequency of the antenna versus the height when the patch length and the width are fixed. More separation between the patch and ground metal is desirable for higher radiation efficiency, which translates to using a lower metal layer for ground. However, using a lower layer for ground results in fewer metal layers available for routing circuits beneath the ground plane, therefore a tradeoff exists. For digital circuit blocks, we take SRAM as a bench mark to determine the minimum routing layers needed. SRAM contains the densest metal routing in VLSI, and typically uses a minimum of 4 routing layers including one ground layer. By sharing M4 as ground plane for both digital circuits and the patch antenna, it provides not only a good AC ground for the RF return current path, but also a good global DC ground. Accordingly, M4 is chosen for the shared patch ground plane and SRAM ground layer, resulting in an antenna height of 14.06 μm, trading a 15% efficiency reduction of the maximum efficiency for 3 metal layers of digital circuit wire routing. The center frequency variation due to different heights is also shown in Fig. 2; however, the center frequency can be tuned by modifying the length of the patch antenna. Fig. 3 shows the dimension of the 60 GHz patch antenna design and its standing wave pattern at the center frequency. The darker area represents a weaker electric field distribution. This standing wave pattern is critical when placing digital circuits and the dummy fillers which will be demonstrated in the later section.

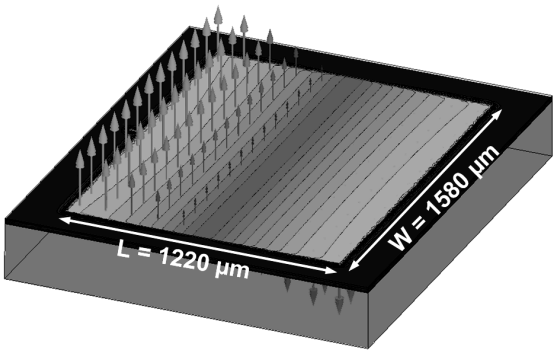

Figure 3. The dimension of the 60 GHz patches antenna design with its standing wave pattern.

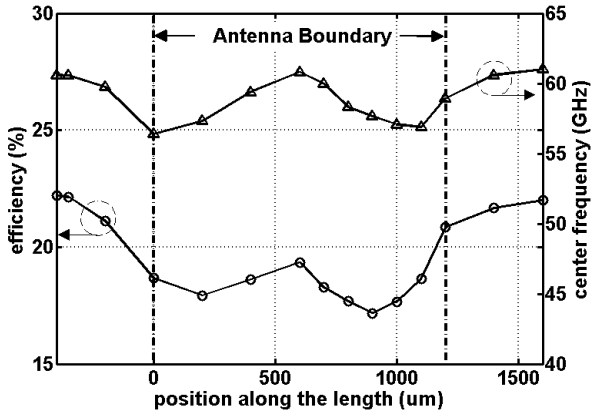

Figure 4. Efficiency and center frequency of the antenna versus the positions of a stripline composed of M6 and M7 along the length.

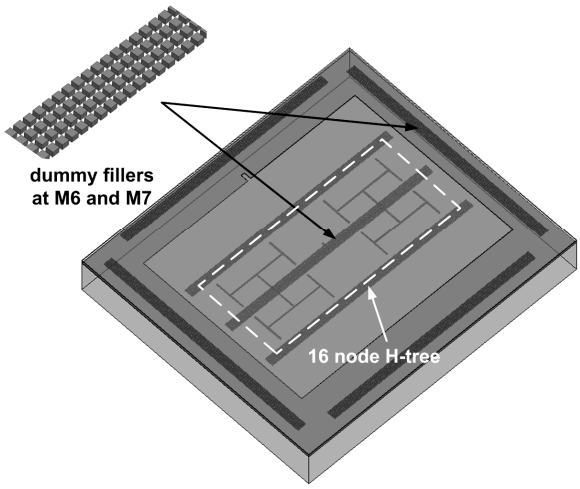

Figure 5. A practical dummy filling scheme with a 16-node H-tree design beneath the patch antenna in standard CMOS process.

B. *Dummy Metal Filling for Local Density Rule*

In order to be fabricated in a CMOS process, the drawn metal on every layer must meet a certain minimum density over a local checking area, and the local checking area is usually smaller than the size of the patch antenna. Dummy metal filler structures are therefore placed under the patch to meet this local density rule, but when placed under or around the antenna, they decrease the gain and vary the center frequency. Therefore, the fillers should be carefully placed to minimize the performance degradation. To analyze the impact of fill, we placed a 100 μm wide strip of metal fill along the width of the antenna (orthogonal to 60 GHz current flow), and swept the location of the strip along the length of the antenna. Fig. 4 shows the results of efficiency and center frequency when sweeping a strip composed of M6 and M7 along the length. The dash-dot line indicates the two radiation edges of the antenna; therefore fill is swept beyond the antenna boundaries. The results are consistent with the standing wave pattern, showing that if the fill is in the center of the patch area, where the electric field null is, then the strip has little effect on the antenna even though it is in between the patch and ground. Fig. 5 shows a practical dummy filling scheme to meet a 10% local minimum density rule over local 400 μm^2 areas stepped across the chip. The strips are composed of floating patch units, and the space between the units reduces the electrical induced current along the length caused by the standing wave on the patch. The results simulated by Ansoft HFSS show the fill reduces the radiation efficiency by 22%, and shifts the center frequency by 3%, with a 0.88 dB drop in peak antenna gain.

C. *Slotting for CMOS Design Rule*

Similar to the metal density rule, a CMOS process also enforces adding small cutouts, or slotting in extremely wide metal wires. The exact slot size depends on design rules, and there are typically fewer degrees of freedom for a designer on the placement of slots. However, to prevent current funneling in the patch antenna, the length of the slots should be oriented parallel to the length of the antenna. In this design, only the ground metal layer M4 needs to be slotted every 50 μm along the length and the width. The radiation efficiency is decreased by only 3% due to slotting of M4.

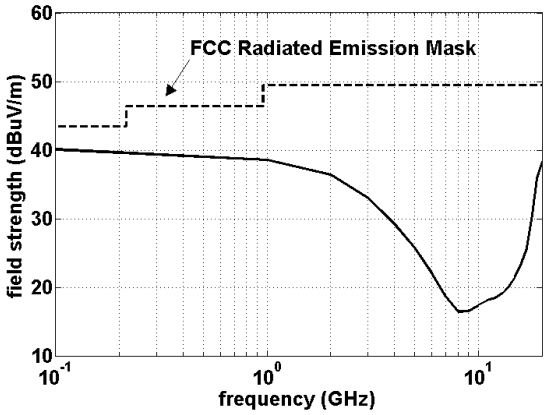

Figure 6. The radiated electric field strength of 1.2 V_{pp} clock signal coupled to the antenna.

IV. MUTUAL COUPLING IN THE SYSTEM

While the patch antenna and the digital circuits beneath are working simultaneously, the isolation for crosstalk between them is important. The digital signal could be picked up by the antenna, and then be radiated out causing the chip to exceed the FCC noise emission mask. Meanwhile, the RF signal may couple to the circuits beneath the patch ground, causing malfunction of the digital logic or feedback loops in the RF front-end. We will discuss the two coupling effects in the following sections.

A. *Coupling from the Circuit Beneath to the Antenna*

In the proposed integration scheme, the digital circuits are running at a lower frequency beneath the antenna, and the switching operations are considered as noise to the RF signal on the antenna. The noise source is modeled as a single, large node that injects clock noise onto the patch. Fig. 5 shows a 16-node clock H-tree at M3 integrated with the patch antenna, the global ground plane, and the dummy fillers. The H-tree is also designed according to the standing wave pattern so that the electromagnetic coupling will be minimized. It is more rectangular in parallel with the radiation edges, and stretching out from the middle of the antenna. Given a 2 GHz clock signal on the tree, an S-parameter analysis shows a -95 dB coupling back to the input port of the patch antenna. Furthermore, Fig. 6 shows the spectrum of radiated electric field strength due to 1.2 V_{pp} full-swing clock signal coupled from the H-tree to the antenna, and the field strengths are always within the mask of 10-m Class A digital device regulation defined by FCC from 100 MHz to 20 GHz [6].

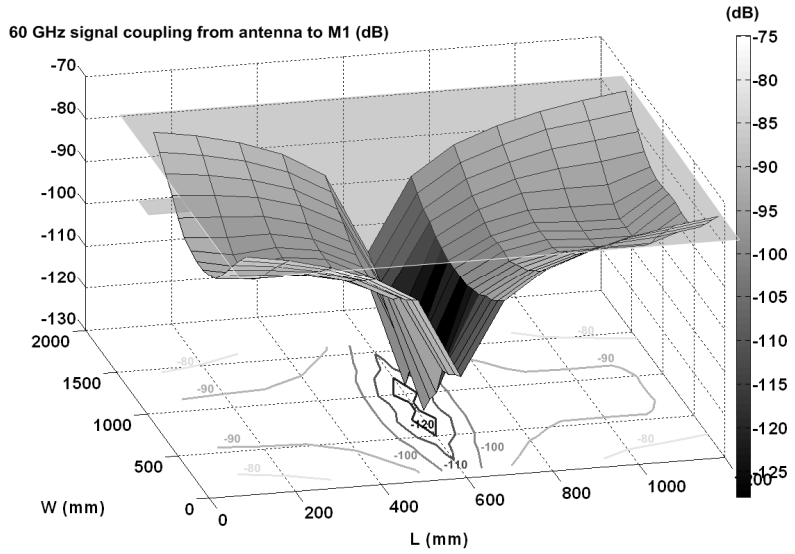

Figure 7. Contour of 60 GHz signal coupled from M8 patch antenna to M1.

B. Coupling from the Antenna to the Circuit Beneath

On the other hand, the circuits beneath the antenna ground plane need good isolation to function correctly. By S-parameter analysis, the 60 GHz signal coupling from the antenna input port to the H-tree is -61 dB. Usually, such high frequency signal coupled to the wire routing will be filtered out by the resistance and capacitances along the routing, and will not cause significant skew or jitter problems in the digital circuits. Moreover, a global contour of 60 GHz signal coupling from the antenna to M1 is reported in Fig. 7. It shows position-dependent coupling information for circuit placement, which is consistent with the standing wave pattern of the patch antenna. Finally, the performance of a realistic 60 GHz on-chip patch antenna design with a 16-node clock tree, ground plane and dummy fillers is summarized in Table II, and compared with the state-of-the-art mm-wave on-chip antennas in integrated wireless communication systems.

V. CONCLUSION

The systematic integration of 60 GHz on-chip antenna in standard CMOS 0.13 μm technology is presented in this paper. An area-efficient layout is proposed by exploiting the space beneath the patch ground plane for digital circuitry. The slotting and local metal density rules during the fabrication are discussed. Based on the standing wave pattern of the patch antenna, a field-dependent dummy filling scheme is provided to minimize the impact to antenna performance. Furthermore, the electromagnetic coupling effect from antenna to digital circuit routings beneath the ground plane is analyzed, and vice versa. In the end, a practical design that contains an antenna, a digital clock tree routings, and dummy fillers is demonstrated, showing a promising result for an area-efficient approach to wireless communication system integration.

TABLE II
SUMMARY OF MM-WAVE CMOS ON-CHIP ANTENNAS

	This work	[2]	[3]	[4]
Topology	Patch	Dipole	Patch	Slot
Post Process	Not needed	Needed	Not needed	Needed
Frequency (GHz)	60.51	79.80	62.80	60.00
Bandwidth (MHz)	810	2000	N/A	N/A
Peak Gain (dBi)	-3.32	2.00	-8.50	-2.00
Efficiency (%)	15.87	N/A	N/A	N/A
Area (mm^2)	1.22 x 1.58	0.02 x 1.15	1.70 x 1.30	N/A

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