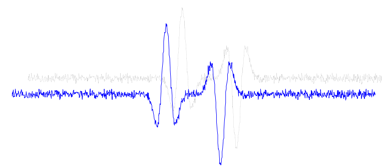
Direct Conversion Pulsed UWB Transceiver Architecture



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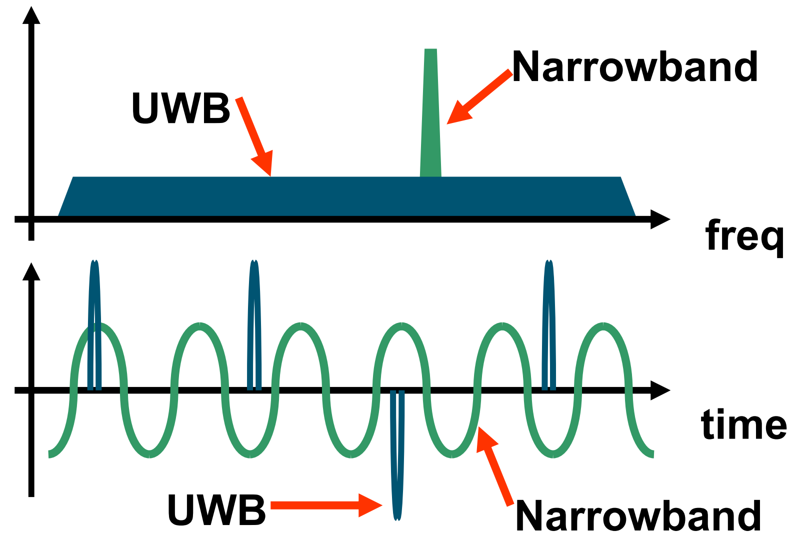
Massachusetts Institute of Technology

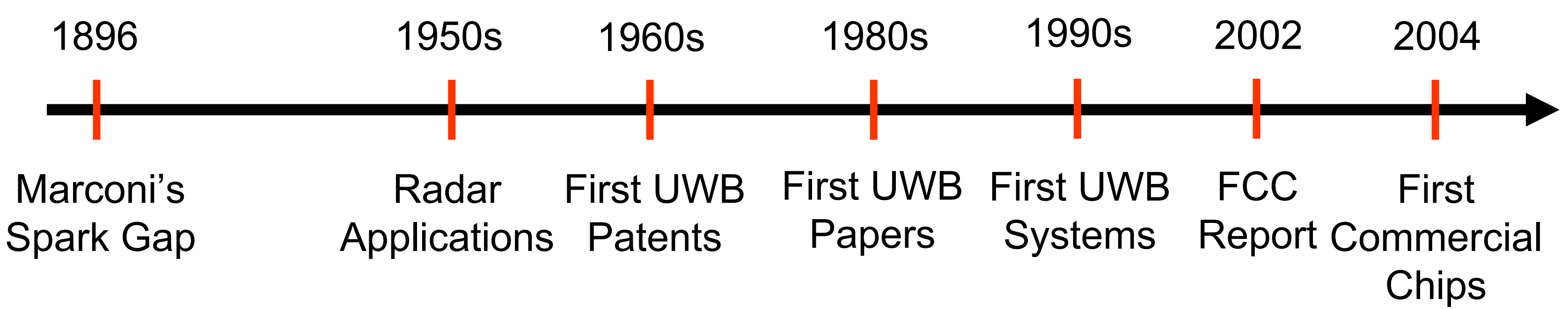
Outline

- Introduction
- Baseband Transceiver
- Direct Conversion Transceiver
- Conclussions

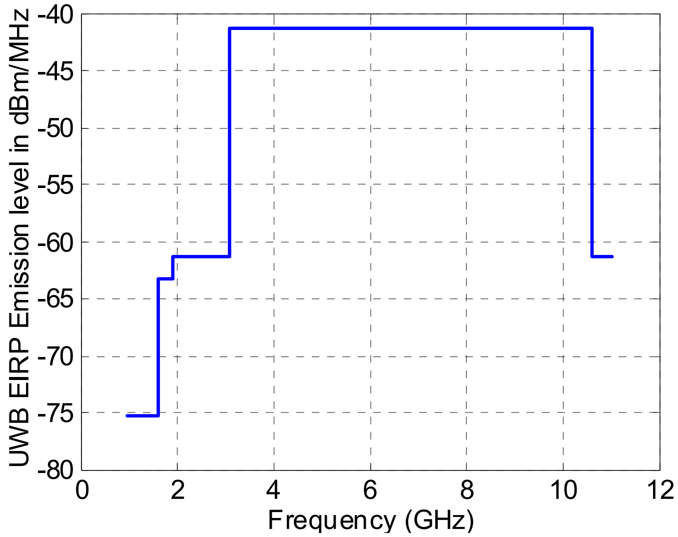
Initial Interpretation of UWB

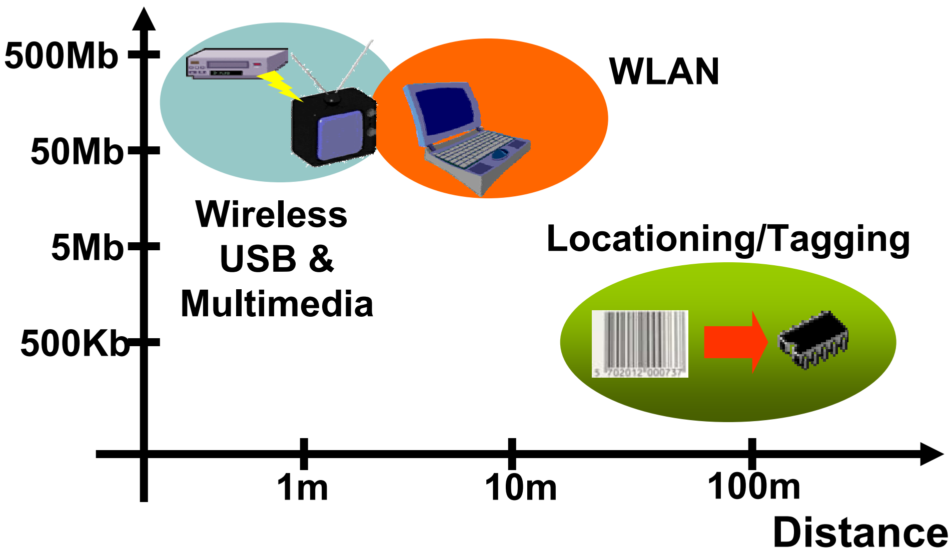
- High data rate.
- Low probability of interception.
- Excellent multipath resolution
- Low interference to preexisting services.
- Simplicity of implementation (low power, largely digital).





Regulation Issues





USA
7.5GHz of free unlicensed spectrum

Europe
Unregulated

Future UWB Standards

IEEE 802.15.3a

- **QoS**
- **High Data-Rate**
- 4 PicoNet in close proximity
- Cost

Distance	Bit Rate
10m	110Mbps
4m	200Mbps
1m	480Mbps

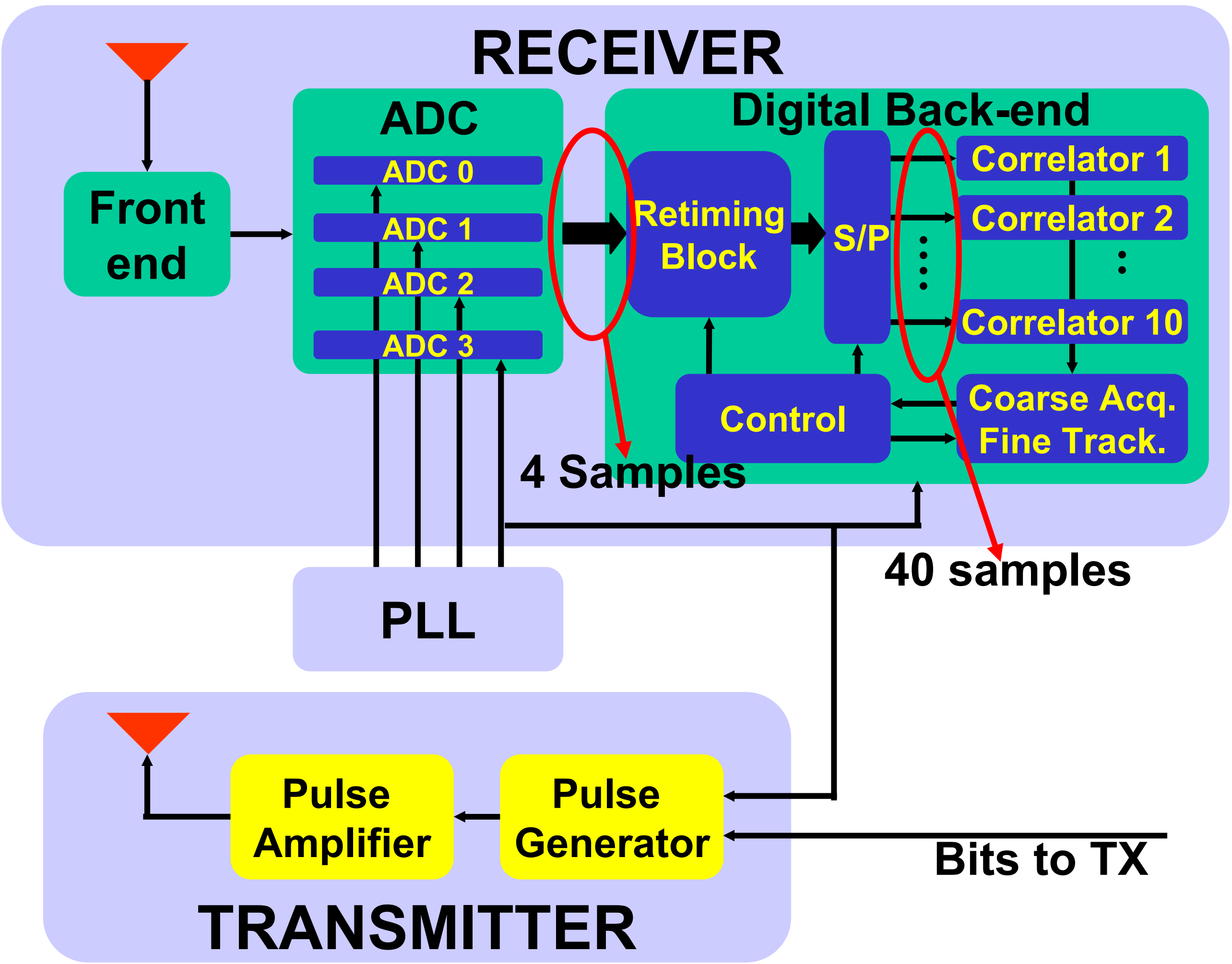
IEEE 802.15.4a

- **High Precision Location Capability**
- **Larger Range**
- Robust multipath performance
- Scalable Data Rate

Applications

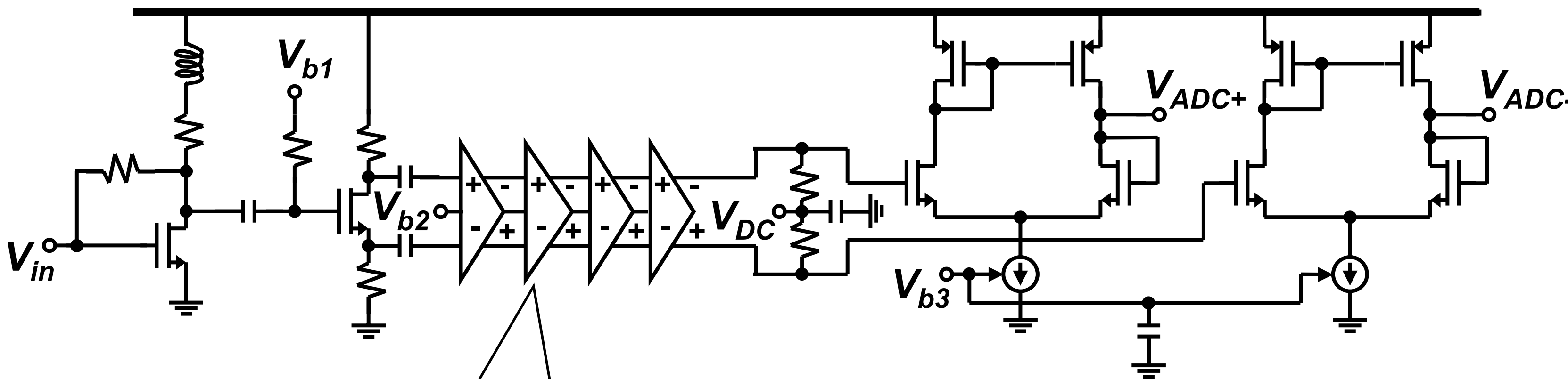
- Safety (Public/Military)
- Smart Buildings
- Item Locating/Tracking
- Networking

UWB Baseband Transceiver

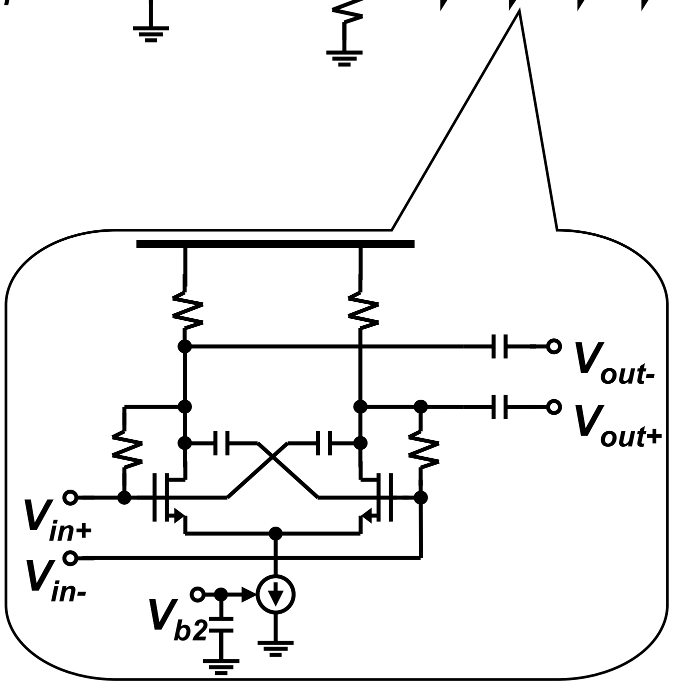


BW = 300MHz, Duty cycle = 2%, 31 pulses per bit

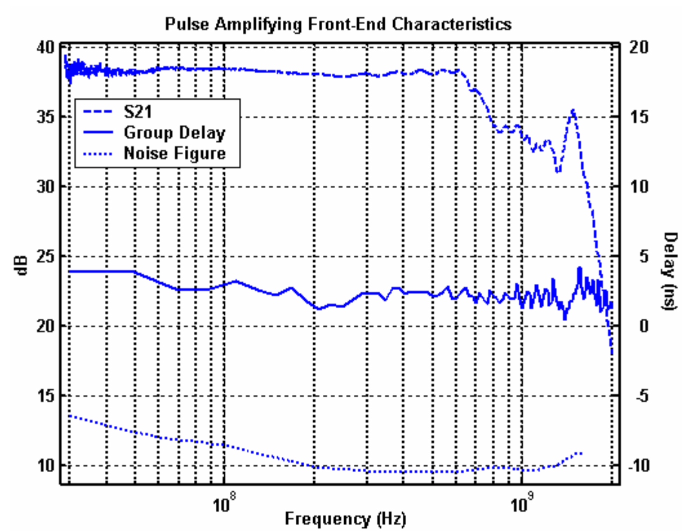
Front-end



V_{b1}
V_{in}
V_{b2}
V_{DC}
V_{ADC+}
V_{ADC-}
V_{b3}

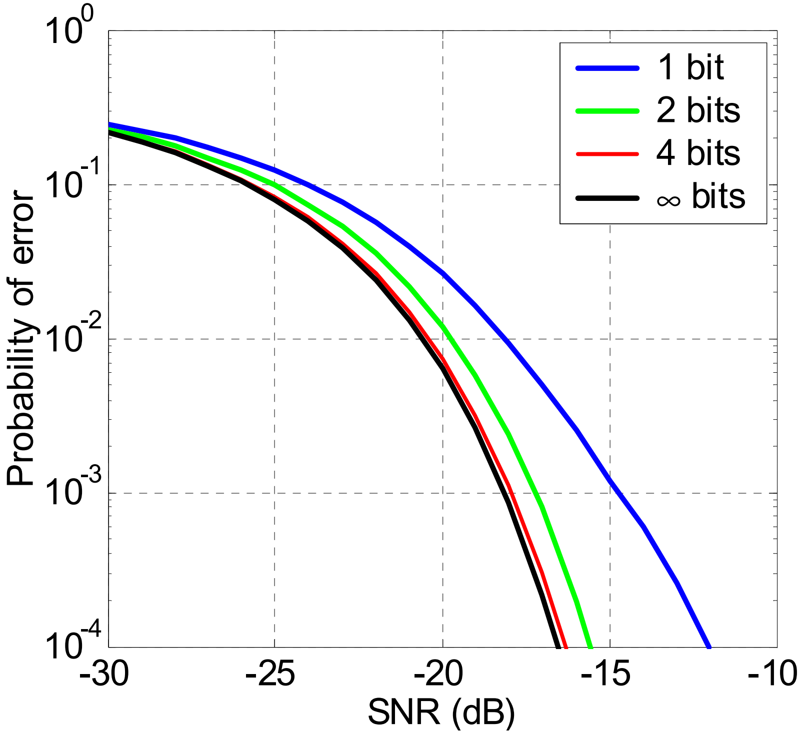


V_{out-}
V_{out+}
V_{in+}
V_{in-}
V_{b2}

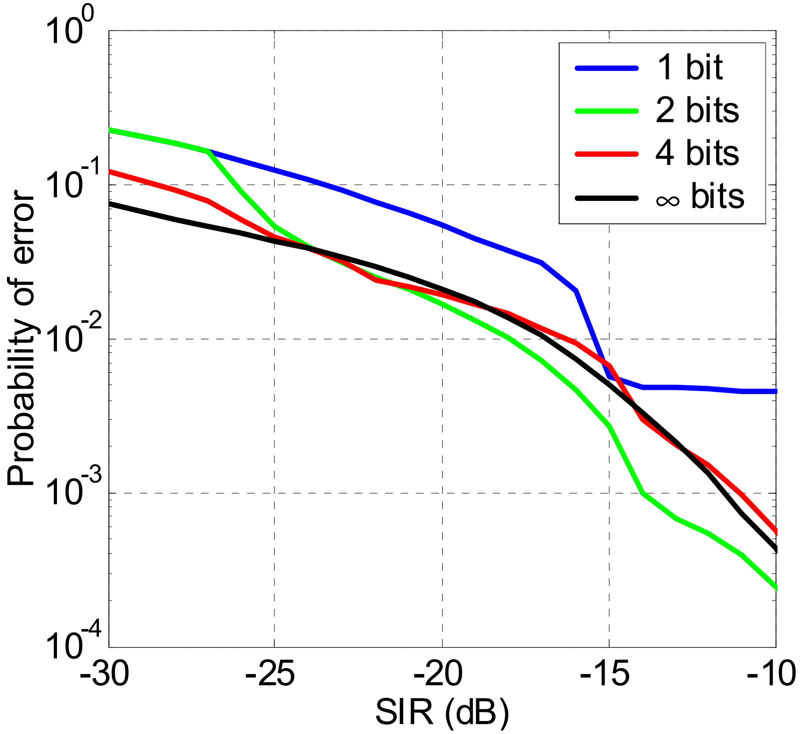


Pulse Amplifying Front-End Characteristics
S21
Group Delay
Noise Figure
dB
Delay (ns)
Frequency (Hz)
40
35
30
25
20
15
10
20
15
10
5
0
-5
-10
10^8
10^9

Specification of the ADC



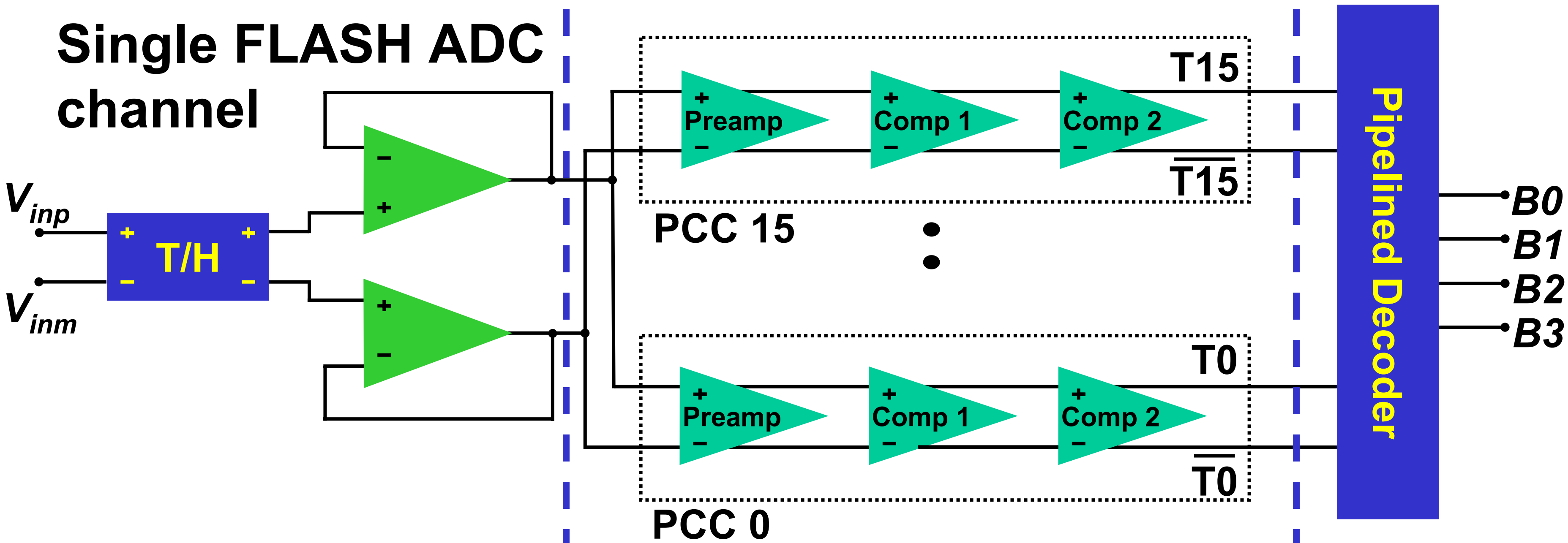
Noise Limited Case



Interference Limited Case

4 bits sufficient for reliable UWB detection

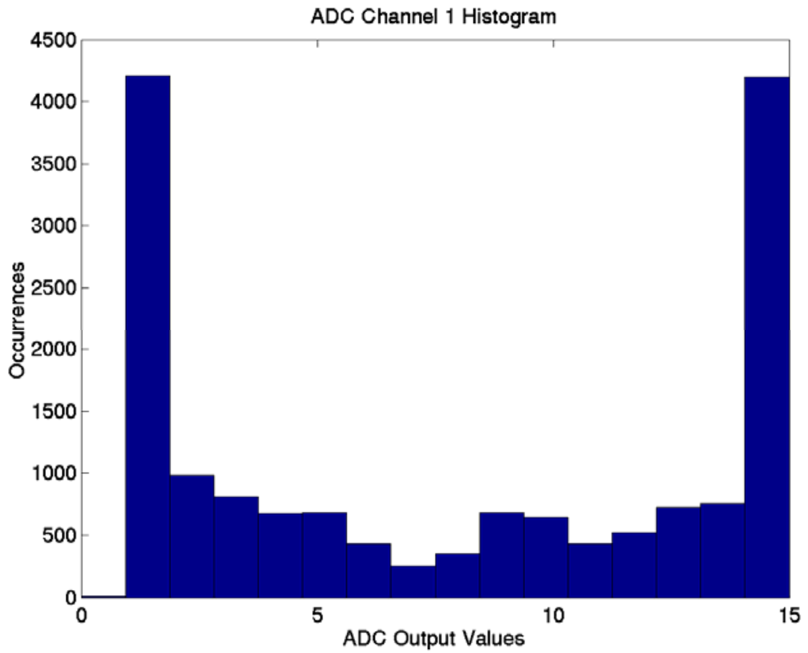
ADC Architecture

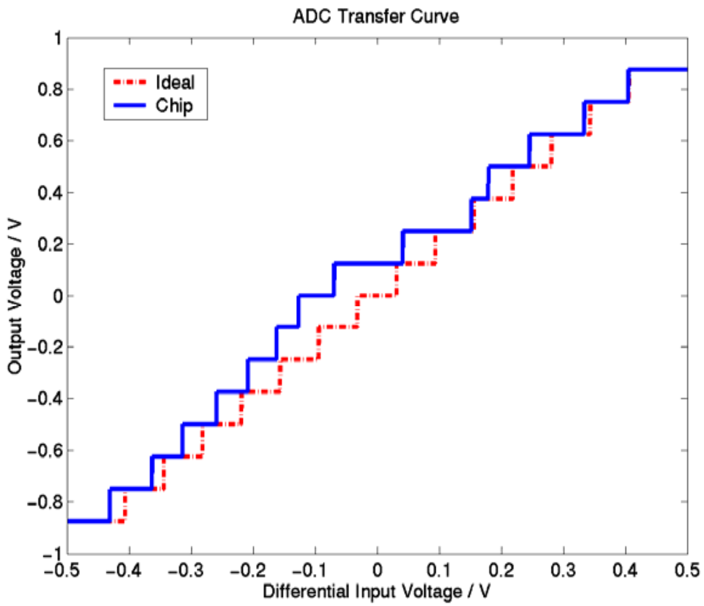


- Switch + Capacitor
- Better dynamic performance
- Low resolution

- Fully Differential Preamplifier and Comparators

ADC (Measurements)

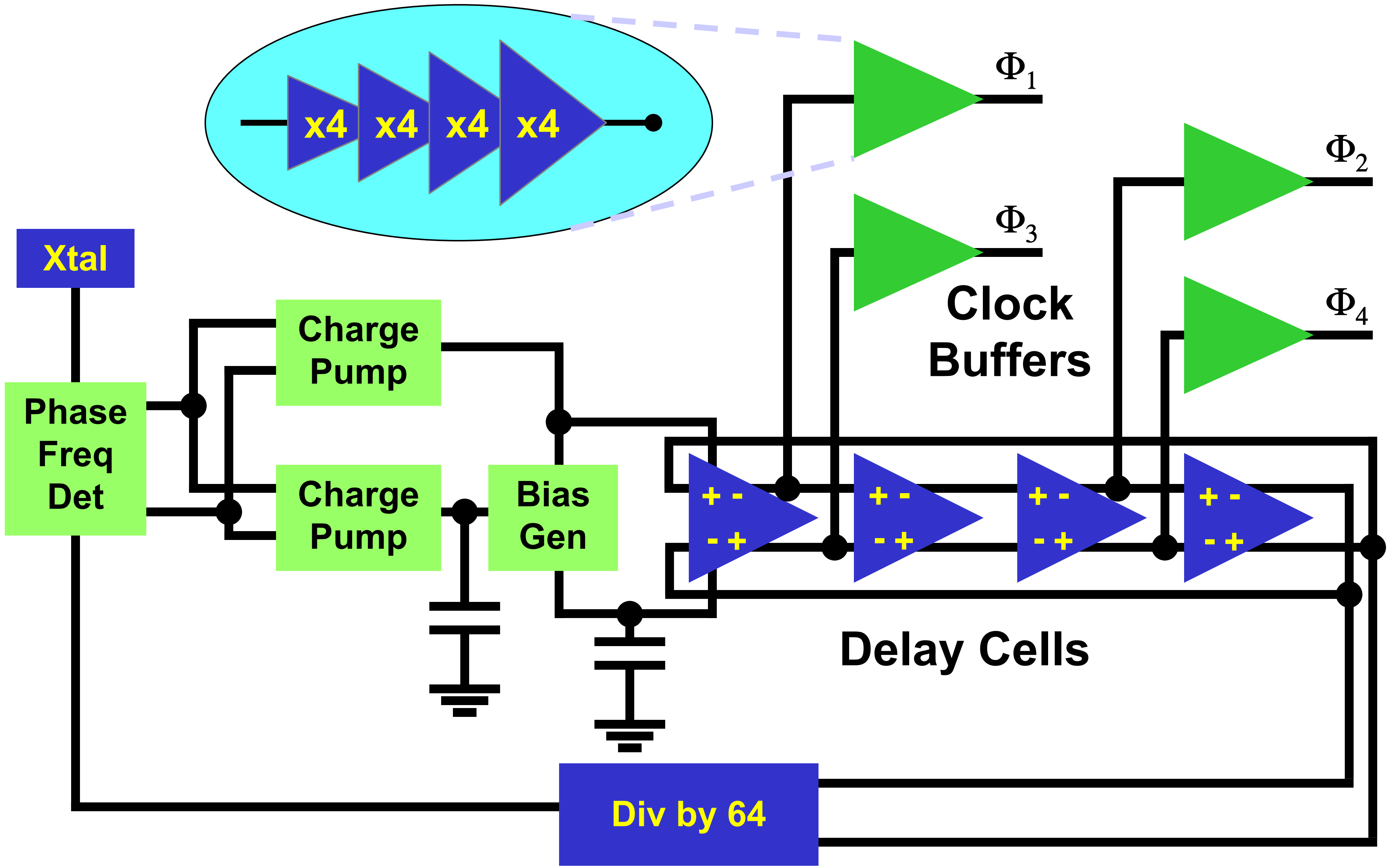




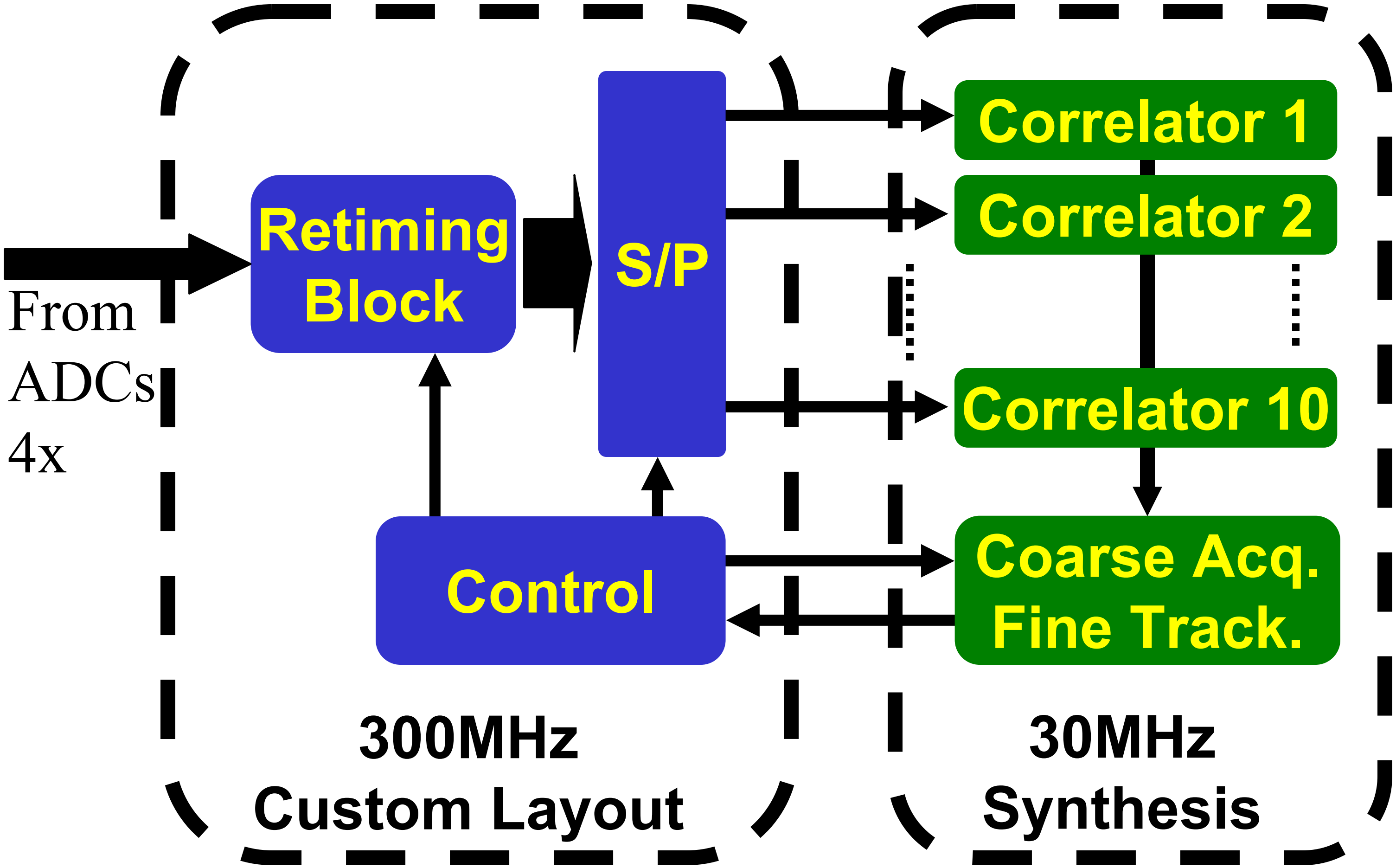
ADC Channel 1		
f_{CLK} / MHz	DNL_{ave} / LSB	INL_{ave} / LSB
250	0.31	0.62
384	0.31	0.62

Dornberg, J., Lee, H.S. and Hodges, D.A., "Full-Speed Testing of A/D Converters", IEEE JSSC, Dec 1984.

Clock Generation Subsystem



Digital Backend Specification



Whole synchronization in digital domain.
Coarse Acquisition < 70μs, Fine Tracking Precision = 1sample

Coarse Acquisition

- **Wider integration window?**

  2 samples per pulse

  N_c pulses per bit

Case 1: 1window ⇒ Width N

$2N_cN$ multiplications

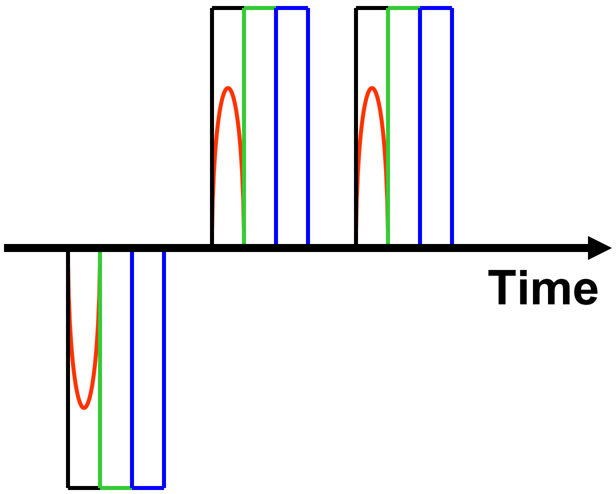
$2N_cN$-1 additions

Case 2: N windows ⇒ Width 1

$2N_cN$ multiplications

$2N_cN$-N additions

PARALLELIZATION



Loss = 1.7dB

Time to Coarse Acq. 70 μs

50 correlations in parallel

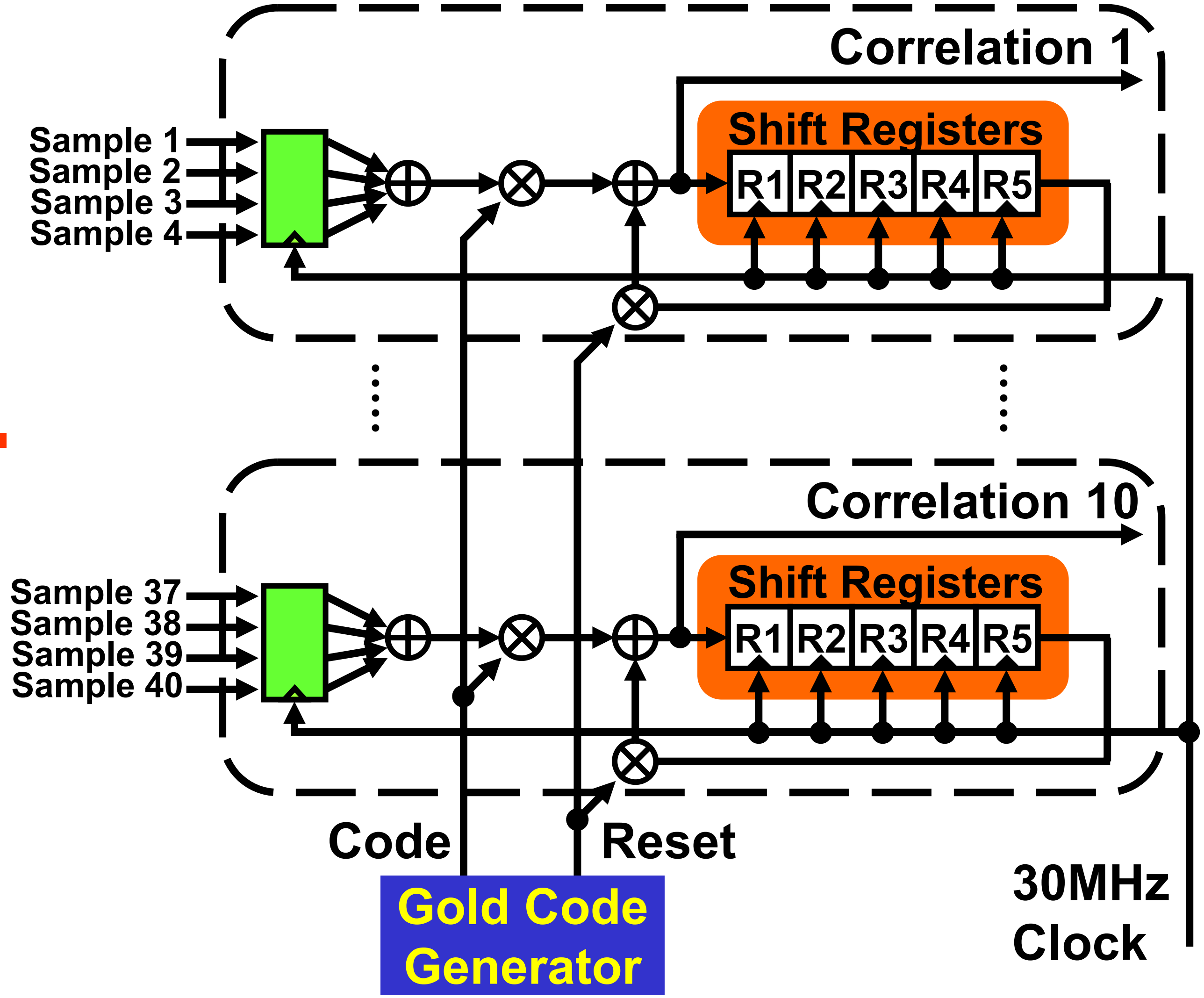
Correlators

1 Correlation:

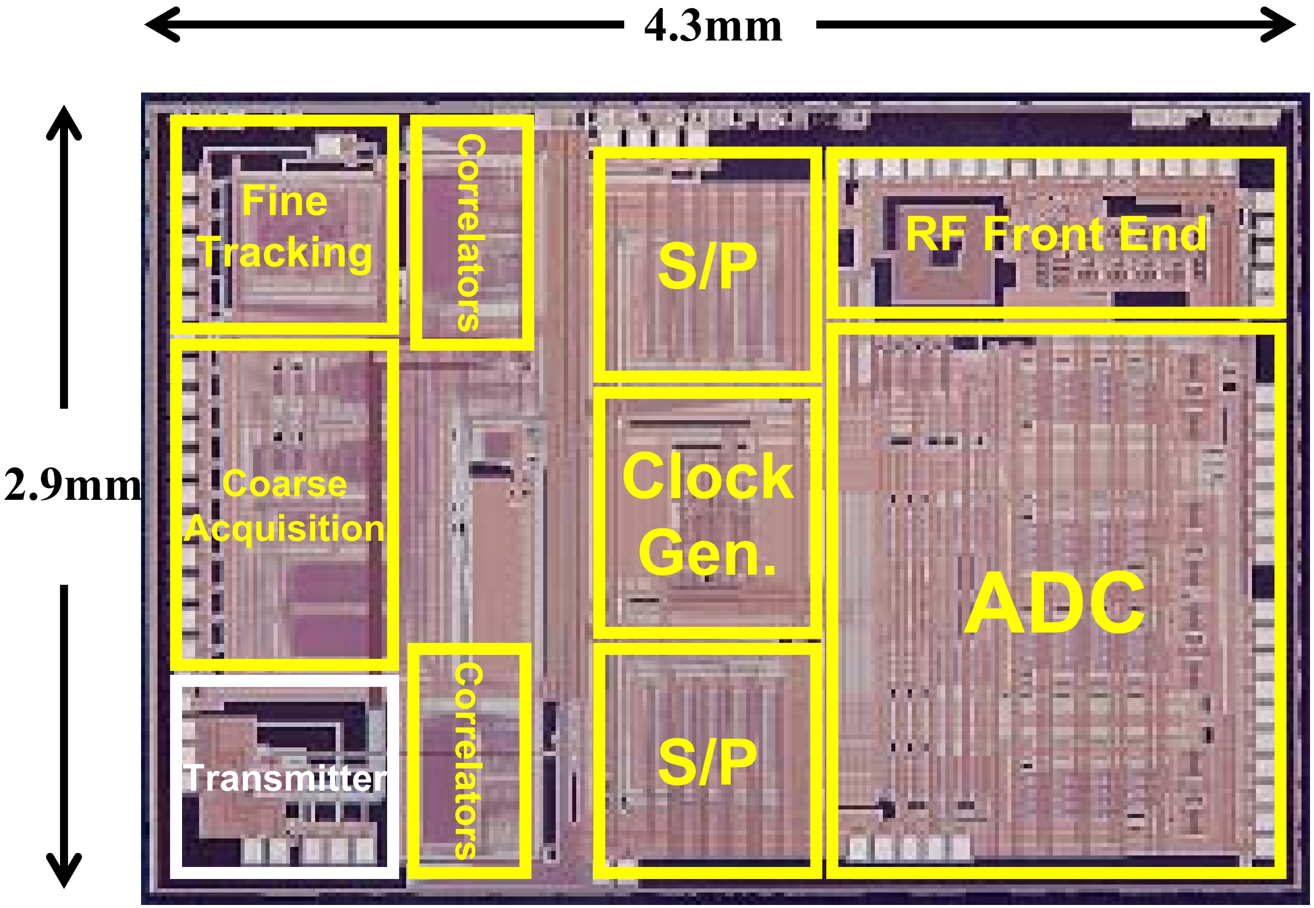
200 samp/frame
31 frames

= 6200 FIR coeffs

50 Correlations in parallel



UWB System on a Chip

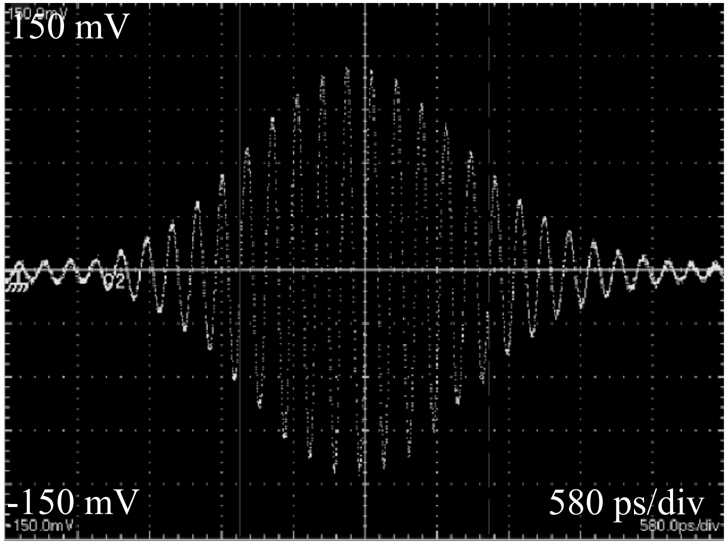


Power Consumption	
Transmitter	5mW
RF Front-end	71mW
ADC	86mW
PLL	45mW
CLK Buffers	65mW
Backend	75mW
Total	347mW

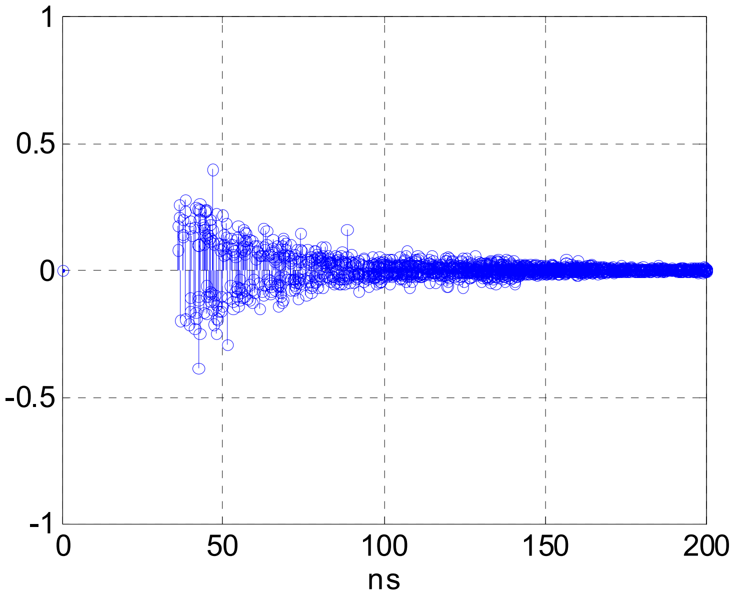
1.8 V - 0.18µm non-epi
Demonstrated 193kbps wireless link

The UWB Channel

- BW_{min} = 500 MHz
- Limitations:
  - In band interferers. (802.11a)
  - Multipath.

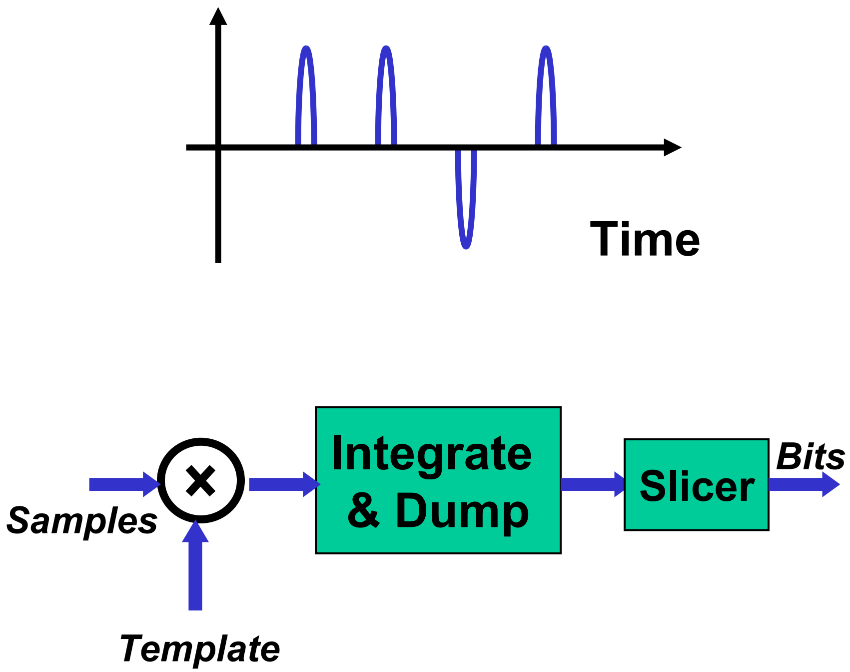


	Description	RMS Delay
CM1	LOS 0-4m	5.3ns
CM2	NLOS 0-4m	8.0ns
CM3	NLOS 4-10m	14.3ns
CM4	Extreme NLOS	25ns



Two Proposals for 802.15.3a

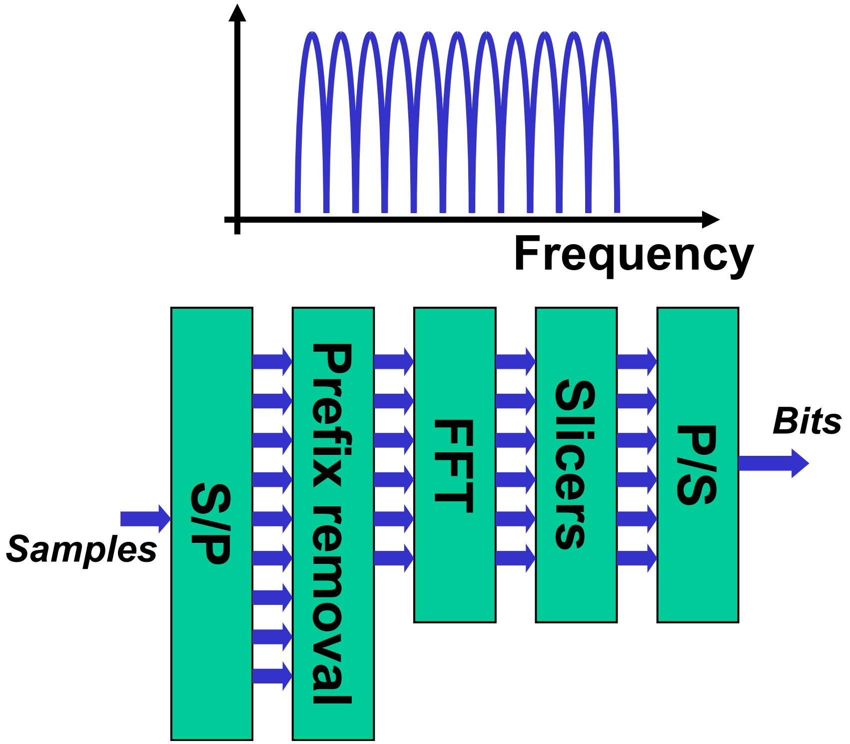
Pulsed UWB



Simple Transmitter
Good behaviour with non-linearities

ISI ⇒ Viterbi-like MLSE Equalizer

MB-OFDM



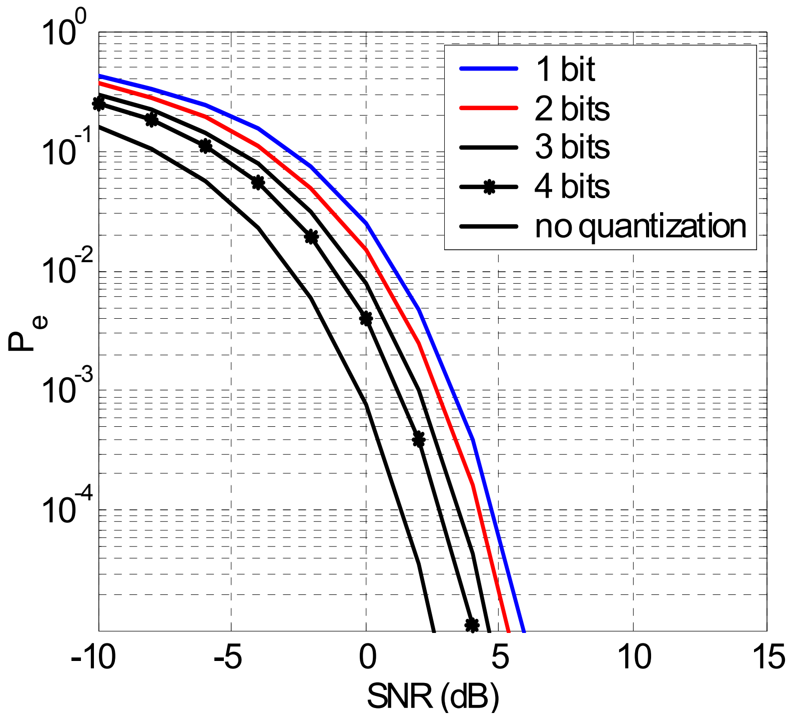
Elegant Equalization
Similar to 802.11a

Linearity required

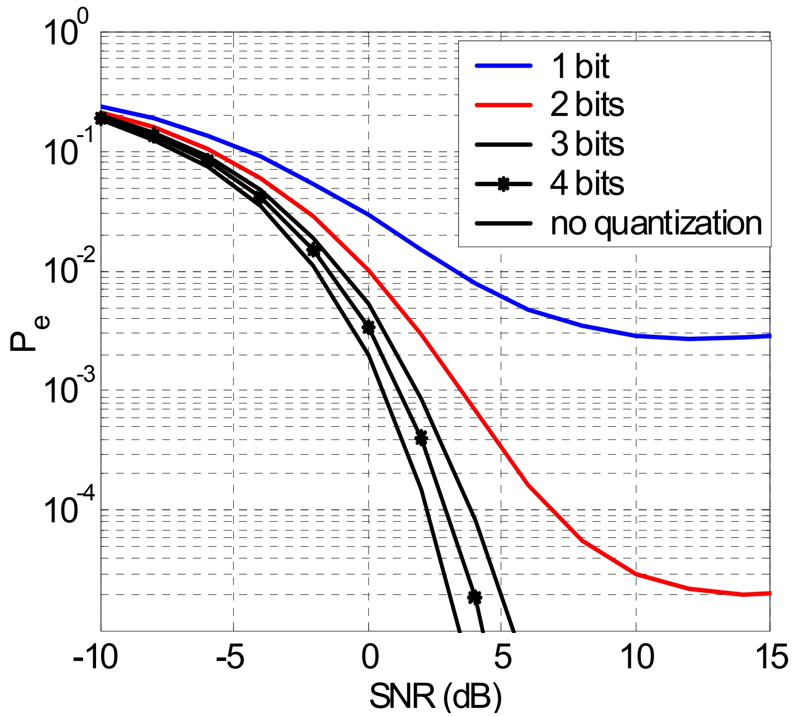
FCC to rule on this dispute next week

ADC Impact in UWB Signals

Pulsed UWB



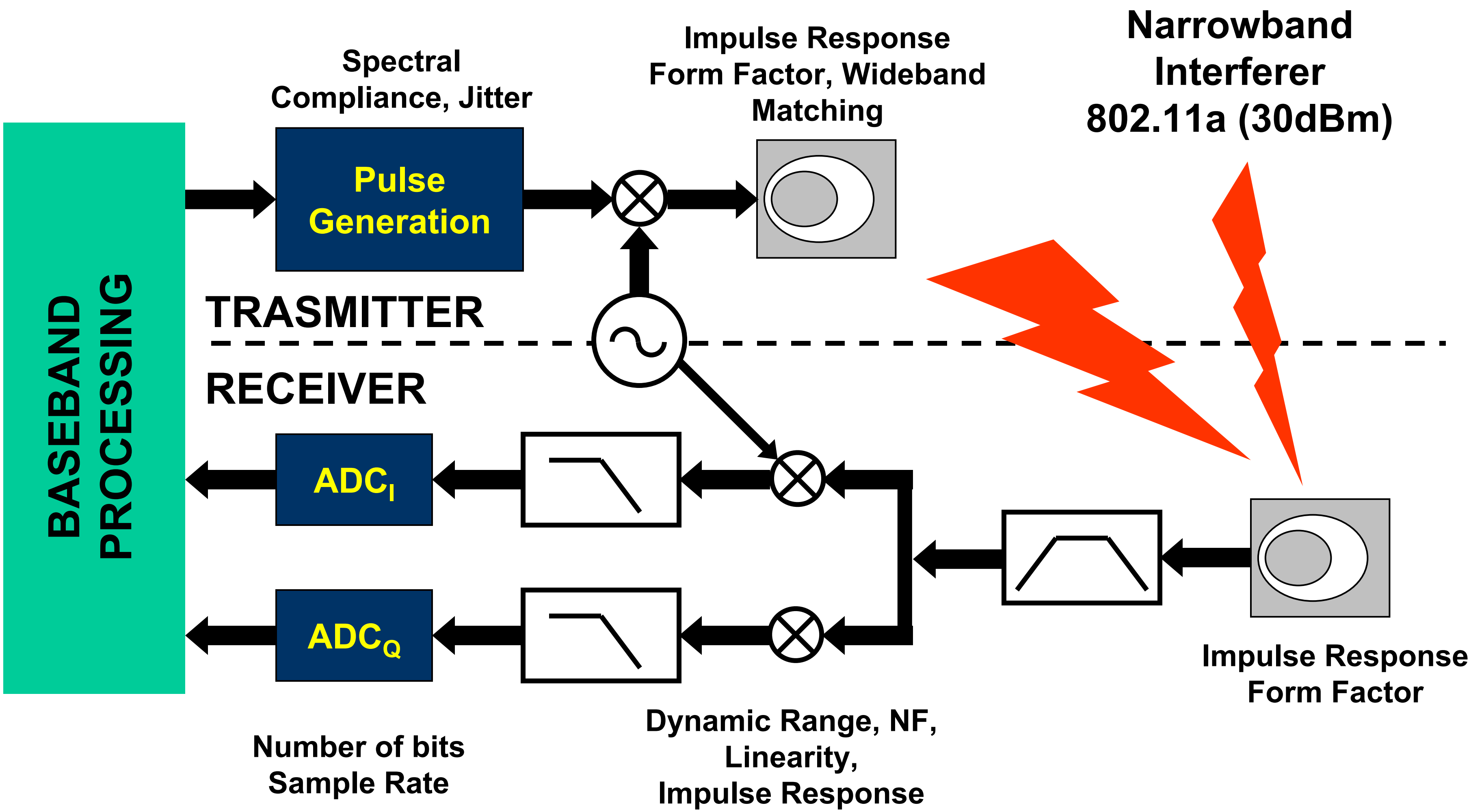
MB-OFDM



Solution: Coding

R. Blazquez, F. S. Lee, D. D. Wentzloff, P. P. Newaskar, J. D. Powell, A. P. Chandrakasan, "Digital architecture for an ultra-wideband radio receiver", VTC Fall 2003, Orlando FA, October 2003.

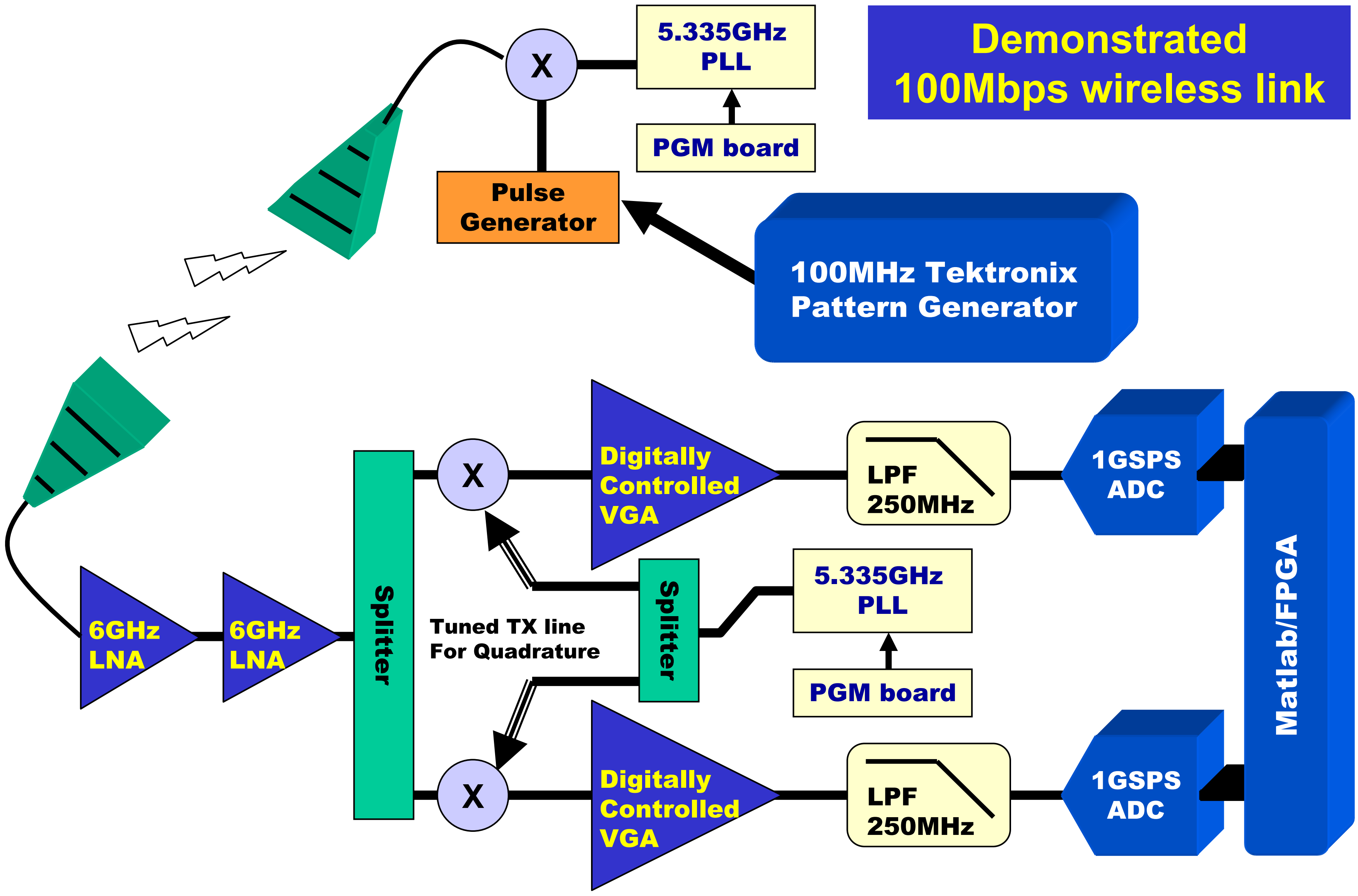
Direct Conversion Receiver



Power Budget for a UWB Transceiver

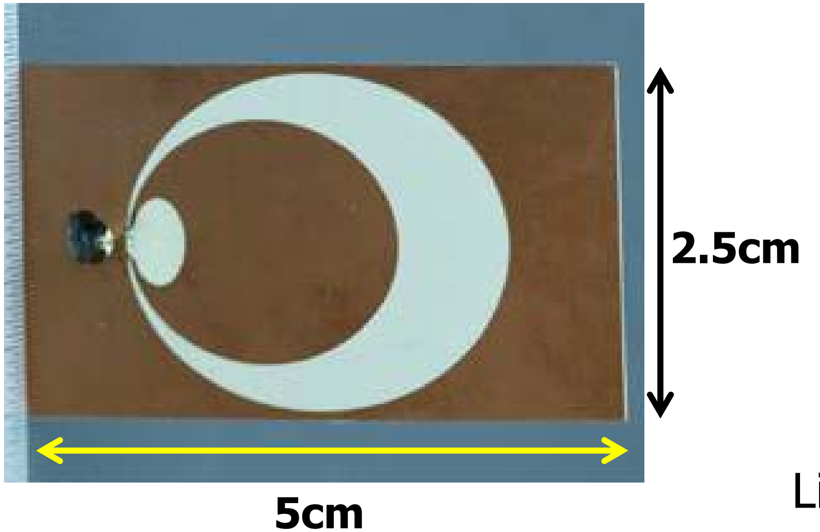
- MB-OFDM :
  - Front-end: 117.5 mW (Bergervoet et al. ISSCC'05) (SiGe BiCMOS 0.25)
  - Clock and carrier generation: 73.44 mW (Leenaerts et al. ISSCC'05) (SiGe BiCMOS 0.25)
  - Digital Back-end: 523 mW (Liu et al. ISSCC'05) (CMOS 0.18)
  - Estimated for 90nm CMOS (MBOA White paper): 93mW in transmission, 169mW in reception
- Pulse UWB (DSSS)
  - Total: 280mW (Iida et al. ISSCC'05) (CMOS 0.18)

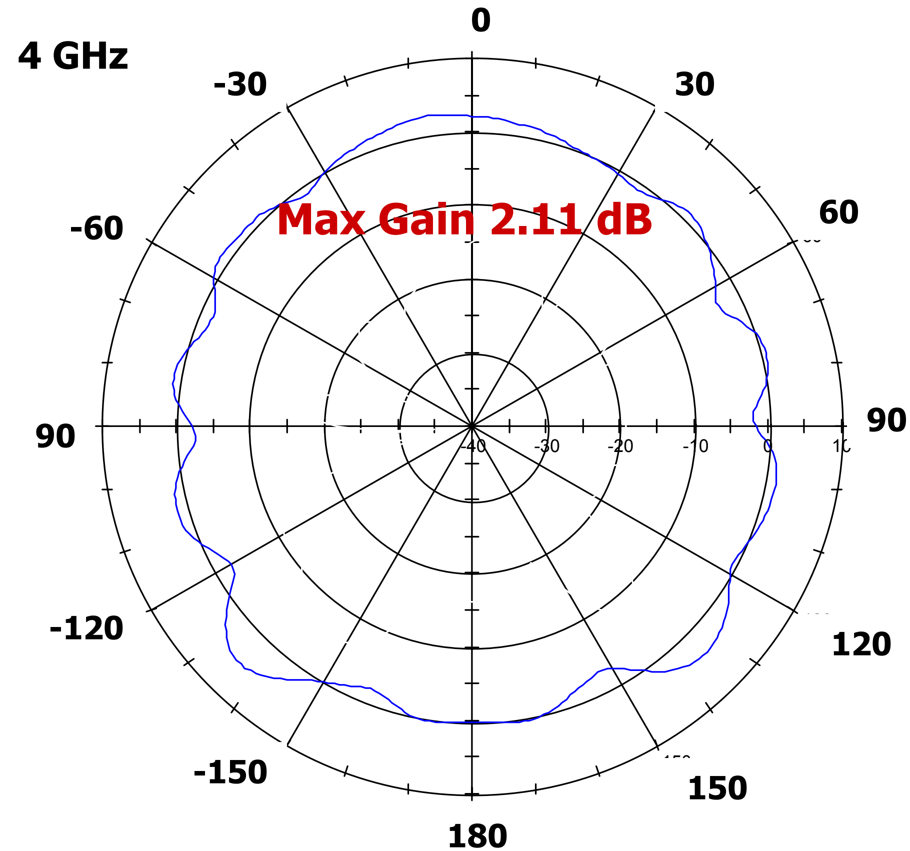
Discrete Prototype



Antenna

- VSWR < 2 for 3.1- 10.6 GHz
- Near Omnidirectional Pattern
- High Radiation Efficiency
- Physically Small Size
- Short impulse response

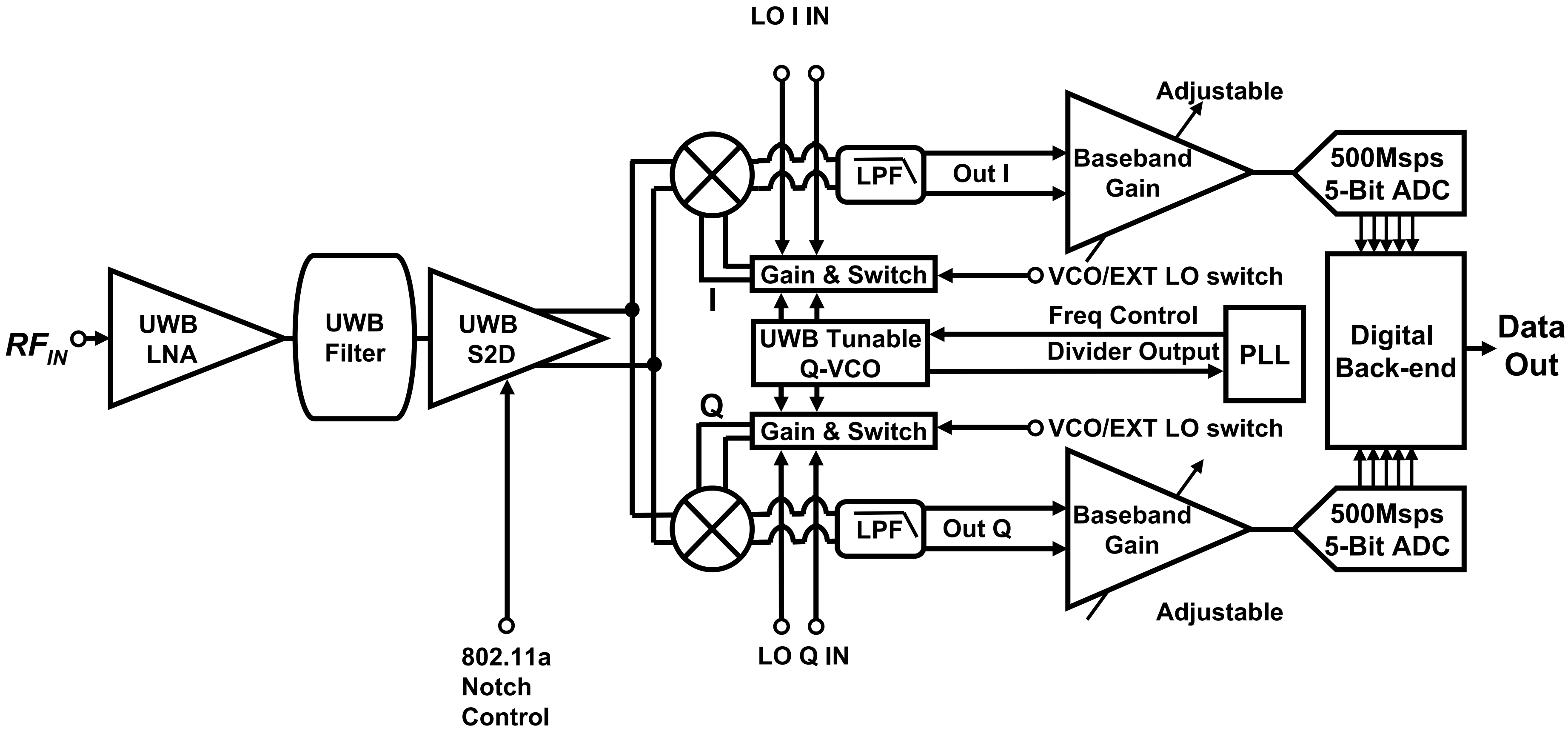




Lincoln Laboratory Measured Azimuth Pattern

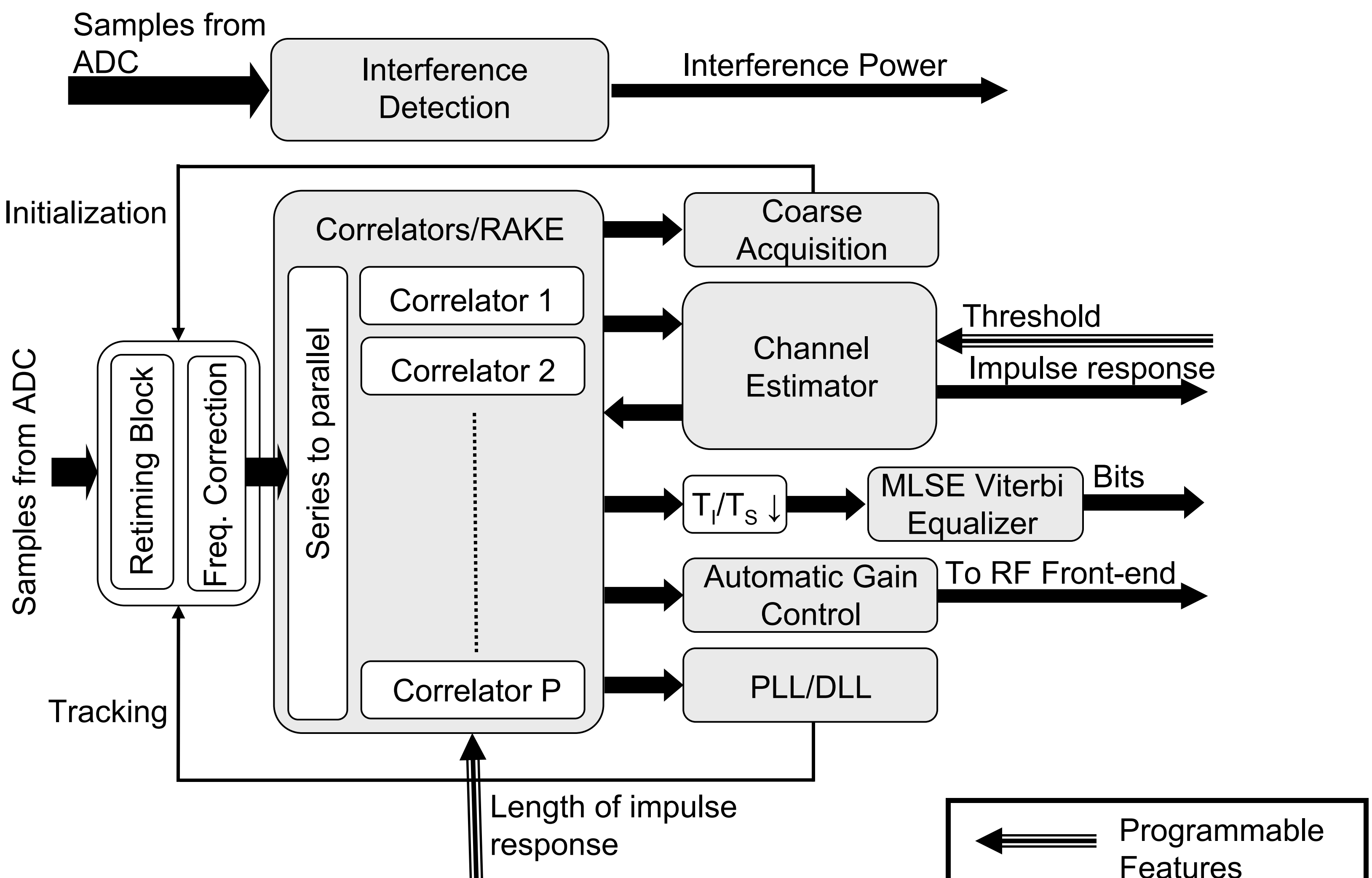
Johnna Powell, Anantha P. Chandrakasan, "Differential and Single Ended Elliptical Antennas for 3.1-10.6 GHz UWB Communication", IEEE Antennas and Propagation Society International Symposium, June 2004.

RF Front-end



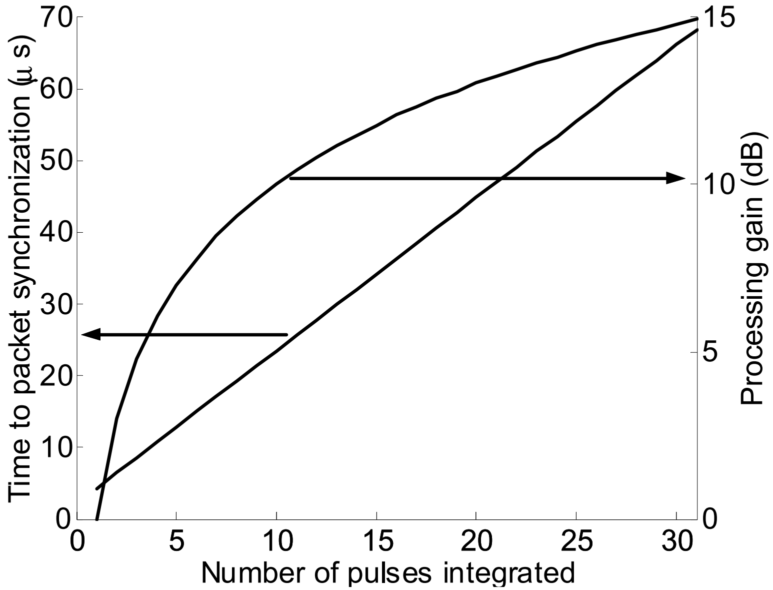
LO I IN
Adjustable
LPF
Out I
Baseband Gain
500Msps 5-Bit ADC
Gain & Switch
VCO/EXT LO switch
I
Freq Control
PLL
UWB Tunable Q-VCO
Divider Output
Digital Back-end
Data Out
RF IN
UWB LNA
UWB Filter
UWB S2D
Q
Gain & Switch
VCO/EXT LO switch
LPF
Out Q
Baseband Gain
500Msps 5-Bit ADC
Adjustable
802.11a Notch Control
LO Q IN

Programmable Baseband

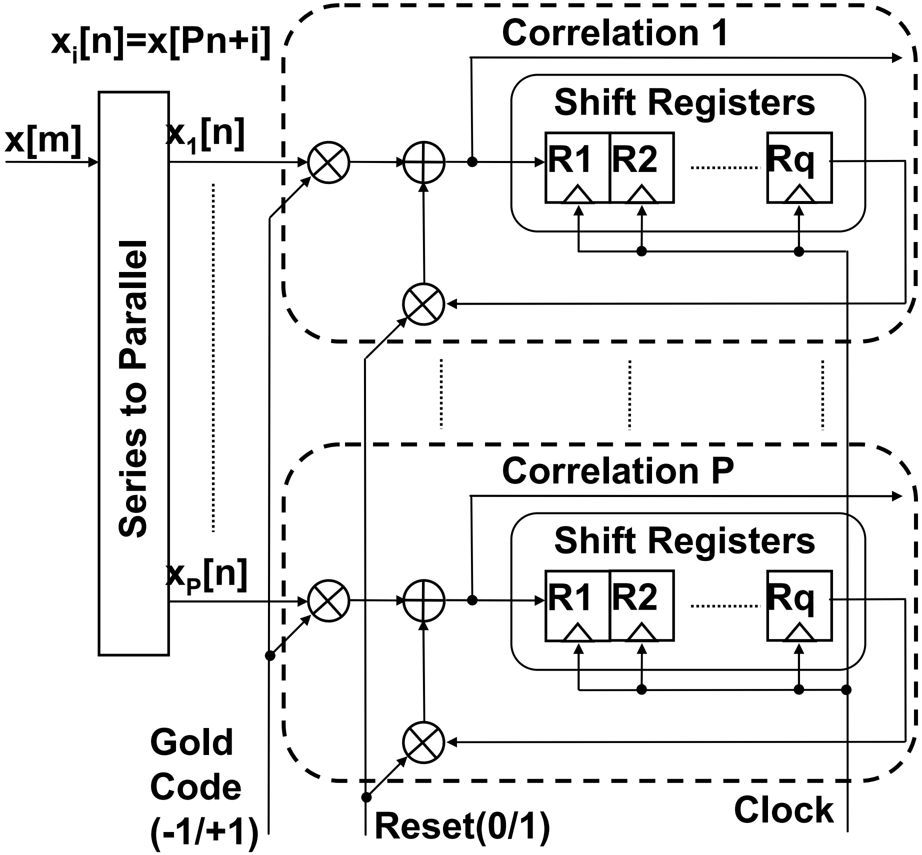


Parallellization

- Faster acquisition.
- Slower clock. Lower Vdd.

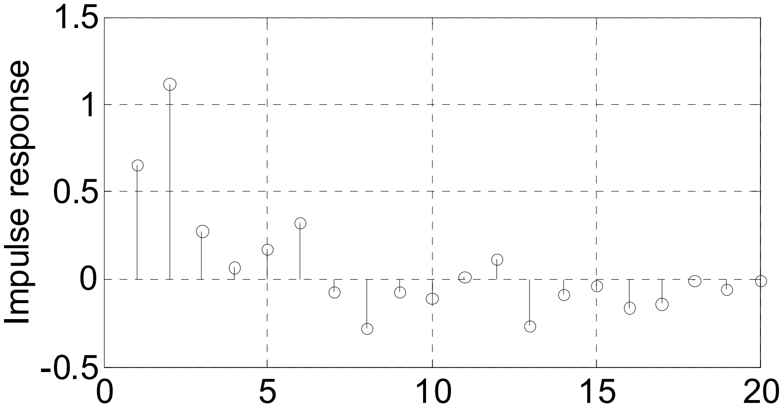


Coarse Acquisition Trade-off



Correlators Architecture

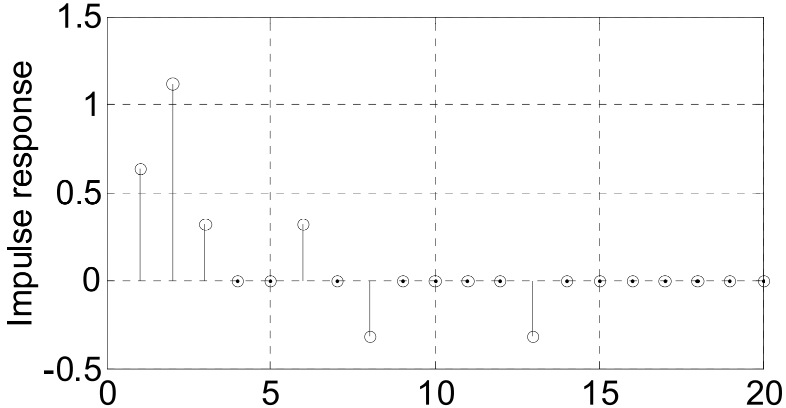
Rake Receiver



Channel Impulse Response (with multipath effects)

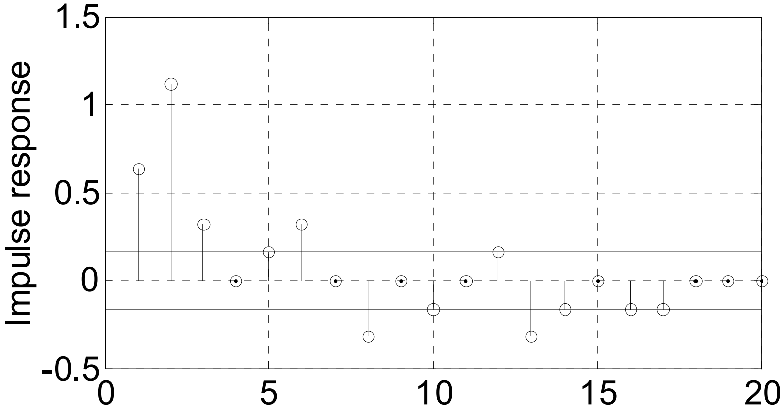
6 finger RAKE

Number of fingers fixed



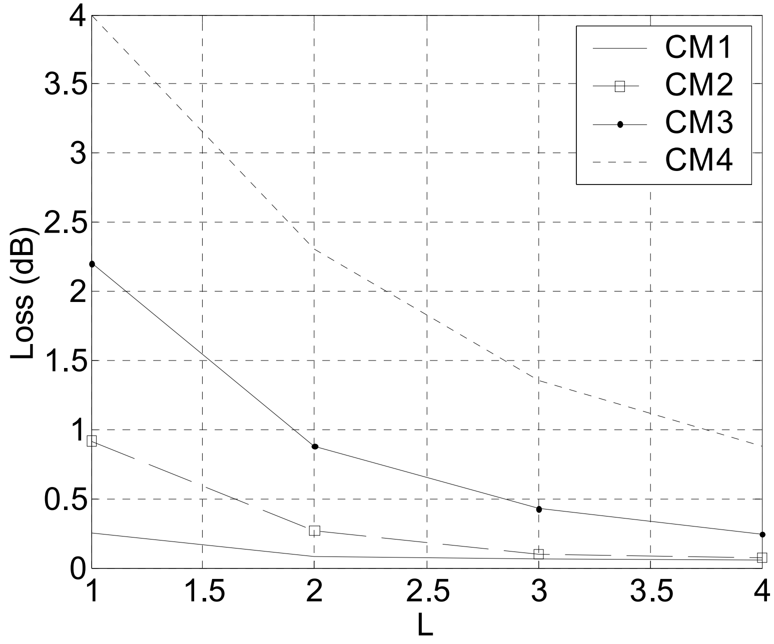
Method implemented

Variable number of fingers based on relative amplitude of response.



Adapting to the Channel

- Digital baseband estimates channel properties:
  - Interference (ISR)
  - Multipath (Impulse Response)
  - Signal power
- Controls over signal processing:
  - Number of states of equalizer.
  - Number of bits of ADC.
  - Threshold of the channel.



NUMBER OF STATES OF MLSE EQ.

KNOBS AVAILABLE TO ADAPT THE COMPLEXITY TO THE CHANNEL QUALITY

Conclusions

- SoC implementation is difficult.
- Higher data rate implies complexity.
- Parallellization allows power reduction.
- Adapt the complexity of the transceiver to channel quality.