A 150 µW -57.5 dBm-Sensitivity Bluetooth Low-Energy Back-Channel Receiver with LO Frequency Hopping

Abdullah Alghaihab[*1], Jacob Breiholz[†2], Hun-Seok Kim[*3], Ben Calhoun[†4], David D. Wentzloff[*5]
[*]University of Michigan, Ann Arbor, MI, USA
[†]University of Virginia, Charlottesville, VA, USA
{[1]abdulalg, [3]hunseok, [5]wentzlof}@umich.edu, {[2]jsb4ns, [4]bcalhoun}@virginia.edu

***Abstract*— A low power backchannel BLE wake-up receiver is presented. The receiver monitors the BLE advertising channels for a pre-programmed pattern. As in the BLE standard, frequency shift modulation (FSK) is chosen to be the modulation scheme of the signal that will be received. This makes the wake-up algorithm compatible with the standard, and hence, it can be generated by a commercial off-the-shelf device. The proposed receiver uses a dual-mixer to down-convert the RF input to reduce the LO power consumption by operating it at half the RF frequency. The receiver has a -57.5 dBm sensitivity while consuming 150 µW.**

***Index Terms*— Backchannel Communication, Bluetooth Low Energy, Dual Mixing, Frequency Hopping, Low Power Radio.**

I. INTRODUCTION

The Bluetooth Low Energy (BLE) standard provides a low power solution to connect IoT nodes with mobile devices, however the power of maintaining a connection with a reasonable latency remains the limiting factor defining lifetime of event-driven BLE devices. BLE radio power consumption is in the milliwatt range [1,2], and can be duty-cycled for average powers around 30µW, but at the expense of long latency. Recent work presents the concept of BLE back-channel (BC) communication as a wakeup mechanism that bridges the gap between ultra-low power and standard compliant BLE radios [3]. This provides a low-power receive mode without compromising on latency but it is also susceptible to interference in the crowded 2.4 GHz band as it senses the signal without discriminating between sources using different BLE channels. This work presents a 150 µW BLE back-channel receiver with a dual-mixer front-end to save power by using an LO at half the RF frequency, and improve selectivity through direct-conversion and filtering. The BC-RX implements FSK communication by detecting the hopping sequence on the three BLE advertising channels, which is compatible with the BLE standard.

Fig.1 shows the top level block diagram of the FSK BLE back-channel receiver. A mixer-first architecture is used to avoid a high power RF LNA at 2.4 GHz. A dual mixer is used to set the LO at half of the input RF frequency,

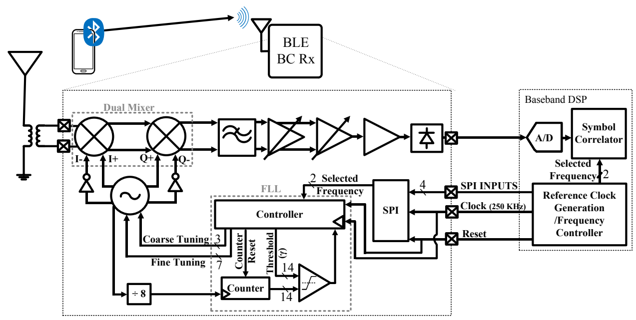

Fig.1 Block diagram of the BLE back-channel receiver.

leading to significant power savings in the LO generation block and its buffers (Fig.2). The direct down-converted baseband signal is then amplified and filtered to enhance the receiver selectivity. The signal is then envelope detected before digitizing it. The FLL programming for a specific frequency hopping sequence is performed by the external baseband DSP through SPI (Fig. 1). Off-chip, the receiver digitized output is correlated with pre-defined templates for each possible BC symbol by the external baseband DSP. Different BC symbols can be defined based on the frequency hopping sequence of advertising events and their timing gaps. As an additional feature to this design, a pre-defined sequence of BC symbols can be used as a wake-up message. The message is valid when the symbol time-stamps are within the allowed time gaps defined by the BLE standard. Consequently, our receiver can wake-up with a BLE compatible message sent by a mobile device.

II. BACK-CHANNEL BLE COMMUNICATION

The concept of back-channel BLE communication is illustrated in Fig.3. Our proposed system architecture is designed to detect the energy at the three BLE advertising channels by hopping between them. These channels are CH37, CH38 and CH39 located at the frequencies 2402, 2426 and 2480 MHz, respectively. An advertising event consists of three packets separated by less than 10 msec. Each packet length can be between 128 to 376 µsec (Fig.3 shows a 300 µsec packet for illustration). The delay between advertising events can be in the range from 20 ms

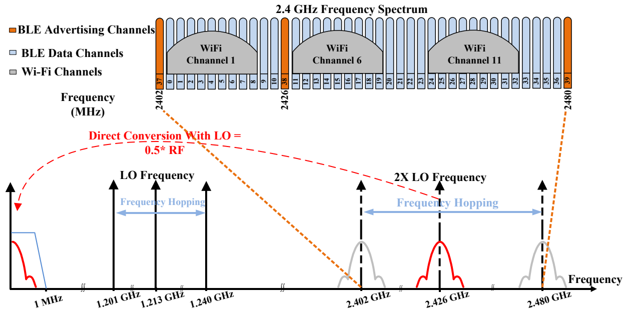

Fig.2 Spectrum allocations for BLE and WiFi channels and frequency spectrum of RF signal down-conversion with dual mixer.

to 10.24 sec in addition to up to 10 msec of pseudorandom delay to avoid collisions. With BC modulation, the information is encoded into the sequence order and timing gaps between advertising packet transmissions at different advertising channels, within a single advertising event. To achieve the targeted selectivity and improve the interference rejection, the receiver bandwidth is limited to 2 MHz, which is equal to the BLE channel bandwidth. To cover all three BLE advertising channels (up to 78 MHz apart), the Rx FLL hops its frequency between the three frequencies of the BLE advertising channels. Depending on the LO frequency hopping speed, the back-channel communication uses either a fast or slow mode. In the fast mode, the LO hopping speed is at least $2/T_{packet}$ to ensure capturing each packet's frequency. On the other hand, in the slow mode, the hopping speed is less than $2/T_{event}$ to ensure capturing a complete advertising event comprising transmissions in all three channels.

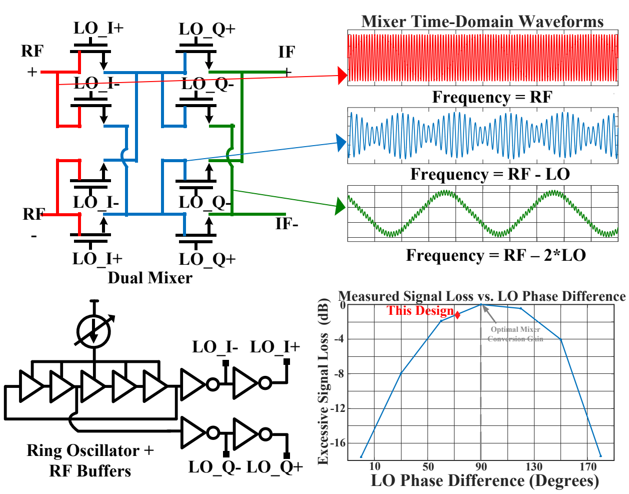

Fig.4 RF front-end circuits: dual mixer and its input, intermediate and output time domain waveforms. Ring oscillator and RF buffers. Mixer excessive loss due to LO phase compared with ideal I/Q.

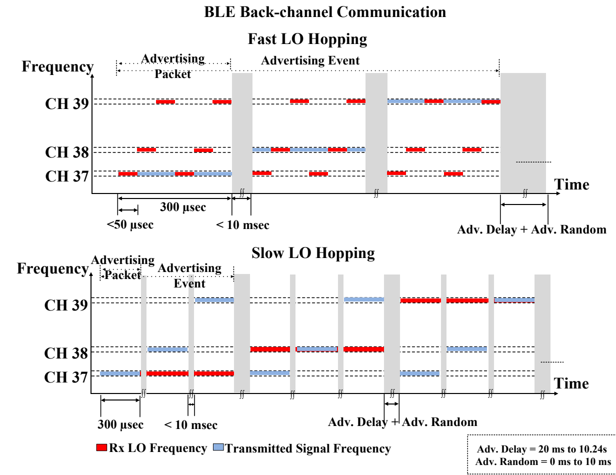

Fig.3 The concept of back-channel communication in fast and slow modes.

III. Receiver Circuits Design

A. RF Front-end

The receiver RF front-end schematic is shown in Fig.4. A ring type oscillator was selected to take advantage of the technology scaling for reducing power consumption [4]. The dual mixer has two passive stages in series driven from the same LO signal source. This effectively performs a two-step down-conversion of the RF signal. Since the mixers are passive switches to save power, the LO phases have to be different between the two stages to effectively down-convert the signal at twice the LO frequency. I/Q LO phases are required to achieve the optimum conversion gain, but Fig.4 shows that some mismatch in phases is acceptable. The plot in Fig.4 also shows that LO phase difference could be up to -30° off from optimum with less than 2 dB signal loss compared with ideal IQ phases. Taking advantage of this trade-off to save power, this design replaces the more traditional, but higher power, differential I/Q ring oscillator with a single-ended ring oscillator having an odd number of stages. The single-ended ring doesn't produce I/Q outputs, but, with 5 stages, the losses from I/Q mismatch are only 1.1 dB of the signal. This design directly downconverts the RF signal at 2×LO frequency to base-band. A current DAC with coarse and fine tuning bits is used to calibrate the oscillator frequency over process, voltage, and temperature (PVT) variations. The tuning bits are also used to hop the oscillator frequency between the three advertising channels using an integrated FLL within 100 KHz resolution. The FLL is based on a counter for the number of the divided LO cycles in one reference clock period, and then comparing that to a target value based on the desired frequency and updating the LO current DAC control bits accordingly.

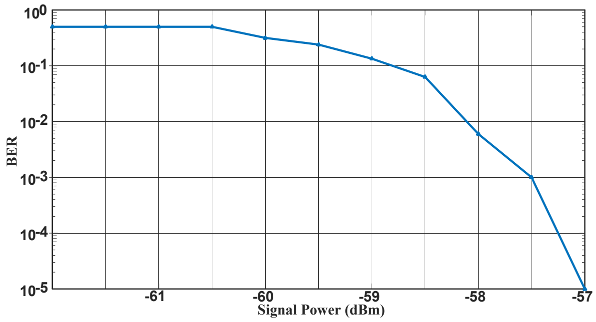

Fig.5 Measured receiver BER vs. signal power

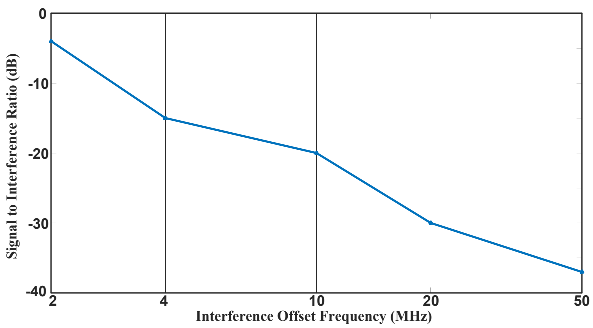

Fig.6 Measured signal-to interference ratio vs. interference offset frequency.

B. *Analog Baseband*

The directly downconverted signal is low-pass filtered at baseband. The filter bandwidth is 2 MHz which is the bandwidth of all BLE channels. This channel selectivity allows the receiver to tolerate, up to a certain extent, adjacent channel interference. Then, the baseband amplifiers provide up to 65 dB of signal gain. A source follower based envelope detector is then used to rectify the signal before digitizing it.

C. *Digital Baseband*

The ED output is processed offline where the signal is first digitized using a one bit comparator. The comparator output is then over-sampled by a factor of 10 to find the packet boundary while the LO frequency is hopping. The bit sequence is correlated with pre-defined templates representing different BC symbols. A wake-up message can be embedded in a BC symbols pattern as additional feature of this communication scheme.

IV. Measurement Results

The back-channel receiver was fabricated in a 65 nm LP CMOS process. The bit error rate (BER) performance in Fig.5 shows the receiver has a sensitivity of -57.5 dBm for a BER of 10^{-3}. Fig.6 demonstrates the signal-to-interference (SIR) performance. The interference rejection was measured to be -4, -20, and -30 dB for the 1st, 5th, and

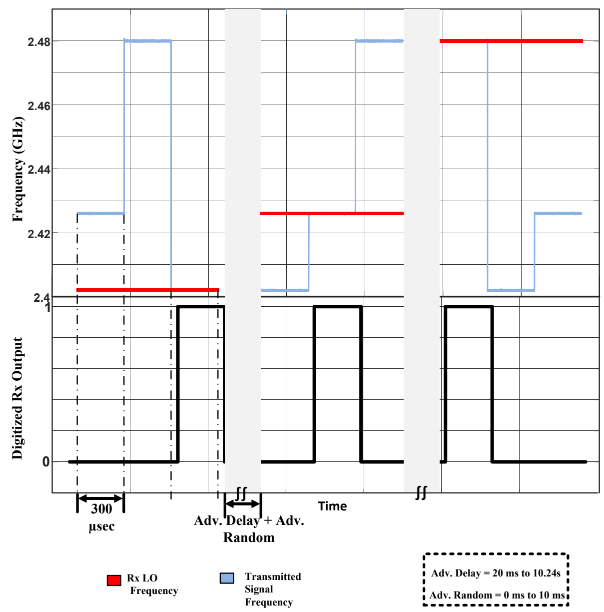

Fig.7 Measured receiver LO frequency and transmitted signal frequency. Digitized receiver output.

10th BLE adjacent channels, respectively. Fig.7 shows the output waveform of the receiver in the slow hopping mode. The waveform demonstrates the receiver ability to selectively listen to the different advertising channels and detect if any transmitted energy exists at these channels. The sequence of advertising packets and events are considered to be valid when the timing gap between them is within the limits set by the BLE standard.

The total power consumption is 150 µW, with 120 µW dissipated by the LO (including its buffers) which are running at 1.2 GHz , the digital FLL, and the LO frequency

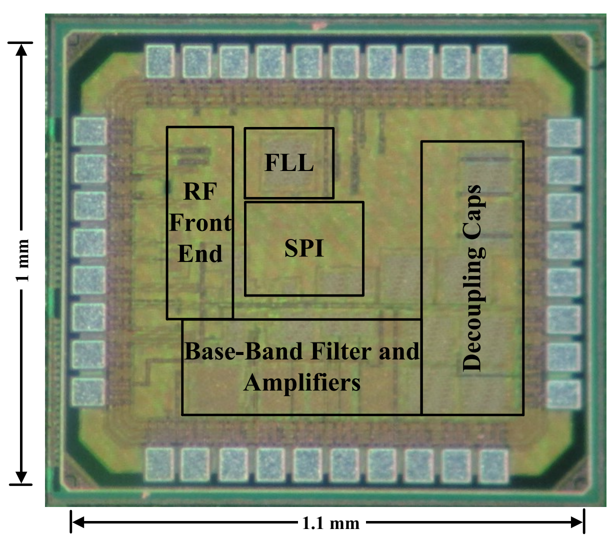

Fig.8 Die micrograph

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF ART.

	This Work	[3]	[5]	[6]	[7]	[8]
Active Power [μW]	150	0.58	600	227*	5500	390
RF Input Frequency [MHz]	2400	2400	2400	2400	2400	2400
WRX Supply [V]	0.9/1.1	0.5/1	0.8	0.6	0.6/1.1	2
Sensitivity [dBm]	-57.5	-39/56	-84.9/-84.2	-83	-90	-58
WRX Modulation	FSK	BLS/ CDMA	-	OOK	GFSK	Constant-Envelope
Rx Data Rate [kbps]	112.5	8.192	-	1000	1000	-
Technology[nm]	65	65	130	65	65	90
Die Area [mm^2]	1.1	2.25	1.2	1.17	9	1.24
BLE Compatible Frequency Hopping	YES	NO	NO	NO	NO	NO
Adjacent Channel SIR (dB) @ 2MHz @ 10 MHz	-4 -20	-	-	8 -22.5	-16 < -30**	-
Channel Selectivity	YES	NO	YES	YES	YES	NO

*Uses External Inductors for VCO and LNA. /** Extrapolated.

dividers. The analog baseband consumes the remaining 30 μW. Table I shows a comparison between this work and the state-of the art. This design consumes the lowest power compared with all other receivers that have channel selectivity in the 2.4 GHz band. To the best of our knowledge, it is the first sub-mW receiver that includes a BLE compatible frequency hopping mechanism. Fig.8 shows the die photo of the chip, which has an area of 1.1 mm^2.

V. CONCLUSION

A BLE back-channel receiver fabricated in CMOS 65nm is presented in this paper. The receiver can decode messages embedded in advertising events sent by commercial BLE devices. Using a dual-mixer as the first stage reduces the power consumption of the receiver by reducing the frequency of the LO. The channel selection, which makes the receiver more robust to interference, is done by hopping the LO frequency while limiting the receiver baseband bandwidth to be the same as that of the BLE channel. The receiver consumes only 150 μW with a sensitivity of -57.5 dBm.

ACKNOWLEDGMENT

The material is supported by NSF under award number F031936.

REFERENCES

[1] J. Prummel *et al*., "A 10 mW Bluetooth Low-Energy Transceiver With On-Chip Matching," in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3077-3088, Dec. 2015.

[2] A. Sai *et al*., "A 5.5 mW ADPLL-Based Receiver With a Hybrid Loop Interference Rejection for BLE Application in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 3125-3136, Dec. 2016.

[3] N. E. Roberts *et al*., "26.8 A 236nW -56.5dBm-sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," *(ISSCC) Digest of Technical Papers*, San Francisco, CA, 2016, pp. 450-451.

[4] N. Pletcher, "Ultra-Low Power Wake-Up Receivers for Wireless Sensor Networks," Ph.D. dissertation, Dept. EECS, Univ. California, Berkeley, 2008.

[5] A. Selvakumar, M. Zargham and A. Liscidini, "13.6 A 600μW Bluetooth low-energy front-end receiver in 0.13μm CMOS technology," *(ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015, pp. 1-3.

[6] L. Jae-Seung, K. Joo-Myoung, L. Jae-Sup, H. Seok-Kyun and L. Sang-Gug, "13.1 A 227pJ/b −83dBm 2.4GHz multi-channel OOK receiver adopting receiver-based FLL," *(ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015, pp. 1-3.

[7] H. Okuni *et al*., "26.1 A 5.5mW ADPLL-based receiver with hybrid-loop interference rejection for BLE application in 65nm CMOS," *(ISSCC) Digest of Technical Papers*, San Francisco, CA, 2016, pp. 436-437.

[8] M. Ding *et al*., "A 2.4GHz BLE-compliant fully-integrated wakeup receiver for latency-critical IoT applications using a 2-dimensional wakeup pattern in 90nm CMOS," *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, 2017, pp. 168-171.