4.32-pJ/b, Overlap-Free, Feedforward Edge-Combiner-Based Ultra-Wideband Transmitter for High-Channel-Count Neural Recording

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***Abstract*— We present an ultralow-power, ultra-wideband (UWB) transmitter (TX) in standard 65-nm CMOS processes. The TX consists of feedforward edge combiners and interpolators for ultralow-power operation and reliable pulse generation that is essential in UWB TXs. The implemented circuit avoids pulse overlapping without complicated calibrations and has achieved an energy efficiency of 4.32 pJ/b at 200-Mbps data rate. The TX is suitable for energy-constraint, high-data-rate applications such as wireless telemetry in implantable high-density neural recording interfaces.**

***Index Terms*— Edge combiner, feedforward, high-channel-count wireless recording system, RF transmitter (TX), ultra-wideband (UWB), ultralow power.**

I. Introduction

ULTRA-WIDEBAND (UWB) technology has drawn extensive attention for short distance, high-data-rate, and ultralow-power applications. One of the most challenging applications is high-density neural interface systems where simultaneous recording and real-time stimulation are essential [1]. It requires 20-Mbps data transmission speed for 1000-channel electrocorticography (ECoG) recording arrays and easily exceeds 200 Mbps for broadband neural recordings with the same channel count.[1] Thanks to highly duty-cycled operation, UWB systems can accommodate such high data rates while maintaining ultralow-power consumption, making it a unique candidate for wireless data transmission of high-density neural interfaces.

To achieve ultralow-power consumption, we adopted the edge-combiner-based pulse generation instead of power-hungry oscillator-based approaches [2], [3]. One of the challenges that need to be addressed in conventional edge-combiner architectures is to minimize the variation of individual delay cells. Significant variations between delay stages can result in inconsistent pulse duty cycles and frequency shifting [4]. As illustrated in Fig. 1, delay variations (Δd_n) can affect the generated pulse duration or the timing of arrival (output 1). In the worst case scenario, the logic gate for combination (XOR) cannot respond to a very short pulse train (output 2). This results in doubling the pulsewidth or reducing the carrier frequency to half. It consequently increases the unwanted spectral density over the maximum cap of Federal Communications Commission (FCC) regulation. Fig. 2 shows the power spectral densities (PSDs) of the generated pulses (output 2). It is clearly observed that the energy spread from inconsistent pulse widths causes the infringement of FCC. In [4], a calibration scheme was adopted by adding capacitor arrays in each delay unit to have a better control of pulse widths. Nevertheless, this manual control approach not only needs continuous monitoring of a stream of pulses but also increases thecomplexity of the system. In this letter, we presented an overlapping-free pulse generation scheme by implementing feedforward compensation in the edge combiner.

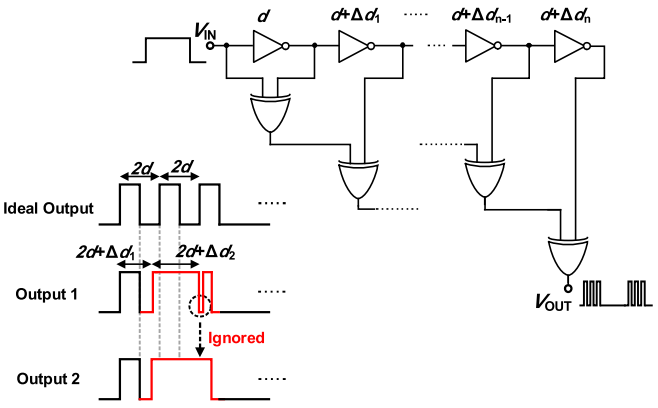

Fig. 1. Schematic of typical edge-combiner circuits and its timing diagram, indicating that delay variations affect the pulse duration of output signals.

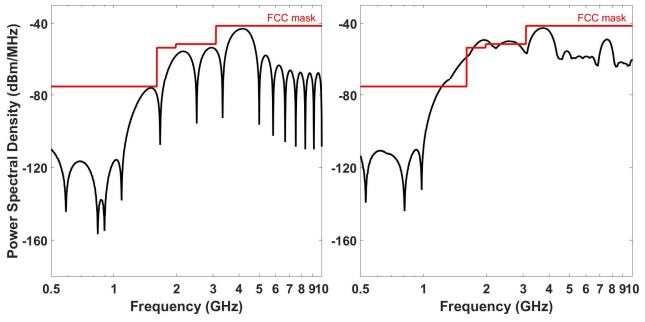

Fig. 2. (a) PSD without overlapping issue (ideal output). (b) PSD with overlapping issue (output 2).

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[1]We assumed 10-b resolution with a sampling rate of 2 kHz for ECoG and 20 kHz for broadband (field potentials + action potentials) recording.

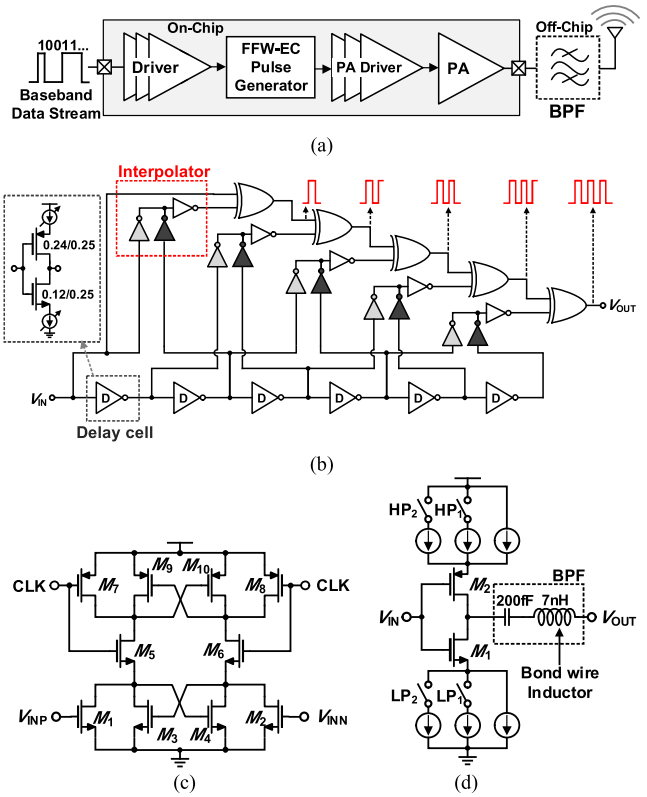


Fig. 3. (a) System architecture of the proposed UWB TX. (b) Conceptual block diagram of feedforward edge-combiner-based pulse generator. (c) Latch-based input driver. (d) Inverter-based PA.

II. Transmitter Architecture

The proposed UWB transmitter (TX) consists of an input driver, a feedforward edge combiner (FFW-EC) with interpolators, and a highly duty-cycled inverter-based power amplifier (PA) driver, as shown in Fig. 3(a). The baseband signal is fed into the input driver at 200-Mbps data rate. The output of the driver then activates the feedforward edge combiner to generate desired pulses. The generated pulses are first amplified by the PA and then fed into a bandpass filter (BPF) which is composed of an on-chip capacitor and a bond-wire inductor. The output is matched to 50 Ω at 4 GHz with a bandwidth of approximately 1 GHz and is connected to an off-chip UWB antenna.

A. Feedforward Edge-Combiner-Based Pulse Generator

The proposed feedforward edge combiner is comprised of a chain of variable delay cells and interpolators [5], which are added between every two delay cells as shown in Fig. 3(b). The delay cell unit is an inverter with two additional programmable current sources for the control of intrinsic delays in order to provide frequency adjustment for multiple-user applications. The interpolator takes the input and output from the two neighboring delay cells and produces a pulse edge with an averaged phase between the two inputs. In mathematical model, the output of the edge combiner is given by

$$y_n(t) = y_{n-1}(t) + x(t+\theta) - 2 \cdot y_{n-1}(t) \cdot x(t+\theta)$$
$$\theta = \begin{cases} (\tau + \Delta t_n) & \text{(conventional)} \\ (2 \cdot \tau + \Delta t_n + \Delta t_{n+1})/2 & \text{(proposed)} \end{cases} \quad (1)$$

where $x(t)$ is the input of the edge combiner, $y_n(t)$ is the output of the nth-stage XOR gate, τ is the intrinsic delay of a delay unit, Δt_n is the variation of delay in each unit, and θ is the actual delay in each stage with effective variations. The actual delay in each stage can be either slower or faster than τ. In the conventional edge-combiner architectures, the variation of delay θ is solely affected by that of each stage, i.e., effective variation $= \Delta t_n$. On the contrary, in the proposed implementation, the delay is averaged between the two stages, where effective variation $= (\Delta t_n + \Delta t_{n+1})/2$, so that the pulse generator is less sensitive to the delay variations of individual stages. The two inverters of the interpolator, shaded in light and dark gray in Fig. 3(b), are sized with a ratio of 1.67 of a unit-size invertor to generate an output edge of averaged phase between the two inputs. The generated edge then feedforwards to the XOR gate input; thus, the falling/rising edges of the XOR gate output will always fall between the two consecutive delay cells to guarantee nonoverlapping pulses in any given baseband signals.

The addition of interpolators imposes power overhead in the system as compared to the conventional edge combiners. However, the proposed feedforward edge combiner can ensure robust nonoverlapping pulses without complicate calibration and continuous supervision required in the conventional systems. Also, precise duty cycles are generated by taking the average of phases between two consecutive delay cells. To compensate for power overhead, we adopted the OOK modulation scheme to relax the power burden in the TX, leaving the high processing overhead to the receiver side, known as asymmetric data transmission. To achieve additional power saving, we implemented pass gate logics. Pass gate logics consume lower switching energy to charge up a node compared to static logics. Also, the number of pulses allocated for sending 1-b information has been assigned to three. At 3.6 GHz, the three pulses take up approximately 1 GHz of bandwidth that sufficiently satisfies the FCC regulations as the minimum bandwidth requirement for UWB is 500 MHz. It also allows multiband transmission for system scalability and multiple-user scenarios.

B. Input Driver and Inverter-Based PA

Because the edge combiner is sensitive to both rising and falling edges, an input driver is required to produce well-defined edges. To save power, a dynamic latch comparator driver is adopted, as shown in Fig. 3(c). Dual cross-coupled pairs, M_{3-4} and M_{9-10}, are implemented to give a fast switching speed. Fig. 3(d) shows the inverter-based (M_1 and M_2) PA. It is implemented with two extra power sink and source pairs, HP_{1-2} and LP_{1-2}, to provide programmability for output power adjustment from −15 to 0 dBm. The output is connected to a BPF which is composed of a 200-fF on-chip capacitor and a 7-nH bond-wire inductor at the band of interest.

III. Experimental Results

The TX has been fabricated using 65-nm CMOS processes with one poly and nine metal layers. The chip is mounted on an FR4 print circuit board (PCB) with voltage regulators to provide stable supplies since the trip point of delay chains is

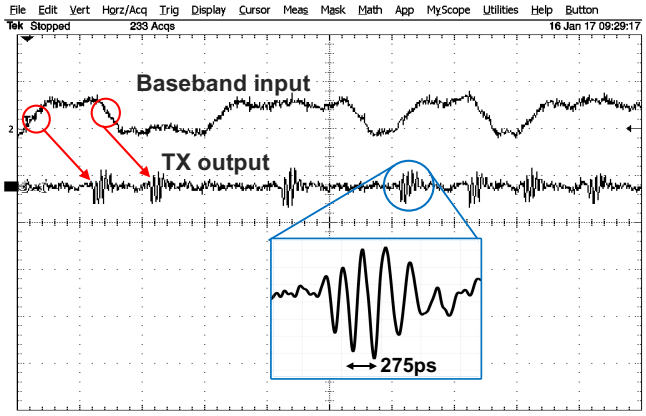


Fig. 4. Measured baseband signal and TX output.

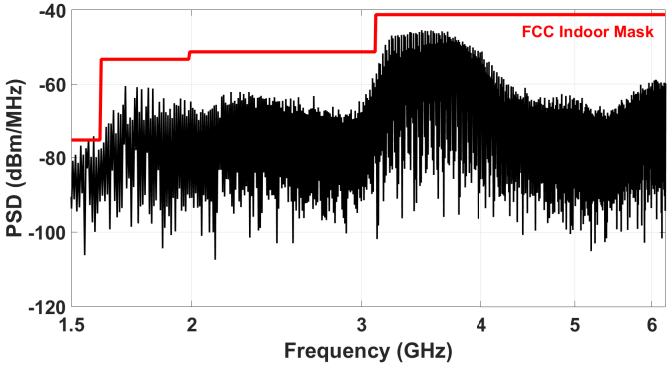
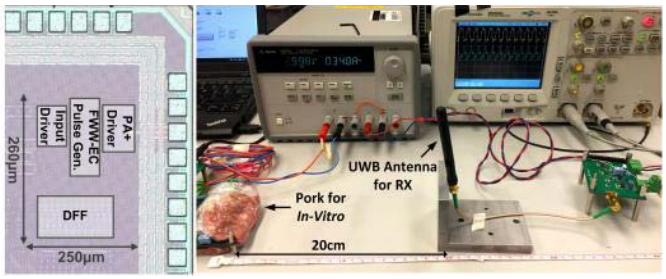


Fig. 5. Measured PSD at a data rate of 200 Mbps.

sensitive to supply variations. If this off-chip linear regulator is replaced by an on-chip converter with high power conversion efficiency, the system power can be further saved [8]. Output matching is done by parasitic capacitance from the PCB along with a bond-wire inductor. Fig. 4 shows the measured baseband signal and the transmitted pulse waveform. The baseband signal is digitized from a subset of prerecorded broadband neural signals. Output pulses are generated and transmitted when input signals toggle. In Fig. 5, the measured PSD is under the FCC indoor mask at 200 Mbps with approximately 1 GHz of bandwidth and a center frequency of 3.6 GHz. Fig. 6(a) shows the chip micrograph. The core area is less than 0.065 mm^2. The system consumes 0.867 mW at 200 Mbps which is equivalent to 4.34 pJ/b at 1-V power supply. To demonstrate the functionality of the proposed TX, an *in vitro* testing setup has been made [Fig. 6(b)]. The antenna, TDK ANT1085, at the TX side is covered with 5-mm-thick ground pork at both top and bottom to emulate the signal transmission from an implanted system. At the receiver side, off-the-shelf components are assembled on the PCB for signal amplification and detection, including MGA 86563 (Broadcom) for LNA, 4000BP (Johnson Technology) for BPF, and HMC713LP3E (Analog Devices) for RF power detector. Signal is retrieved from a distance of 20 cm with bit error rate $< 10^{-3}$ at a data rate of 50 Mbps, which is constrained by the bandwidth of RF power detector. Table I summarizes the performance compared with recently published state-of-the-art results. This letter has achieved the lowest figure of merit (FoM).



(a) (b)

Fig. 6. (a) Chip microphotograph. (b) *In vitro* distance testing setup.

TABLE I
PERFORMANCE COMPARISON WITH RECENT WORKS

	Tech. [nm]	Area [mm^2]	Pulse Generator	Data rate [Mbps]	P_{OUT} [dBm]	Power [mW]	FoM [pJ/b]
[2]	65	4.6*	Oscillator	1000	-8.7	21.4	21.4
[3]	65	1.7	Oscillator	1000	-26	7.46	7.46
[4]	65	0.182	E.C.	200	-4	36	180
[6]	90	0.37	E.C.	12	-7	0.54	45
[7]	65	0.032	Oscillator	0-50	-11	0.8	8-16
This work	**65**	**0.065**	**E.C.**	**200**	**-9**	**0.86**	**4.32**

*Including TRX E.C. = Edge Combiner

IV. CONCLUSION

In this letter, a robust overlap-free ultralow-power UWB TX is presented by using 65-nm CMOS technology. It successfully regulates the timing of rising/falling edges and ensures nonoverlapped pulse train by implementing feedforward edge combiners. It has achieved the lowest FoM of 4.32 pJ/b at 200 Mbps with frequency programmability for multiuser scenarios. This letter is applicable to accommodate 1000-channel broadband neural signal recording and 10k-channel ECoG recording.

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